STRUCTURE OF IC PAD AND ITS FORMING METHOD

Field of the Invention:

The invention relates to a structure of IC pad and its forming method, in particular to a structure and method that are adapted to form a pad of integrated circuit of high frequency and low noise; not only the noise from the semiconductor substrate be separated effectively and the value of equivalent electric capacitance of the pad be lowered, but also the bonding adherence be further enhanced.

Background of the Invention:

Recently, since the requirement of transceiver of low power and low cost is steadily on the increase, so the technology of mainstream IC competitively concentrates on how to realize further more functions of radio frequency on one single chip. Except making integrated circuit be able to arrange on the package substrate, the external circuit connected by the external legs of package substrate must be electrically connected to the integrated circuit. So, when packaging the integrated circuit, the technology of pad has become an important factor that influences the yield and quality of a product. This pad adapted for providing electric connection between the integrated circuit and the external circuit is usually arranged in the metal zone around the IC die. When the pad is formed, the metal connecting wire must contact with the pad accurately and connect to the external legs of the IC packaging substrate. Because of the limitation of the prior arts and the characteristics of metal connecting wire and pad, the area of pad is sometimes too large to occupy too much area of chip. Furthermore, during high frequency, the performance of the integrated circuit is influenced because the equivalent electric capacitance is too large.

Additionally, because of the market growth of communication IC recently, the operational frequency of integrated circuit is also growing in indexing type. The

low noise and low loss o f high frequency signal are always the pursuing goals for communication IC.

In 1987, the US Patent No. 4,636,832 "Semiconductor device with an improved bonding section" proposed a design method of the pad of integrated circuit. Please refer to Fig. 1, which is a cross-sectional diagram of the IC device disclosed in the US Patent No. 4,636,832. The characteristic of this prior art is that the semiconductor element 10 is arranged below the pad 15. Although it may reduce the area of layout, this kind of pad can not be adapted to high frequency circuit with low noise because the noise coming from the semiconductor substrate 20 will directly influence the signal of high frequency when it passes through the pad.

To overcome the tensile and tension of bonding, the US Patent No. 5,248,903 "Composite pads for semiconductor devices" proposed a kind of pad. Please refer to Fig. 2, which is the cross-sectional diagram of the IC device disclosed in the US Patent No. 5,248,903. Wherein, the pad 30 has at least two layers of electric-conduction layer 30a and 30c and a connection layer 30b. But, this kind of pad is not adapted for the signals of high frequency and low noise because the noise of semiconductor substrate 35 will directly influence the quality of signal.

The US Patent No. 5,502,337 "Semiconductor device structure including multiple interconnection layers with interlayer insulating films" proposed a different designing method for pad. Please refer to Fig. 3, which is a cross-sectional diagram for the IC device disclosed in the US Patent No. 5,502,337, which arranges the connection layer 40a in the pad 40 around the bonding zone 45. When the integrated circuit is manufactured, a bonding zone of arc shape will be formed on the pad 40 to thereby enhance the bonding adherence. However, the technology of current integrated circuit has stepped into the levels of sub micrometer or deep sub micrometer, and CMP (Chemical-Mechanical Polish) is already a standard procedure for current semiconductor process. So, this kind of prior art no longer generates original effectiveness in current semiconductor process, besides this technique has the same drawback as that of previous

techniques; i.e., it can not separate the noise coming from the semiconductor substrate 50.

From above discussion, we know that the prior arts described there are unable to propose an effective solution that aims for the high frequency, low noise and bonding adherence. Therefore, the emphasis of the invention is to provide a pad structure adapted for a integrated circuit of high frequency and low noise to lower down the equivalent electric capacitance and enhance the bonding adherence, such that it can prevent the entire pad from being drawn out of the semiconductor chip by the tension generated in the bonding procedure.

SUMMARY OF THE INVENTION

The main objective of the present invention is to provide a structure of IC pad and its forming method, which are adapted for the structure of the pad of an integrated circuit of high frequency and low noise, such that the effective area of the pad may be reduced effectively to thereby reduce its value of equivalent electric capacitance.

The second objective of the present invention is to provide a structure of IC pad and its forming method effectively separate the noise coming from the semiconductor substrate.

The further objective of the present invention is to provide a structure of IC pad and its forming method effectively enhance the bonding adherence, such that it prevent the entire pad from being drawn out of the semiconductor chip by the tension generated in the bonding procedure.

To achieve above objectives, the invention provides an IC pad structure arranged in an insulation layer comprises a lower electric-conduction layer, a compound layer structure and a pad layer.

The lower electric-conduction layer is arranged in the insulation layer and is connected to an electric potential.

The compound layer structure arranged on the insulation layer comprises at least one electric-conduction layer and at least one electric-conduction connecting layer, each of the electric-conduction layer are connected to each other.

The pad layer is arranged on the compound layer structure.

To achieve above objectives, the invention further presents method for forming IC pad structure, comprising the following steps of:

Step (a): providing a substrate arranged with an insulation layer.

Step (b): forming a lower electric-conduction layer which prepared connect to an electric potential .

Step (c): forming a compound layer structure composed by inter-overlapping or connect at least one electric-conduction layer and at least one electric-conduction connecting layer on the insulation layer.

Step (d): forming a pad layer on the compound layer structure, of which area is larger than that of the electric-conduction layer of the compound layer structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional diagram for the IC device disclosed in the US Patent No. 4,636,832.

Fig. 2 is a cross-sectional diagram for the IC device disclosed in the US Patent No. 5,248,903.

Fig. 3 is a cross-sectional diagram for the IC device disclosed in the US Patent No. 5,502,337.

Fig. 4 is an upper side view for the structural illustration of a preferable embodiment of the IC pad according to the invention.

Fig. 5 is a cross-sectional view along the A-A line cutting through Fig. 4 illustrating the preferable embodiment of the IC pad according to the invention.

Fig. 6 is a flowchart illustrating the preferable embodiment of the method forming the IC pad according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

For your esteemed member of reviewing committee to further recognize and understand the characteristics, objectives, and functions of the present invention, a detailed description together with corresponding drawings are presented thereinafter.

The invention discloses a structure of IC pad and its forming method. Its embodiments are described according to referential drawings, in which similar referential numbers represent similar elements.

Please refer to Fig. 4 and Fig. 5, which are structural illustrations for the preferable embodiments of the IC pad according to the present invention. The structure of the IC pad according to the invention is formed in an insulation layer 500 on a substrate 500. The IC pad structure includes a lower electric-conduction layer 300, a compound layer structure 100, and a pad layer 600. Two sides of the lower electric-conduction layer 300 arranged at appropriate position in the insulation layer 500 are respectively arranged with plural electric-conduction layers and plural electric-conduction connecting layers 201, all which are inter-overlapped to each other, such that the lower electric-conduction layer 300 may connect and conduct electric signals to a pad layer 700 arranged on the upper surface exposing on the insulation layer 500 through this structure constructed by multiple inter-overlapped layers to further provide a connection to a device with potential (not shown in the drawings). The pad layer 700 further forms a bonding zone with a chip passivation layer 205. In the meantime, the noise transferred from the substrate 400 will be kept away by the lower electric-conduction layer 300 and may be connected to a cleaner power source or electric potential by the pad layer 700.

The compound layer structure 100 is arranged on the insulation layer 500 and is composed of at 1east one electric-conduction layer 102 and at least one electric-conduction connecting layer 101, both which are inter-overlapped to each

other. The pad layer 600 is arranged on the compound layer structure 100 and is adjacent to the top face side of the insulation layer 500. In the preferable embodiments according to the invention and in order to lower down the value of the effective capacitance of the entire pad, the pad layer 600 is realized by the structuring method of polygon shape and the area of the electric-conduction layer 102 is designed to be smaller than that of the pad layer 600, such that the value of the equivalent electric capacitance to the lower electric-conduction layer 300 may be further effectively lowered down. The electric-conduction layer 102 may be realized by the methods of railing structure or honeycomb structure that may reduce the area of electric-conduction layer 102. The electric-conduction connecting layer 101 further includes plural via and plural via plugs. The structure of this electric-conduction connecting layer 101 may be modified and implemented by those who are skilled in such art according to above disclosure, but it still possesses the merits of the invention and is also within the spirit and scope of the invention, so repetitious description is not presented herein.

In the preferable embodiments according to the invention, the IC pad structure further includes a passivation layer 105, which is arranged on the insulation layer 500 and is partially connected to the pad layer 600. From above design, the compound layer structure 100 is signally connected and structured to the pad layer 600, and a steady bonding zone is thereby formed, such that it may enhance the boding tension and effectively raise the bonding adherence. Therefore, the tension generated during the bonding procedure to draw the entire structure of the IC pad out of the semiconductor chip may be prevented.

In order to further recognize and understand the characteristics, objectives and functions of the present invention, please refer to Fig. 6, which is a flowchart illustrating the preferable embodiment of the method forming the IC pad according to the invention, wherein the numbers 91, 92, 93, 94 and 95 shown in the drawing respectively illustrate the steps from (a) to (e) of the method forming the IC pad according to the invention.

Step (a): providing a substrate that is arranged with an insulation layer thereon.

Step (b): forming a lower electric-conduction layer at an appropriate position in the insulation layer; the lower electric-conduction layer is composed of plural electric-conduction layers and plural electric-conduction connecting layers. In this embodiment, each of the electric-conduction layer is interlaced-connected to the corresponding electric-conduction connecting layers, as shown in FIG. 5, such that a signal connection may be provided to a bond-pad electric-connection layer, which further forms a bonding zone with a passivation layer, such that the pad layer may be connected to a potential of cleaner power source or electric potential.

Step (c): a compound layer structure formed on the insulation layer is composed of at least one electric-conduction layer and at least one electric-conduction connecting layer, each of the electric-conduction layer is interlaced-connected to the corresponding electric-conduction connecting layers, as shown in FIG. 5, and the area of the electric-conduction layer can be reduced by the methods of railing structure or honeycomb structure, and the electric-conduction connecting layer further includes the structure of plural via and plural via plugs.

Step (d): forming a pad layer on the compound layer structure, wherein the area of the former is larger than that of the electric-conduction layer of the latter, and the pad layer is structured as a polygon shape.

Step (e): forming a passivation layer on the insulation layer, such that the pad layer may form a bonding zone with the passivation layer.

Accordingly, the structure of an IC pad and its forming method according to the invention may indeed reduce the value of equivalent electric capacitance of the entire pad, separate the noise coming from the semiconductor substrate, and increase the bonding adherence, so this kind of designing method may be adapted to integrated circuit of high frequency and fulfill the requirement of high frequency and low noise.

WHAT IS CLAIMED IS:

1. An IC pad structure, which is arranged in an insulation layer, comprising:

a lower electric-conduction layer arranged in the insulation layer is connected to an electric potential;

a compound layer structure arranged on the insulation layer comprises at least one electric-conduction layer and at least one electric-conduction connecting layer, the at least one electric-conduction layer is interlaced-connected to the corresponding electric-conduction connecting layers; and

a pad layer arranged on the compound layer structure.

2. The IC pad structure according to claim 1, wherein the area of the lowermost electric-conduction layer of the compound layer structure is smaller than that of the pad layer.

3. The IC pad structure according to claim 1, wherein the pad layer is a polygon.

4. The IC pad structure according to claim 1, wherein the electric-conduction layer of the compound layer structure is a railing.

5. The IC pad structure according to claim 1, wherein the electric-conduction layer of the compound layer structure is a honeycomb.

6. The IC pad structure according to claim 1, wherein the lower electric-conduction layer is provided for separating the noise coupling to the substrate.

7. The IC pad structure according to claim 1, wherein the electric-conduction connecting layer further comprises plural via and plural via plugs.

8. The IC pad structure according to claim l, wherein the insulation layer is arranged on a substrate.

9. The IC pad structure according to claim 1, wherein the IC pad structure further comprises a passivation layer arranged on the insulation layer.

10. An IC pad structure, comprising:

a substrate;

an internal circuit arranged on the substrate;

an insulation layer arranged on the internal circuit;

a lower electric-conduction layer arranged in the insulation layer is connected to an electric potential;

a compound layer structure arranged on the insulation layer comprises at least one electric-conduction layer and at least one electric-conduction connecting layer, wherein the at least one electric-conduction layer is interlaced-connected to the corresponding electric-conduction connecting layers; and

a pad layer arranged on the compound layer structure.

11. The IC pad structure according to claim 10, wherein the electric-conduction layer of the compound layer structure is structured as a honeycomb.

12. The IC pad structure according to claim 10, wherein the area of the lowermost electric-conduction layer of the compound layer structure is smaller than that of the pad layer.

13. The IC pad structure according to claim 10, wherein the pad layer is a polygon.

14. The IC pad structure according to claim 10, wherein the lower electric-conduction layer is provided for separating the noise coupling from the substrate.

15. The IC pad structure according to claim 10, wherein the IC pad structure further comprises a passivation layer arranged on the insulation layer.

16. An IC pad structure, which is arranged in an insulation layer, comprising:

an electric-conduction layer arranged in the insulation layer;

an electric-conduction connecting layer arranged on the electric-conduction layer comprises plural vias and plural via plugs; and

a pad layer arranged on the compound layer structure;

wherein the area of the lowermost electric-conduction layer is smaller than that of the pad layer, such that the value of the equivalent electric capacitance of the IC pad structure lowered.

17. The IC pad structure according to claim 16, wherein the pad layer is a polygon.

18. The IC pad structure according to claim 16, wherein the insulation layer is arranged on a substrate.

19. The IC pad structure according to claim 16, wherein the IC pad structure further comprises a passivation layer arranged on the insulation layer.

20. A method for forming IC pad structure, comprising the following steps of:

(a) providing a substrate arranged with an insulation layer;

(b) forming a lower electric-conduction layer connected to an electric potential in the insulation layer;

(c) forming a compound layer structure composed by interlaced-connecting at least one electric-conduction layer and at least one electric-conduction connecting layer on the insulation layer; and

(d) forming a pad layer on the compound layer structure, of which area is larger than that of the electric-conduction layer of the compound layer structure.

21. The method for forming IC pad structure according to claim 20, wherein the electric-conduction connecting layer in step (c) further comprises plural vias and plural via plugs.

22. The method for forming IC pad structure according to claim 20, wherein a step further comprises:

(e) forming a passivation layer on the insulation layer.