02104/04
20040020129

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 May 2003 (01.05.2003)

PCT

(10) International Publication Number
WO 2003/036449 A1

(51) International Patent Classification[7]: G06F 1/26, 1/32

(21) International Application Number:
PCT/US2002/033833

(22) International Filing Date: 22 October 2002 (22.10.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/682,816 22 October 2001 (22.10.2001) US

(71) Applicant: INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors: SMITH, Jack, Robert; 11 Catkin Drive, South Burligton, VT 05403 (US). VENTRONE, Sebastian, Theodore; 38 Butler Drive, South Burlington, VT 05403 (US).

(74) Agent: ABATE, Joseph, P.; International Business Machines Corporation, Dept. 18G/Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

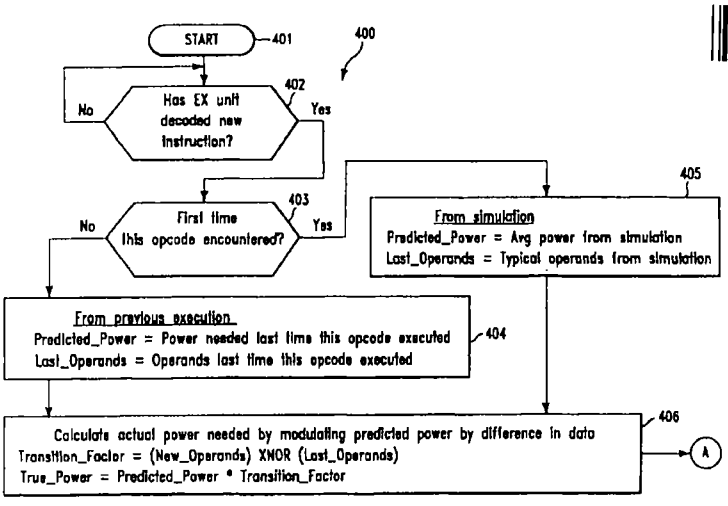
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR CONTROLLING DATA RATE ON A FORWARD CHANNEL IN A WIRELESS COMMUNICATION SYSTEM



(57) Abstract: In a first aspect, a method is provided for conserving power in a processing integrated circuit. This method includes the steps of calculating (401-408) power consumption for executing an instruction and data corresponding to the instruction; and executing (409, 410) the instruction if such execution does not exceed a predetermined power level. In a second aspect, a method is provided for conserving power in a processing integrated circuit employing a plurality of execution units. The method includes the steps of comparing (301, 302) a total power to be consumed by the processing integrated circuit to a power budget for the processing integrated circuit; and if the total power exceeds the power budget, freezing (304) execution of an instruction by one of the plurality of execution units so as to allow execution of the instruction to continue at a later time from where execution waSt frozen. Numerous other aspects are provided, as are systems and apparatus.

162162

WO 2003/036449 A1

ACTION

(48) **Date of publication of this corrected version:**
26 August 2004

(15) **Information about Correction:**
see PCT Gazette No. 35/2004 of 26 August 2004, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.