

ABSTRACT

PACKAGE SUBSTRATE, SEMICONDUCTOR PACKAGE, AND ELECTRONIC DEVICE

This application provides a package substrate, a semiconductor package, and an electronic device. The package substrate includes a substrate body. The substrate body is provided with a plurality of unit regions. Each unit region includes at least one solder ball group. The solder ball group includes a first solder ball, a second solder ball, a third solder ball, a fourth solder ball, a fifth solder ball, and a sixth solder ball that are arranged at spacings. The first solder ball, the second solder ball, the third solder ball, and the fourth solder ball are respectively located at four vertices of a parallelogram, and the second solder ball and the third solder ball each are adjacent to the first solder ball. The fifth solder ball is provided on a side of the parallelogram and is located between the first solder ball and the third solder ball. The sixth solder ball is provided on another side of the parallelogram and is located between the second solder ball and the fourth solder ball. The first solder ball and the fourth solder ball are located on a perpendicular bisector of a connection line between the fifth solder ball and the sixth solder ball. This can reduce crosstalk between pins and reduce a package area, to implement a high-density and low-crosstalk pin arrangement mode.

[Figure 2]