Fig. 1A

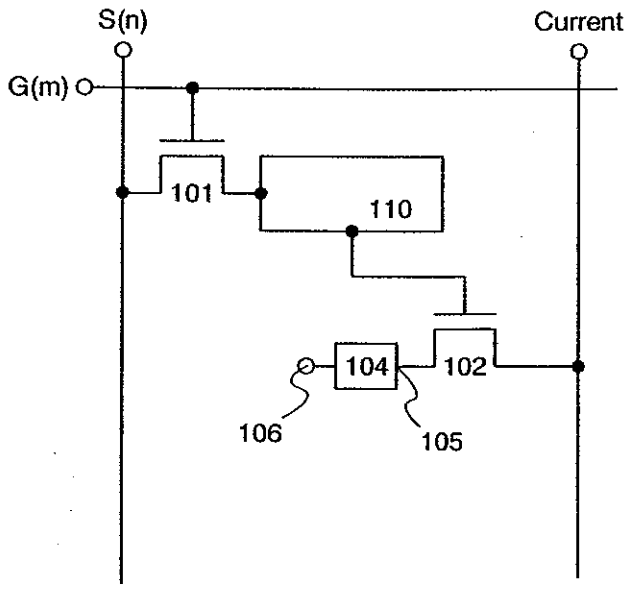

S(n)
Current
G(m)
101
110
104
102
106
105

Fig. 1B

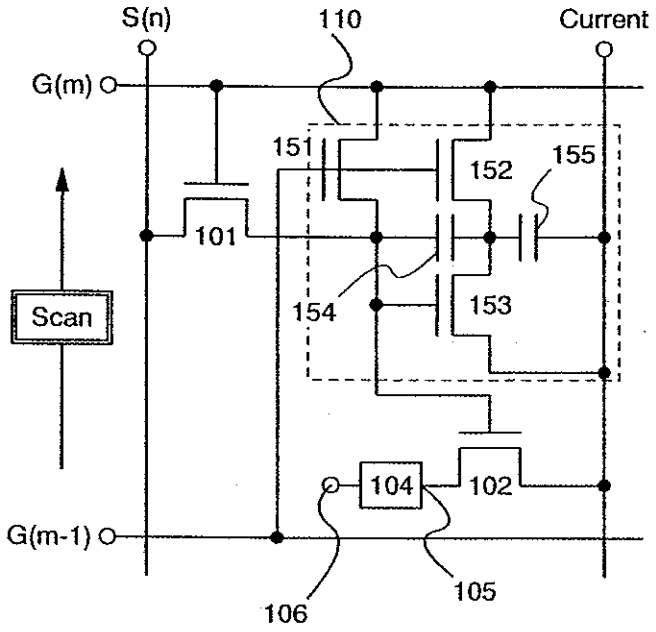

S(n)
110
Current
G(m)
151
152
155
101
Scan
154
153
104
102
G(m-1)
106
105

Fig. 2A

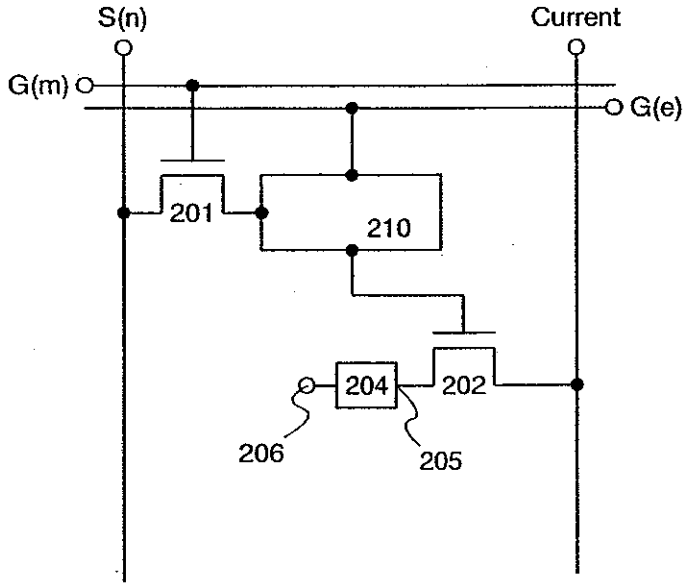

S(n)
Current
G(m)
G(e)
201
210
204
202
206
205

Fig. 2B

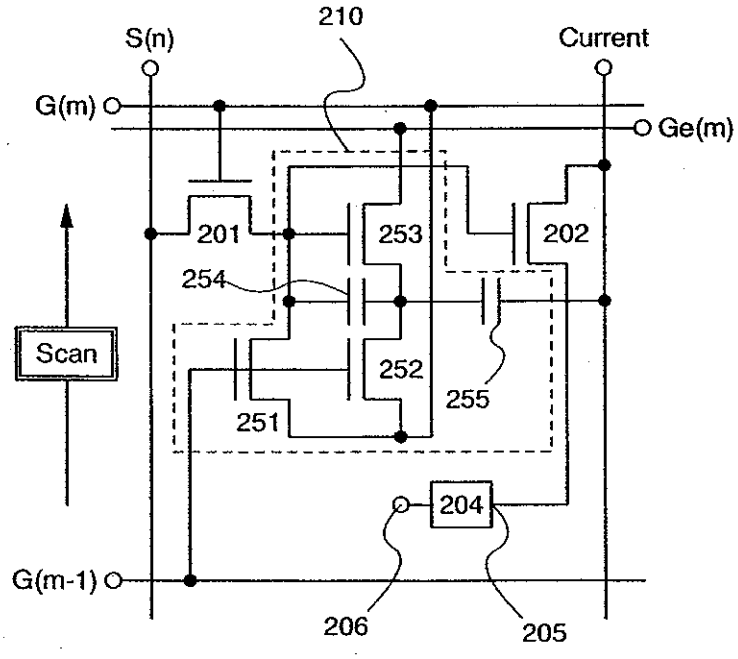

210
S(n)
Current
G(m)
Ge(m)
201
253
202
254
Scan
252
255
251
204
G(m-1)
206
205

Fig. 3A

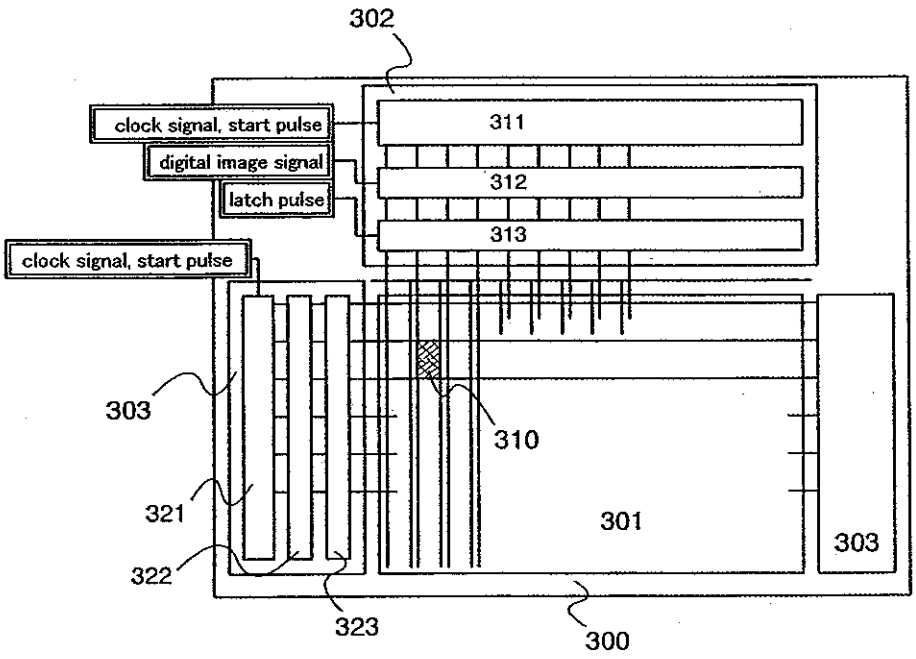

302
clock signal, start pulse
digital image signal
latch pulse
clock signal, start pulse
311
312
313
303
310
321
301
303
322
323
300

Fig. 3B

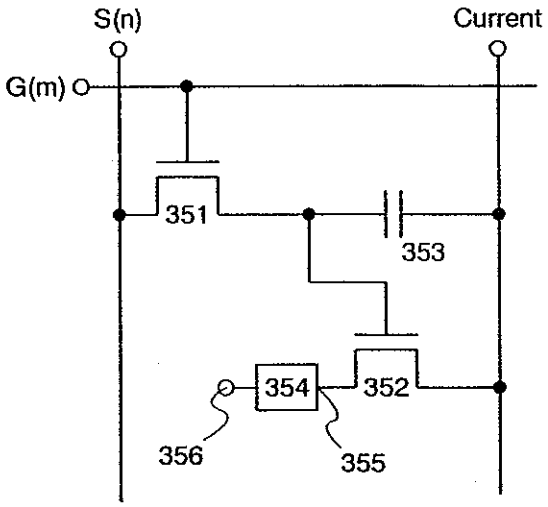

S(n)
Current
G(m)
351
353
354
352
356
355

Fig. 4A

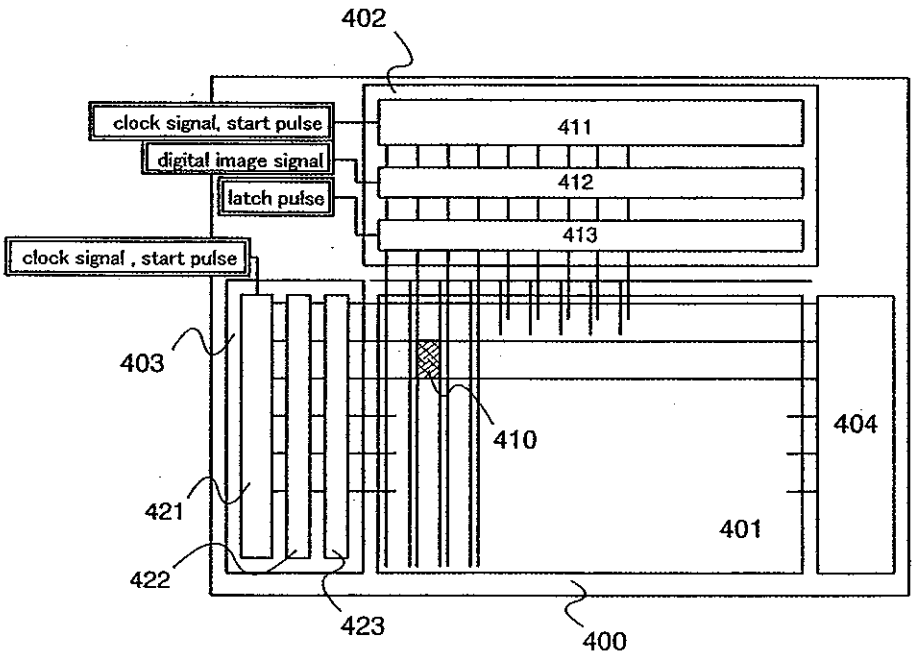

402
clock signal, start pulse
digital image signal
latch pulse
clock signal , start pulse
411
412
413
403
410
404
421
401
422
423
400

Fig. 4B

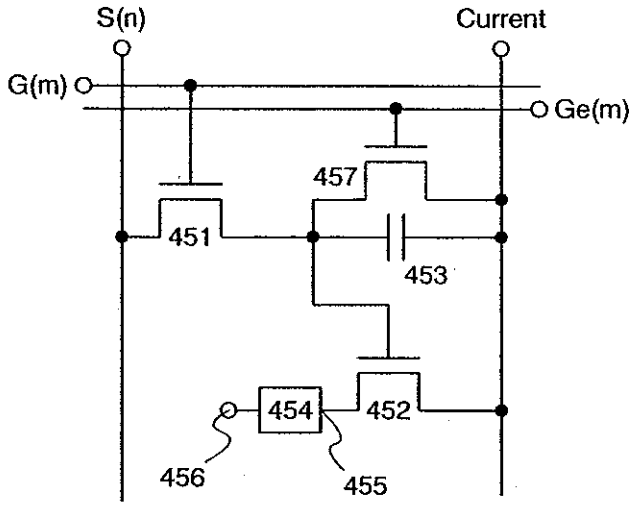

S(n)
Current
G(m)
Ge(m)
457
451
453
454
452
456
455

Fig. 5A

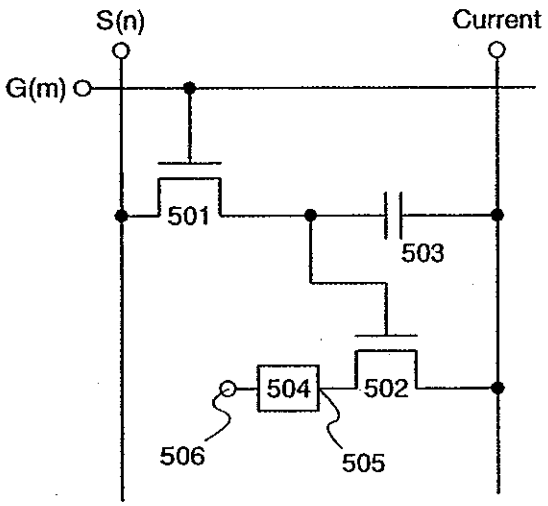

S(n)
Current
G(m)
501
503
504
502
506
505

Fig. 5B

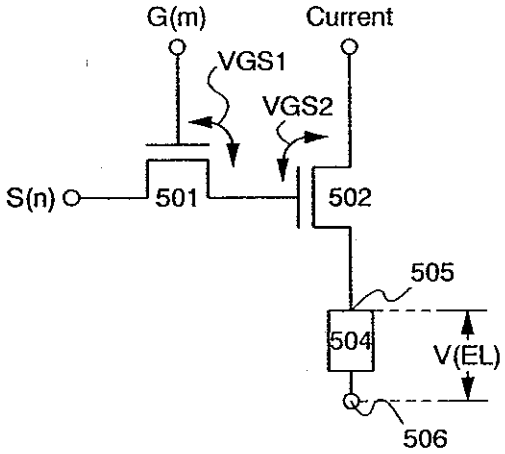

G(m)
Current
VGS1
VGS2
S(n)
501
502
505
504
V(EL)
506

Fig. 6A

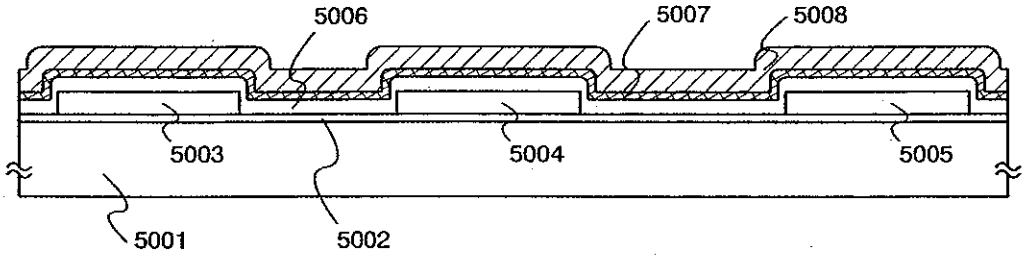


Fig. 6B

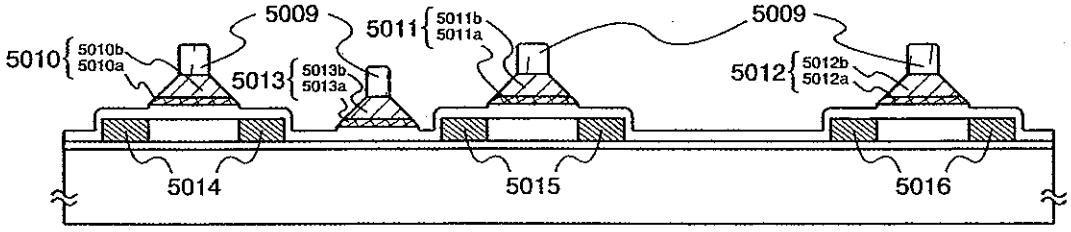


Fig. 6C

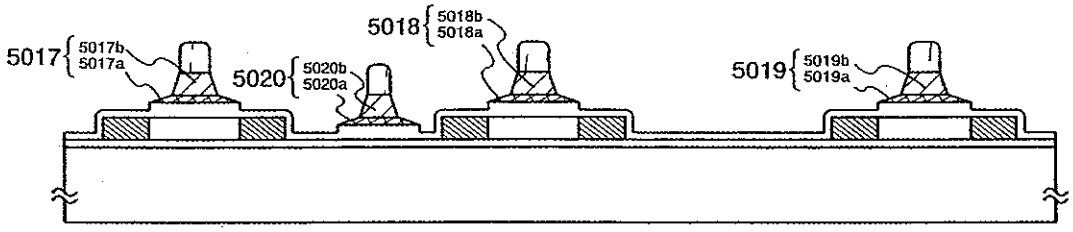


Fig. 6D

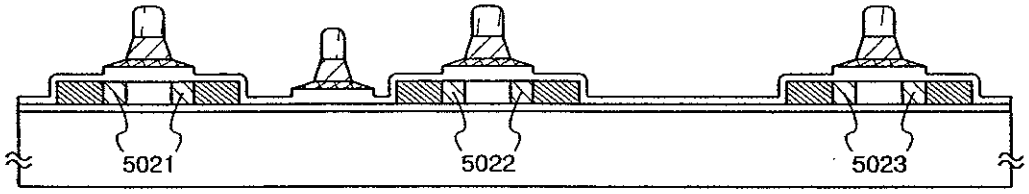


Fig. 7A

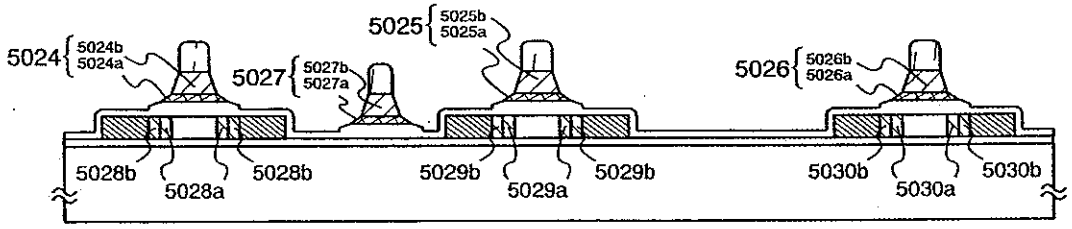


Fig. 7B

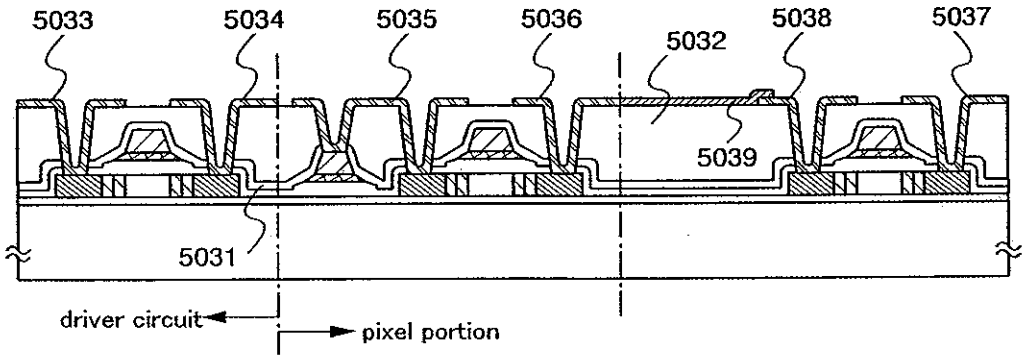


Fig. 7C

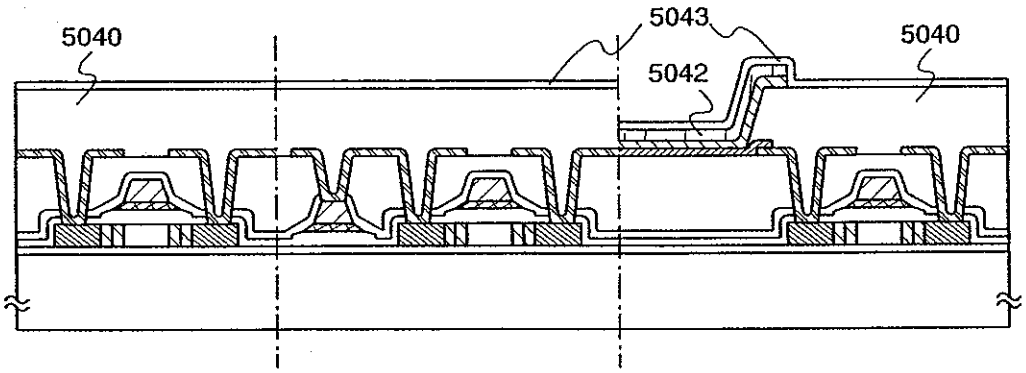


Fig. 8A

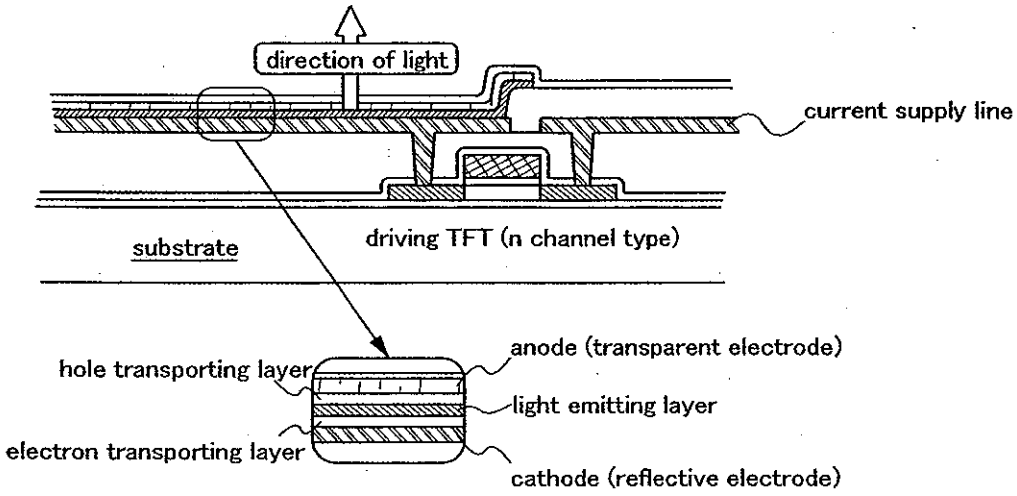

direction of light
current supply line
substrate
driving TFT (n channel type)
anode (transparent electrode)
hole transporting layer
light emitting layer
electron transporting layer
cathode (reflective electrode)

Fig. 8B

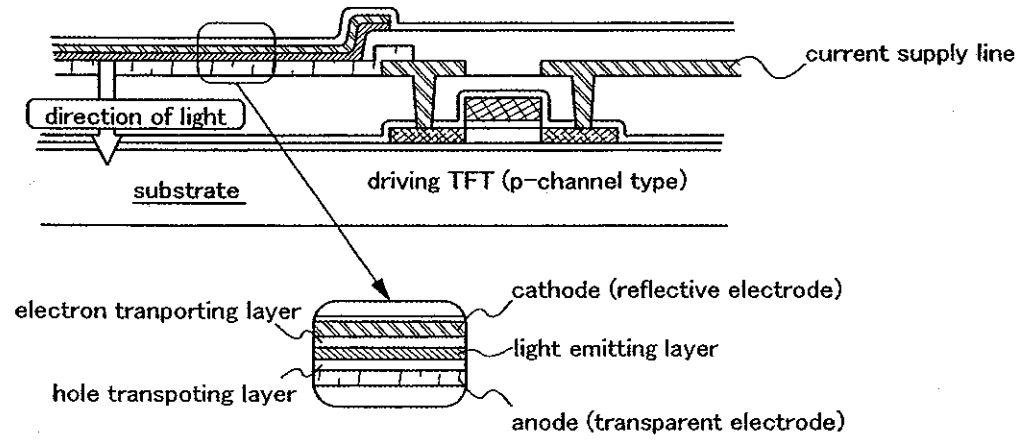

current supply line
direction of light
substrate
driving TFT (p-channel type)
cathode (reflective electrode)
electron tranporting layer
light emitting layer
hole transpoting layer
anode (transparent electrode)

Fig. 9A

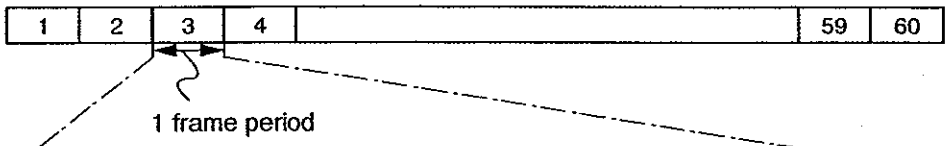


Fig. 9B

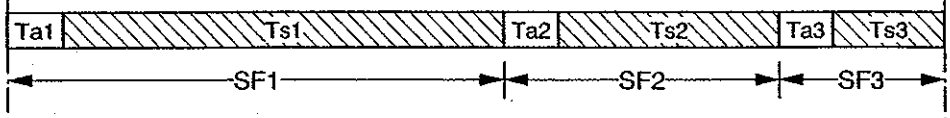


Fig. 9C

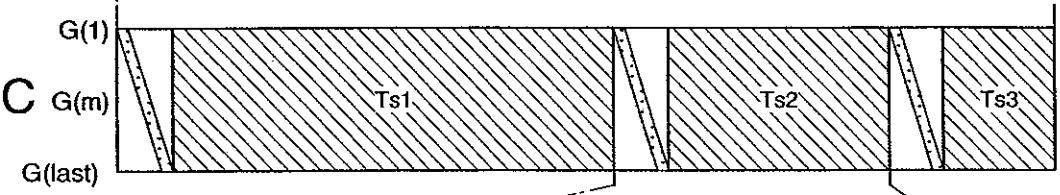


Fig. 9D

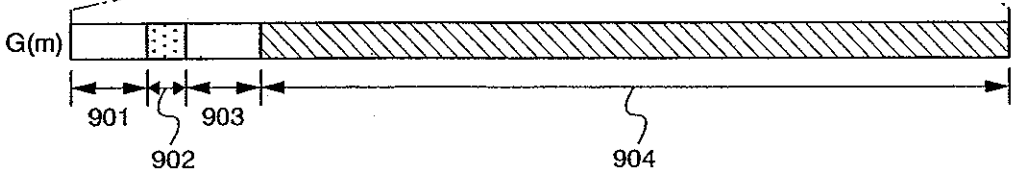


Fig. 9E

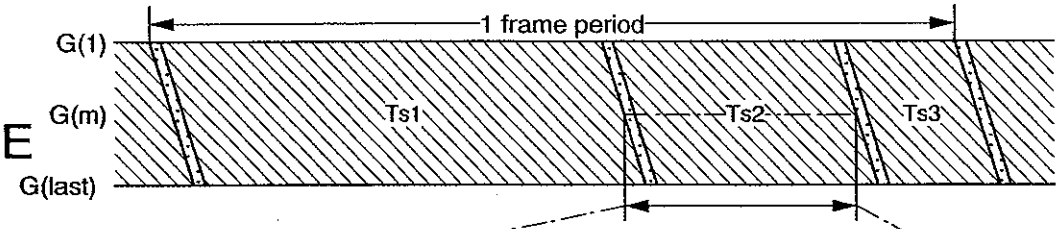


Fig. 9F

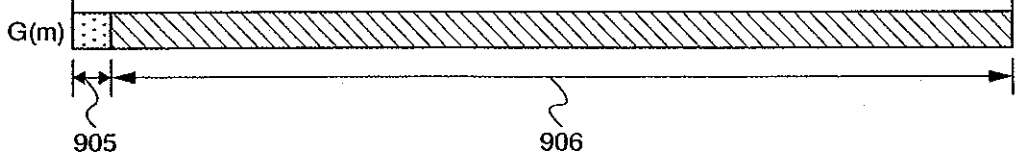


Fig. 10A

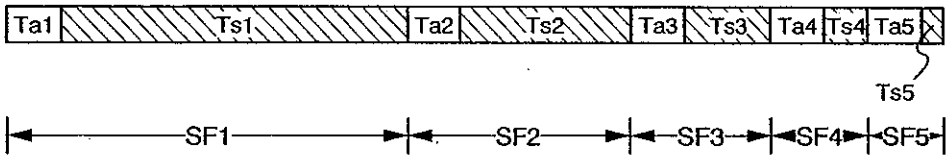


Fig. 10B

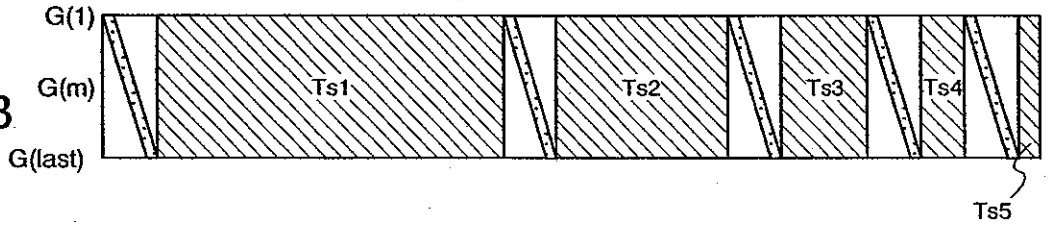


Fig. 10C

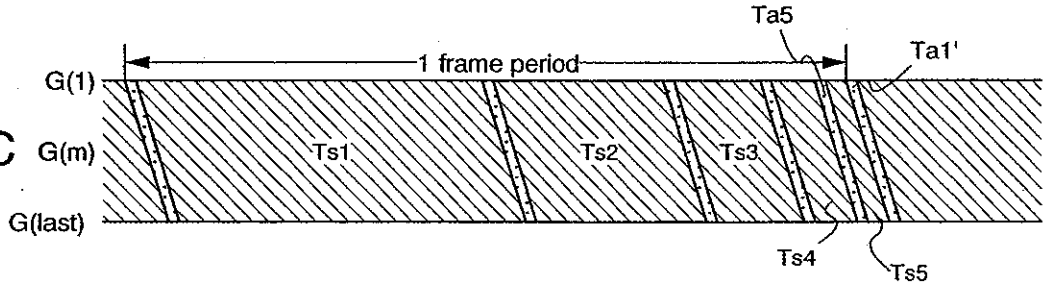


Fig. 10D

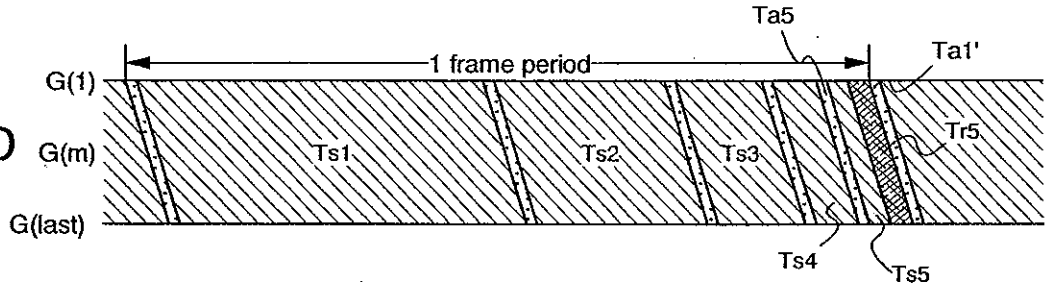


Fig. 11A

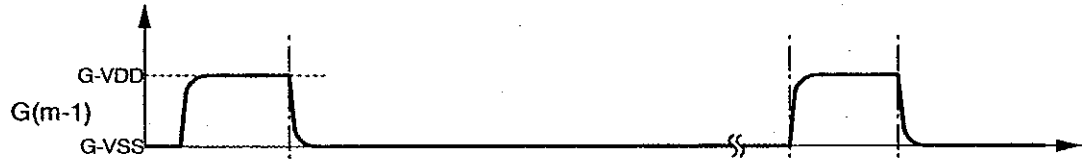


Fig. 11B

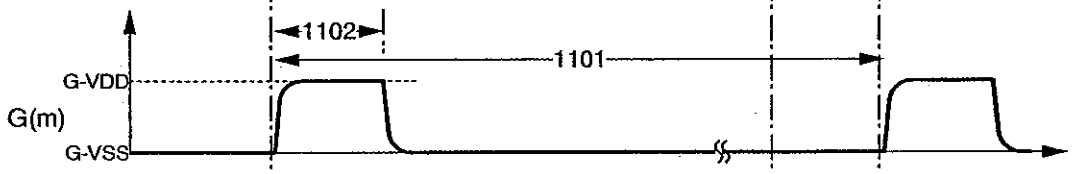


Fig. 11C

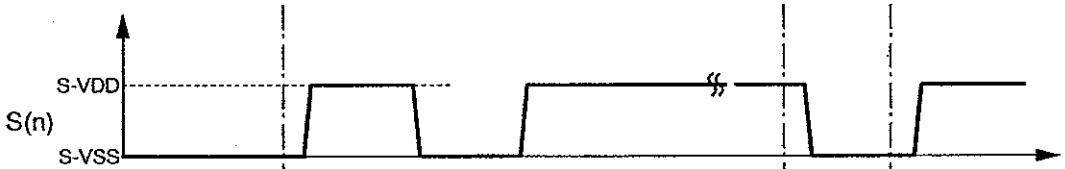


Fig. 11D

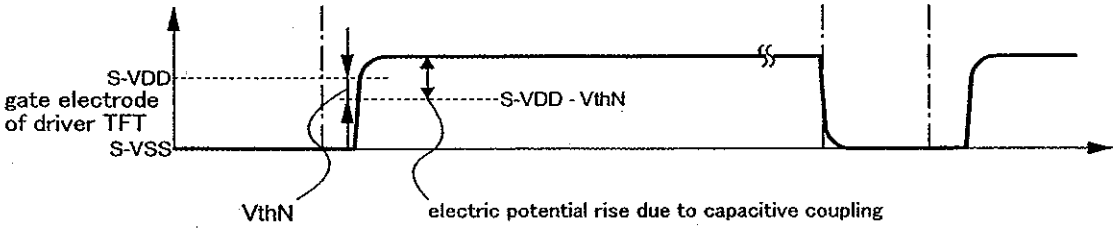


Fig. 12A

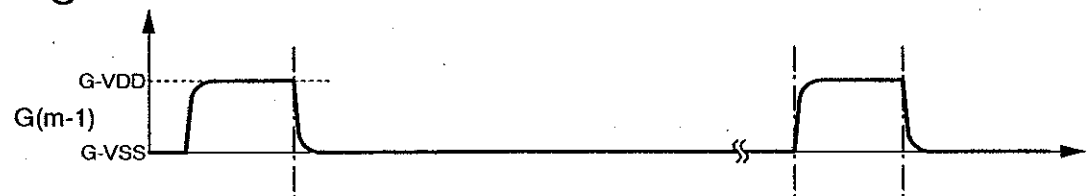


Fig. 12B

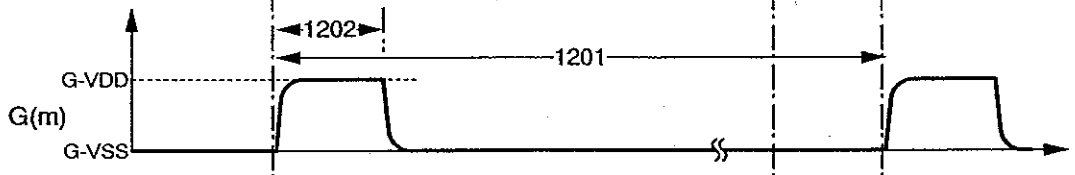


Fig. 12C

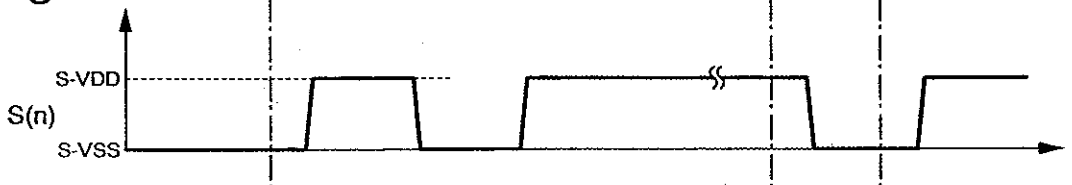


Fig. 12D

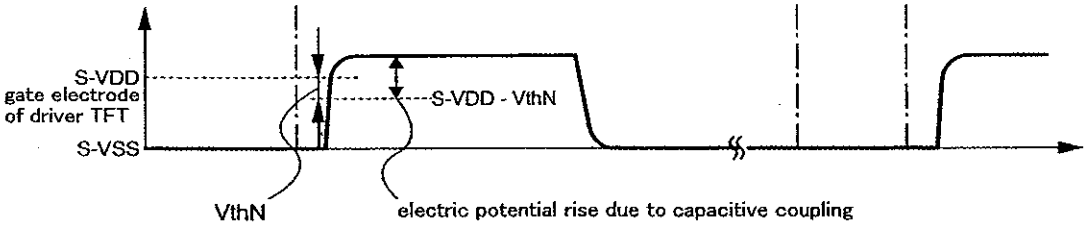
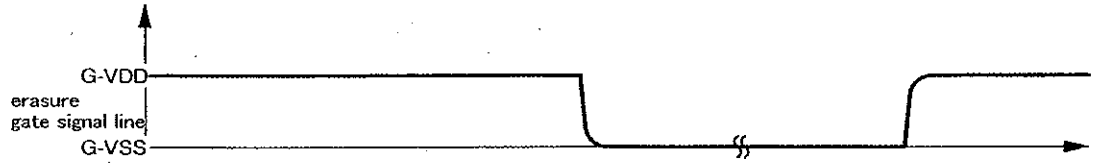


Fig. 12E



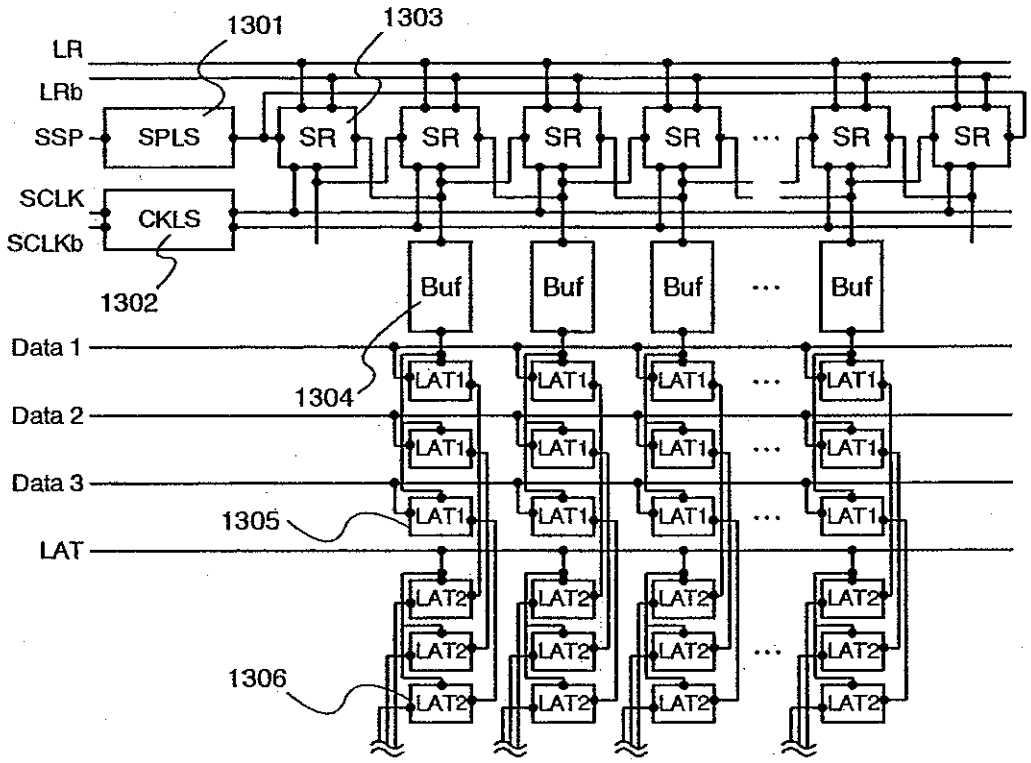

1301
1303
LR
LRb
SSP
SPLS
SR
SCLK
CKLS
SCLKb
1302
Buf
Data 1
1304
Data 2
Data 3
1305
LAT
LAT1
LAT2
1306

Fig. 13

Fig. 14A

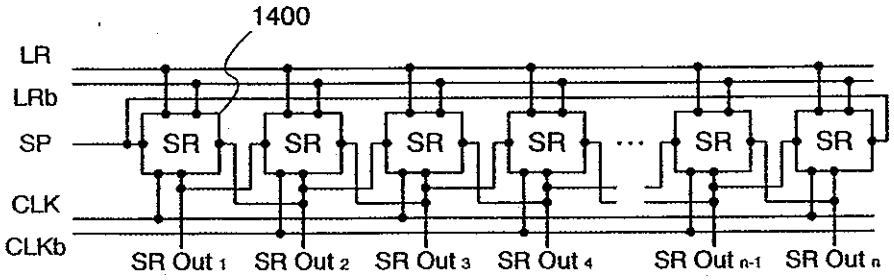
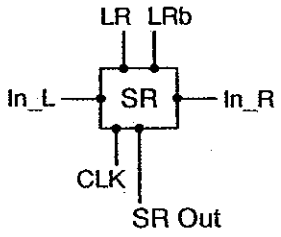
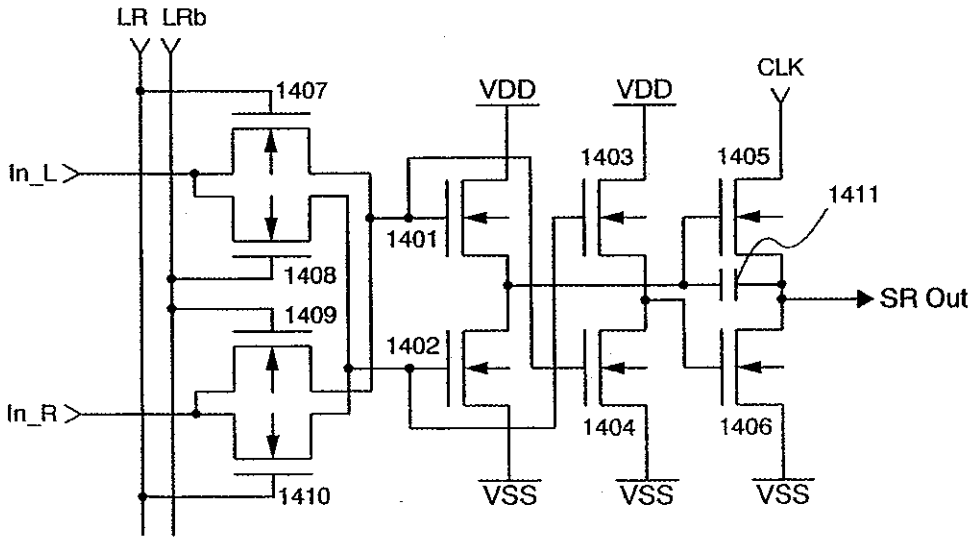


Fig. 14B





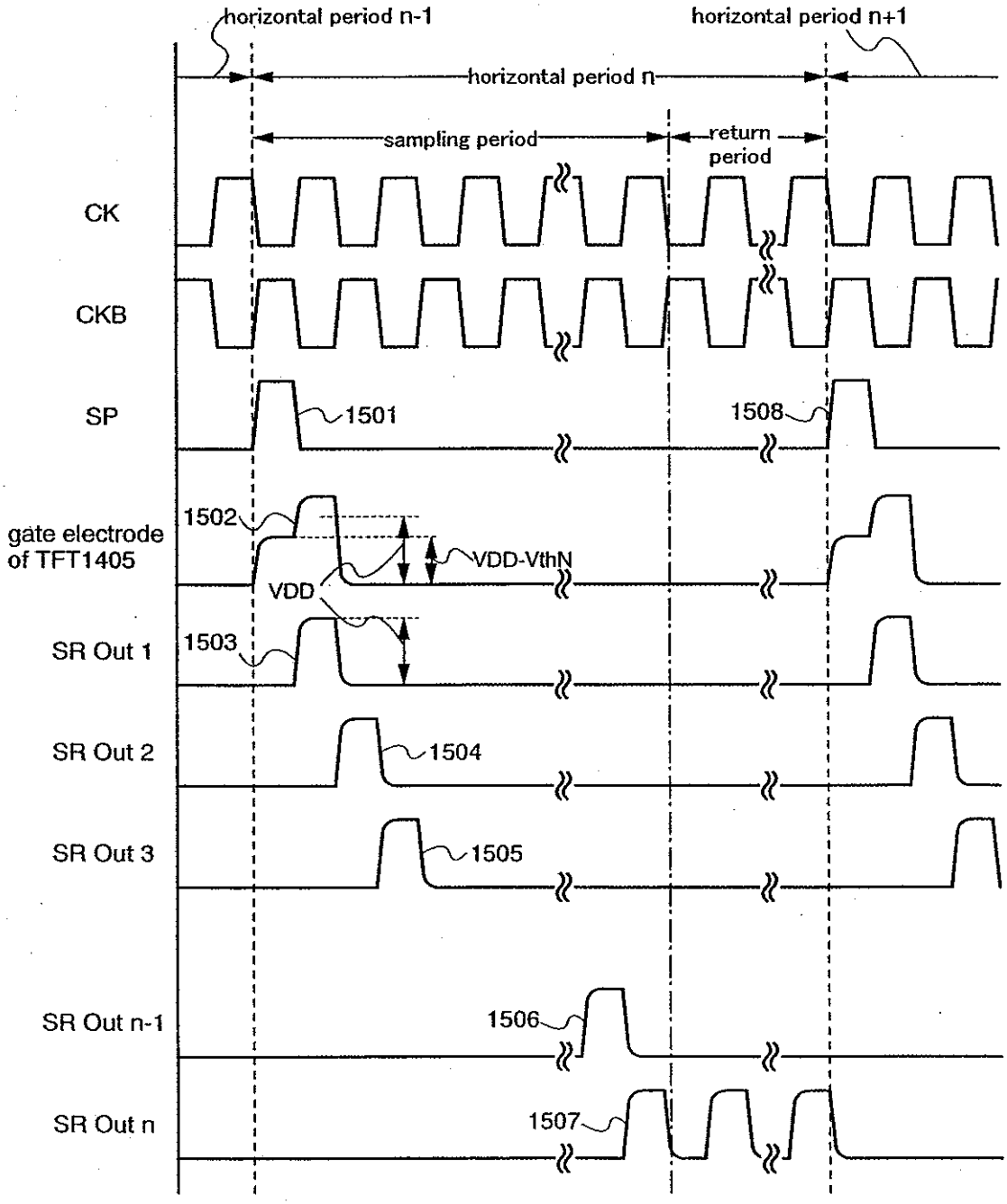

horizontal period n-1
horizontal period n
horizontal period n+1
sampling period
return period
CK
CKB
SP
1501
1508
gate electrode of TFT1405
1502
VDD-VthN
VDD
SR Out 1
1503
SR Out 2
1504
SR Out 3
1505
SR Out n-1
1506
SR Out n
1507

Fig. 15

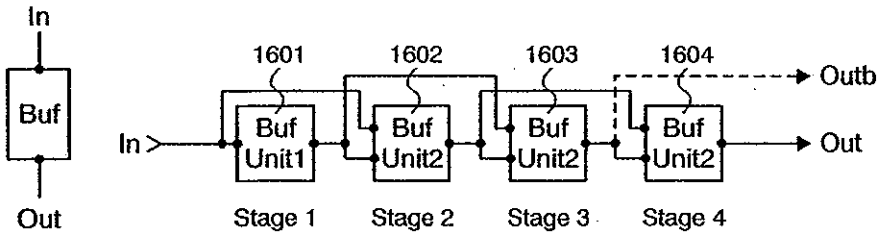


Fig. 16A

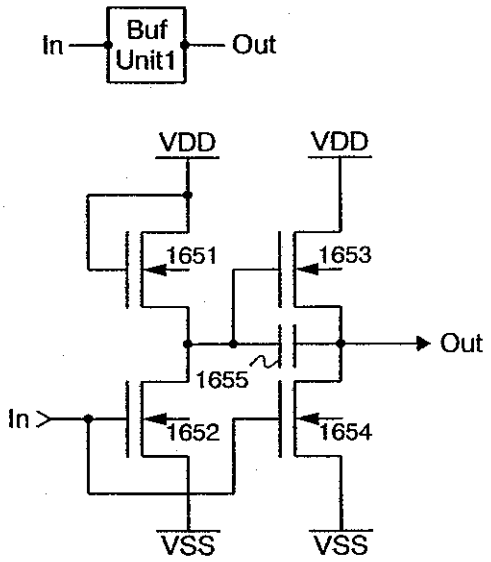


Fig. 16B

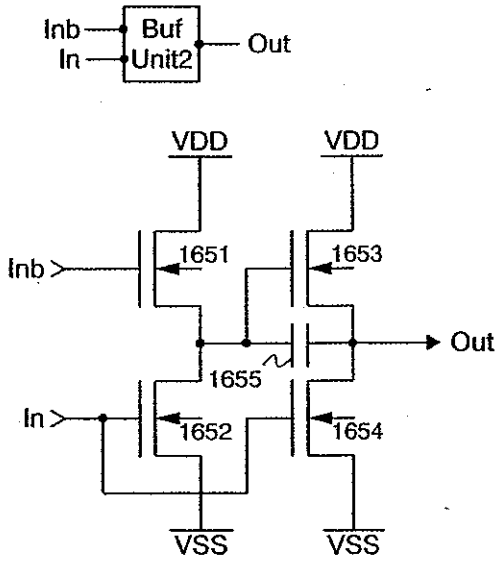


Fig. 16C

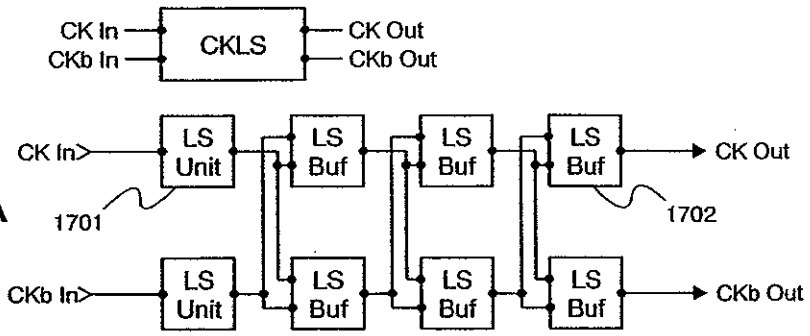


Fig. 17A

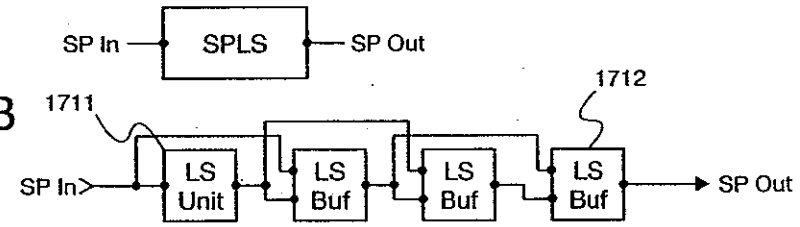


Fig. 17B

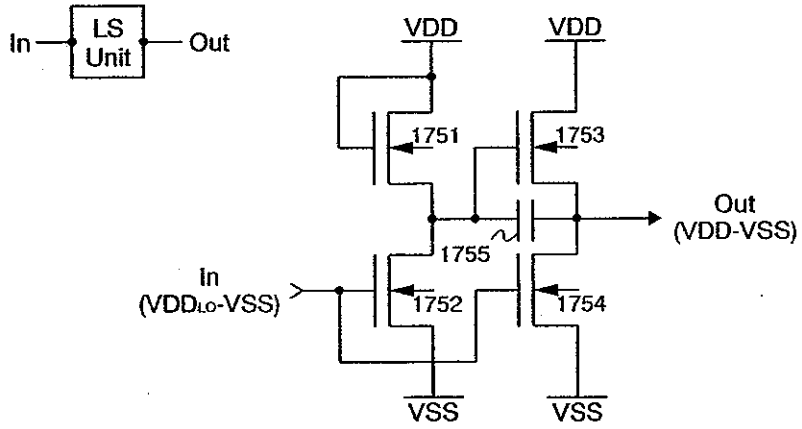


Fig. 17C

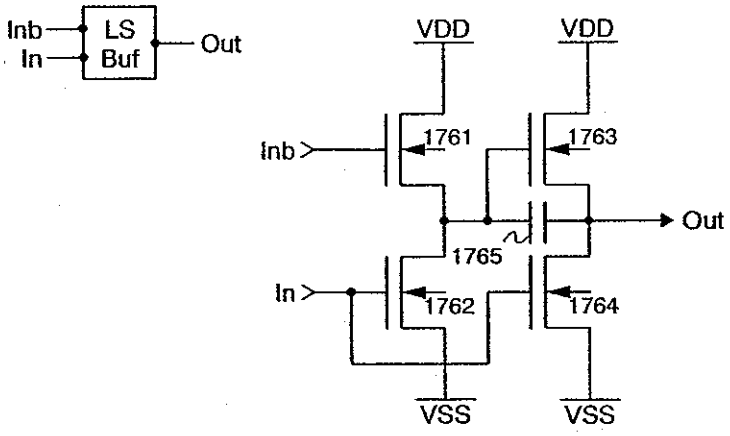


Fig. 17D

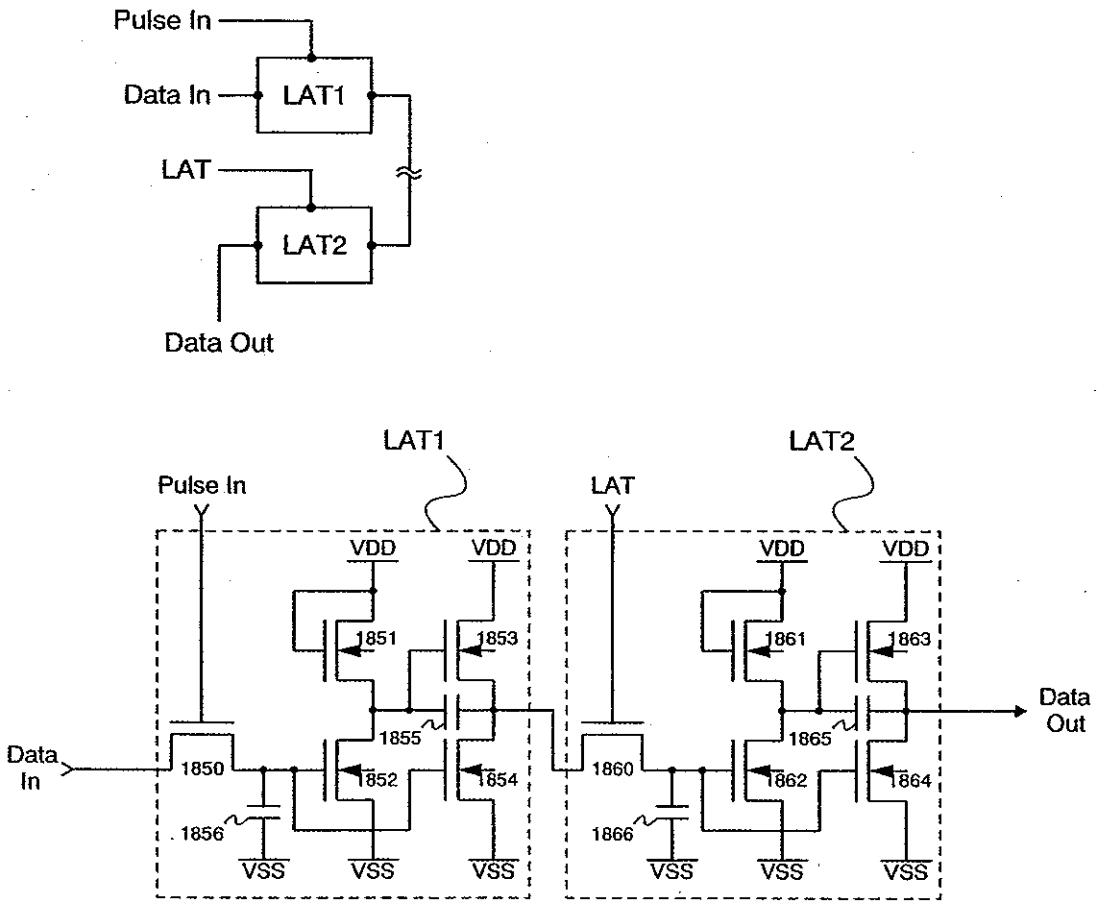

Pulse In
Data In
LAT1
LAT
LAT2
Data Out
LAT1
LAT2
Pulse In
LAT
VDD
VDD
VDD
VDD
1851
1853
1861
1863
1855
1865
Data
In
1850
1852
1854
1860
1862
1864
Data
Out
1856
1866
VSS
VSS
VSS
VSS
VSS
VSS

Fig. 18

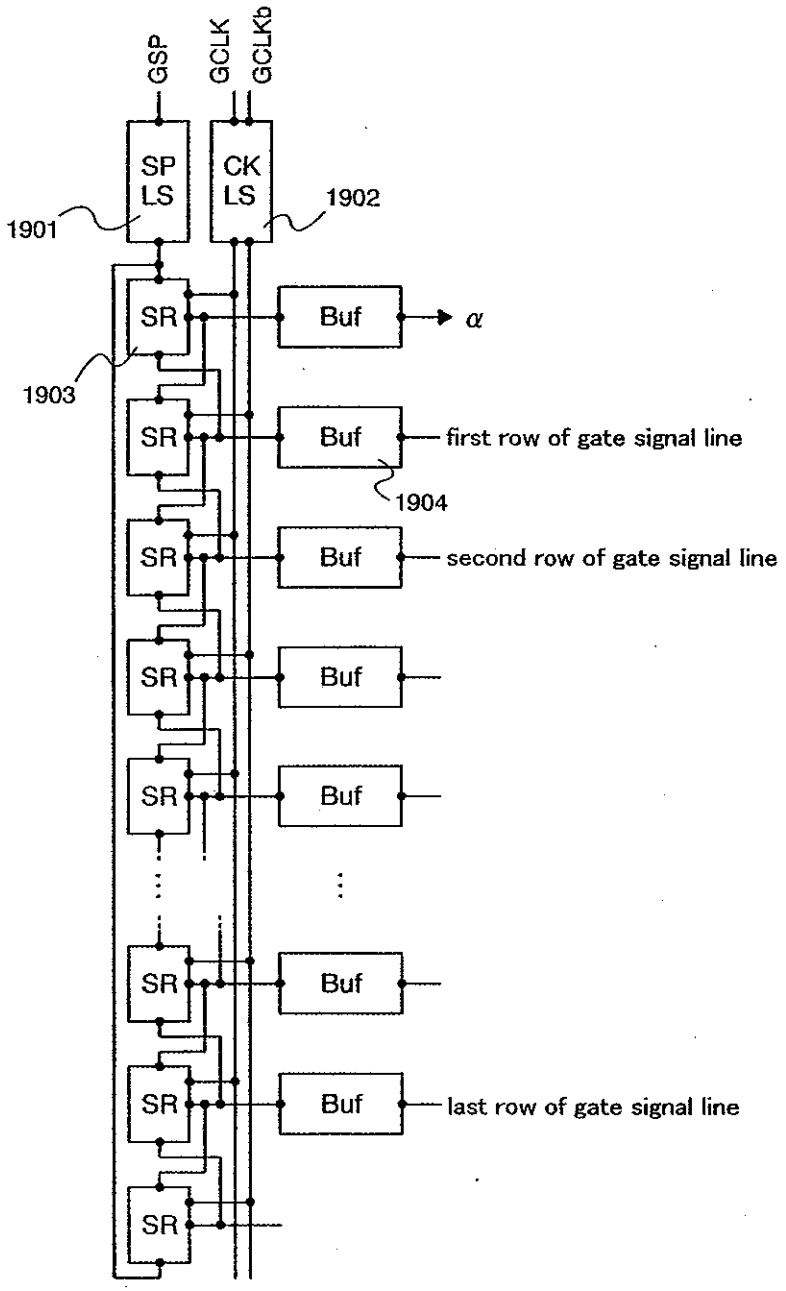

GSP
GCLK
GCLKb
SP LS
CK LS
1901
1902
1903
1904
SR
Buf
α
first row of gate signal line
second row of gate signal line
last row of gate signal line

Fig. 19

Fig. 20A

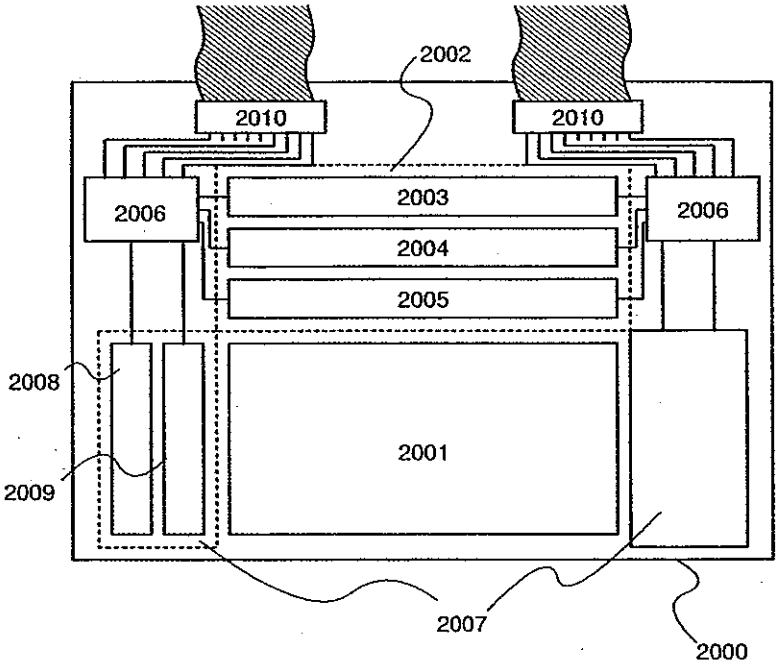


Fig. 20B

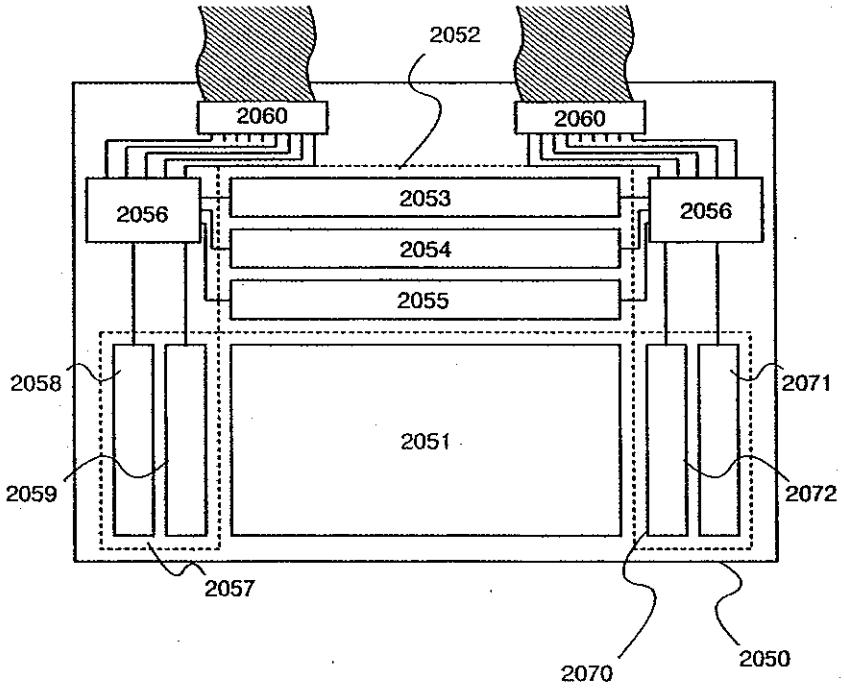


Fig. 21A

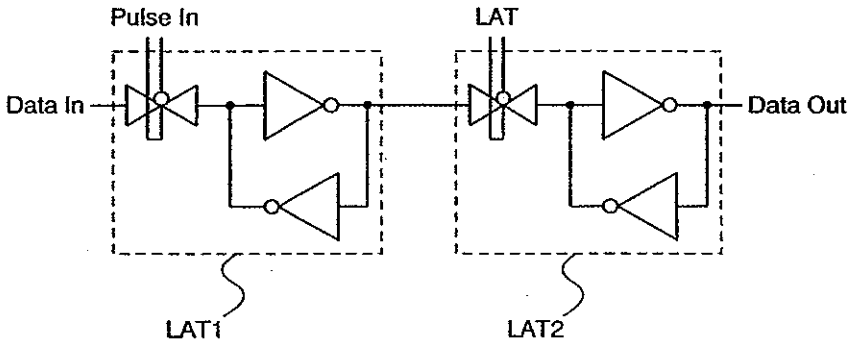


Fig. 21B

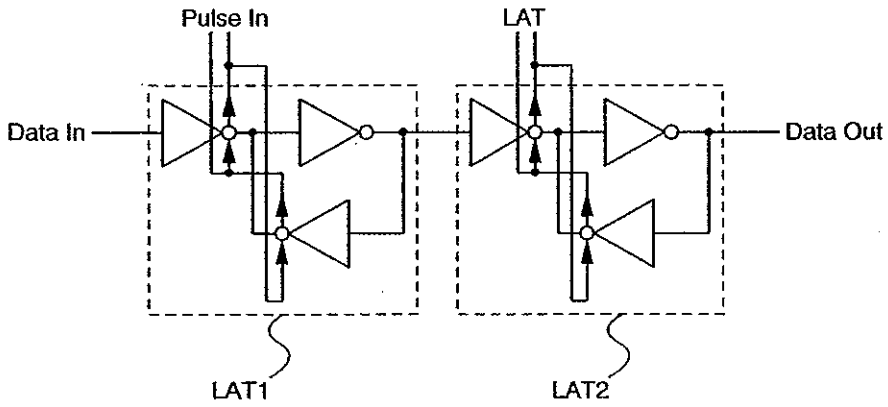


Fig. 21C

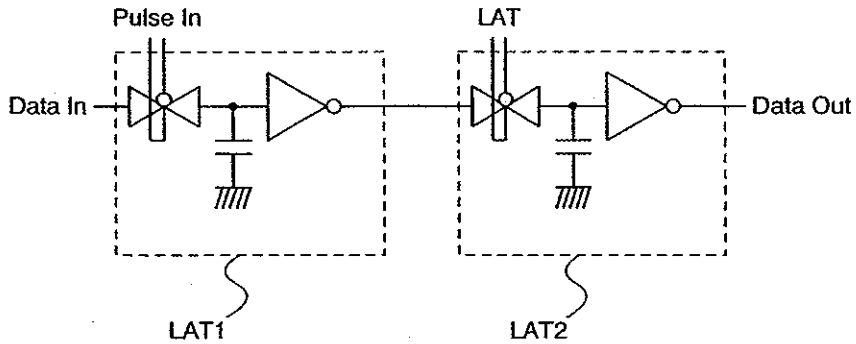


Fig. 22A

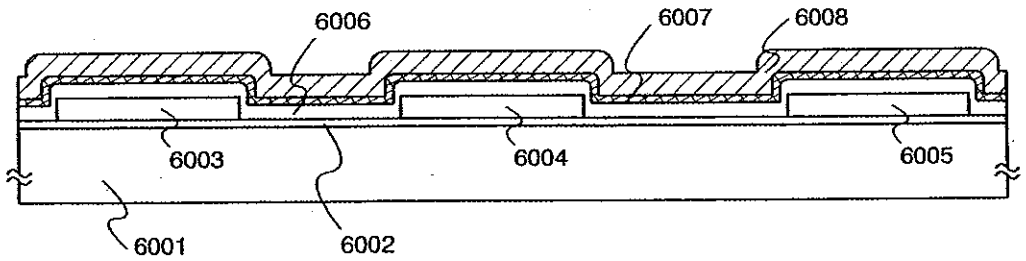


Fig. 22B

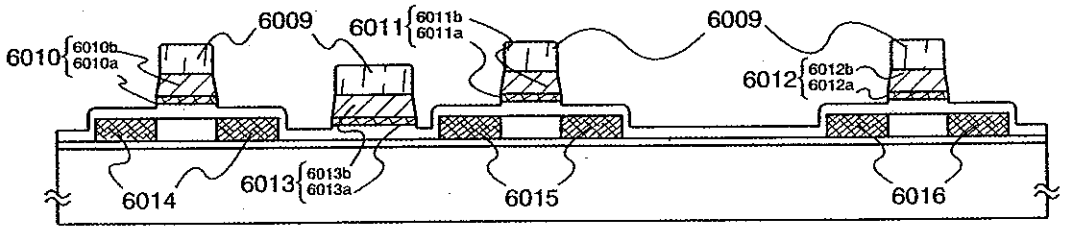
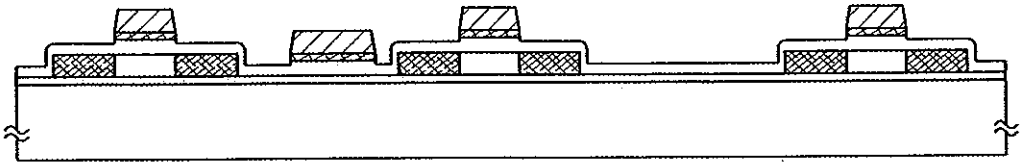


Fig. 22C



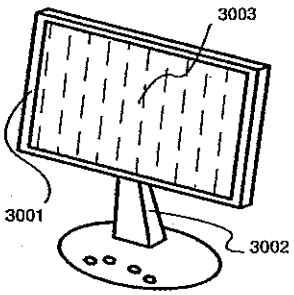


Fig. 23A

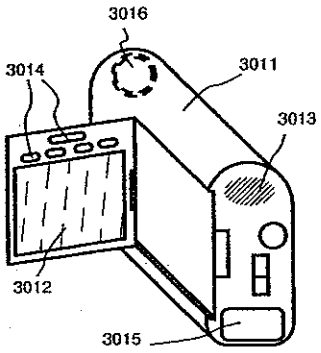


Fig. 23B

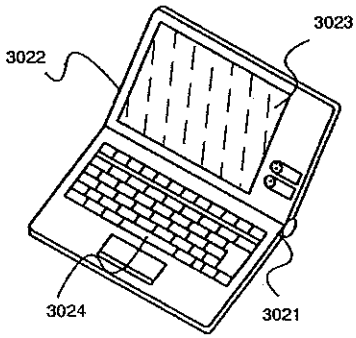


Fig. 23C

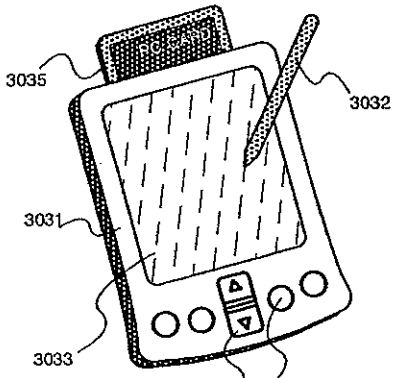


Fig. 23D

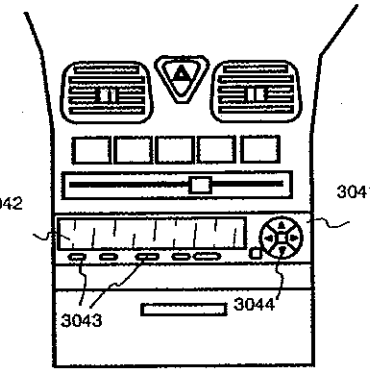


Fig. 23E

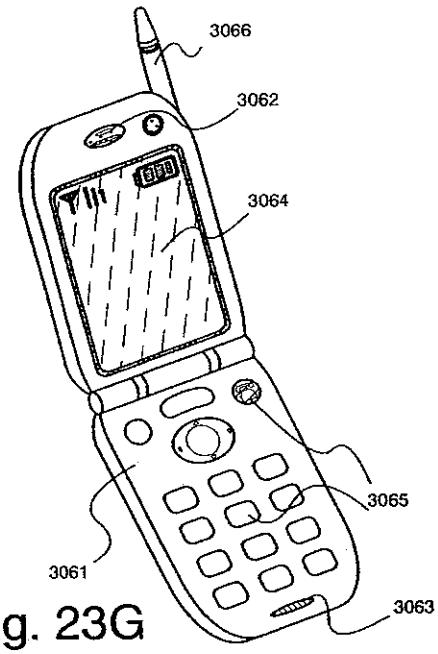


Fig. 23G

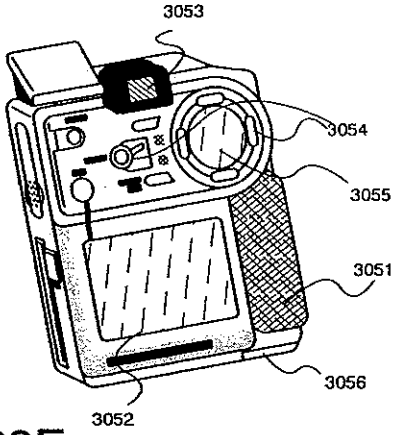


Fig. 23F

Fig. 24A

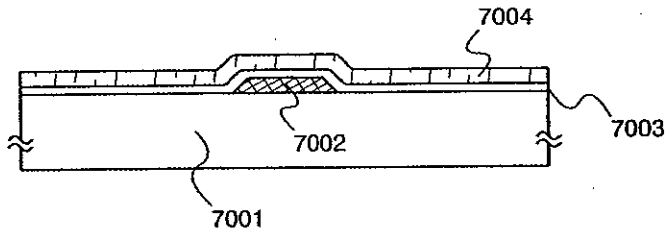


Fig. 24B

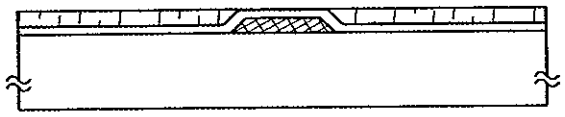


Fig. 24C

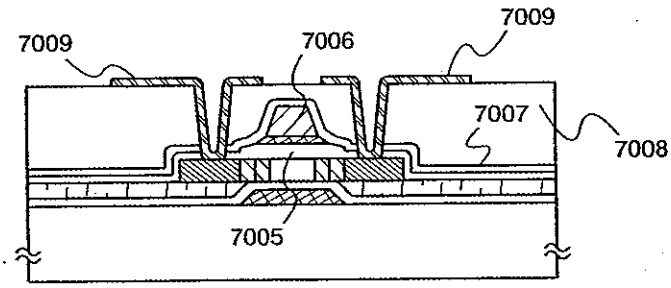


Fig. 25A

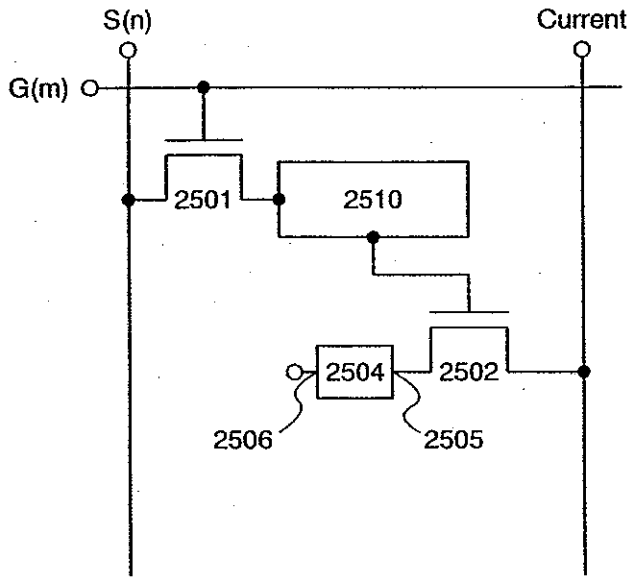
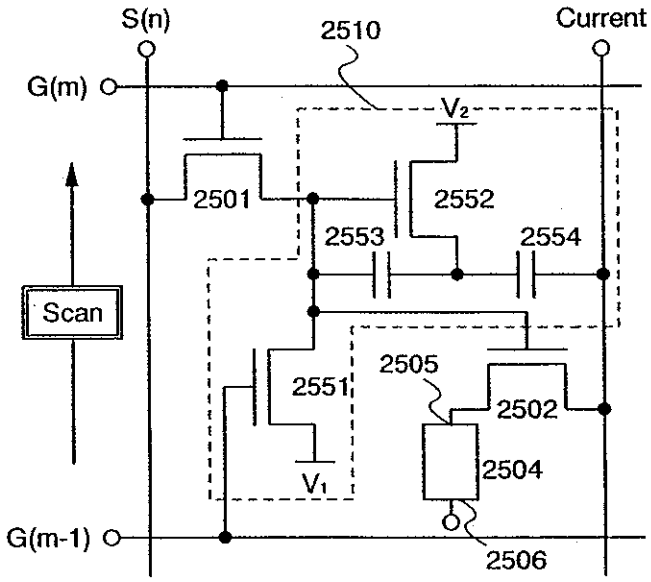


Fig. 25B



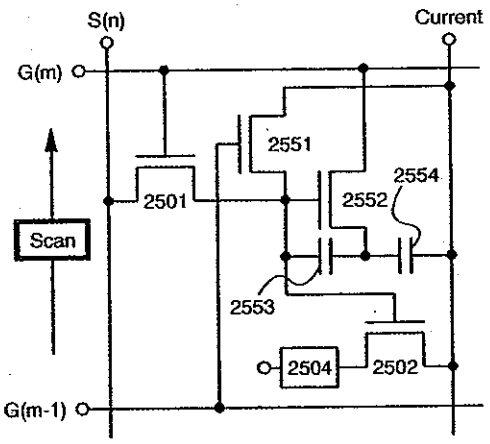


Fig. 26A

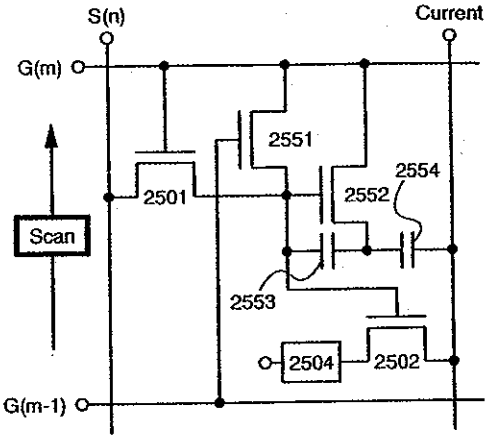


Fig. 26B

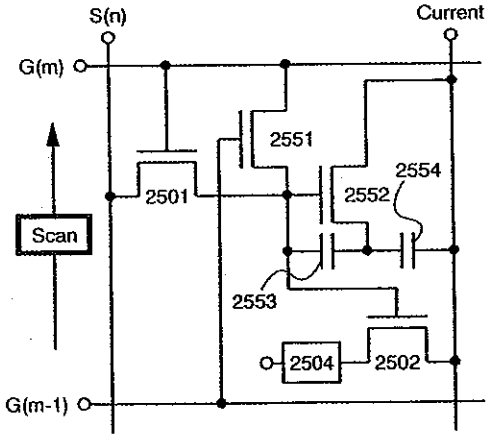


Fig. 26C