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(72) Inventors: MERRILL ROE HUNT
CHRISTOPHER ANGLOS LADAS
SAL THOMAS MASTROIANNI

(54) DOUBLE MASTER MASK PROCESS FOR INTEGRATED CIRCUIT MANUFACTURE

(71) We, MOTOROLA, INC., a corporation organized and existing under the laws of the State of Delaware, United States of America, of 1303 E. Algonquin Road, Schaumburg, Illinois 60196, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:–

The present invention relates in general to the fabrication of semiconductor devices and, in particular, to self-aligned methods for manufacturing high density integrated circuits.

A recent advance in fabricating high density integrated circuits is the use of self-aligning techniques. These techniques use selectively etchable thin layers with openings in one layer forming the etching mask for openings in subsequent layers to form a given device region. In addition to the fundamental device region registration advantages offered by self-alignment, the use of multiple dielectric layers in a selective etching technique offers inherent protection against device defects caused by mask scars or pinholes. This pinhole protection derives from the fact that any pinholes in the upper dielectric layer caused by defects in the master mask will be covered by photoresists in the steps used to selectively "enable" selected groups of master mask openings in subsequent process steps.

In prior art process for fabricating transistors, multiple dielectric layers and selective etching have been used in conjunction with a single master mask to form collector contact, base contact and emitter regions which are self-aligned with respect to each other. These processes require preliminary masking steps to provide the required registration of isolation and buried layer regions, base and isolation regions and when required, the registration of a deep collector contact within the isolation region. With the advent of higher density integrated circuits and, in particular, with large memory and microprocessor integrated circuits having a large number of closely spaced devices, the registration of base and isolation regions becomes extremely critical. The yields of these type integrated circuits manufactured using prior art processes have suffered because this registration problem is not addressed. The yields of large, high density integrated circuits manufactured using prior art processes are also adversely affected by the fact that the pinhole protection inherent in self-alignment techniques is unavailable to preliminary masking steps and by the fact that the sequence of selective diffusion and reoxidation process steps required by a single master mask create additional dielectric layer transitions or "steps" across the upper surface of the integrated circuit. The loss of planarity associated with these "steps" makes it difficult to obtain reliable interconnecting metal patterns, especially in multilevel metallization systems.

According to one aspect of the present invention there is provided a self-aligned method for manufacturing integrated circuits including the steps of providing a semiconductor substrate having a surface of a first conductivity type, forming a first masking means over said surface, forming a second masking means over said first masking means, said second masking means exhibiting a slow etch rate in an etchant for said first masking means, forming a predetermined pattern of openings in said second masking means, etching open-

ings in said first masking means through some but not all of said openings in said second masking means, forming a first set of doped regions by selectively applying impurities of a second conductivity type opposite said first conductivity type through said openings in said first masking means, etching openings in said first masking means through the remainder of said openings in said second masking means, forming a second set of doped regions by applying impurities of said second conductivity type through all of said openings, removing said first and said second masking means from said surface, forming a third masking means over said surface and said doped regions, said third masking means having a second predetermined pattern of openings formed therein, forminv a third set of doped regions by selectively applying impurities of said first conductivity type through some but not all of said openings of said second predetermined pattern of openings and applying contact means to said doped regions through said second predetermined pattern of openings.

According to a further aspect of the invention there is provided a self-aligned method of manufacturing a semiconductor device comprising the steps of providing a semiconductor substrate having a surface of a first conductivity type, forming a first masking layer over said surface, depositing a second masking layer on said first masking layer, forming a predetermined pattern of openings in said second masking layer, said predetermined pattern comprising a first and a second group of openings, forming a first group of semiconductor device regions by applying impurities through openings etched in said first masking layer using said first group of openings as an etching mask, forming a second group of semiconductor device regions by applying impurities through openings etched in said first masking layer using said second group of openings as an etching mask, removing said first and second masking layers, forming u third masking layer over said surface, depositing a fourth masking layer over said third masking layer, forming a predetermined pattern of openings in said fourth masking layer, said predetermined pattern of openings comprising a third and a fourth group of openings, forming a third group of semiconductor device regions by applying impurities through openings etched in said third masking layer using said third group of openings as an etching mask and forming a group of contact openings in said third masking layer using said fourth group of openings as an etching mask.

The invention will now be described by way of example only with particular reference to the accompanying drawings wherein:

Figures 1 to 9 show a cross-sectional views of a semiconductor substrate at various stages of the manufacturing method of the present invention.

The self-aligned method of integrated circuit fabrication of the present invention will now be described in terms of ths detailed fabrication steps used to manufacture the preferred embodiment together with the attached figures which show the structure of the integrated circuit devices being fabricated at various stages in the process. To simplify the discussion, conventional process steps will be described only briefly, while those steps relating to the novel aspects of the process will be described in greater detail.

Initially, as shown in Figure 1 and using conventional techniques, N+ buried layers 10 and 12 are formed in a P-type semiconductor body 14 by diffusing an arsenic impurity into the semiconductor body 1 . and thereafter growing a thin N-type expitaxial silicon layer 16 (typically 0.3 ohm-centimeter resistivity, 3 microns thick) to obtain the resulting substrate 18. The surface of substrate 18 is then coated with approximately 2,500 °A of thermally grown silicon dioxide to form layer 20 and then a silicon nitride layer 22 approximately 1,500 °A thick is deposited over the surface of layer 20. This procedure provides selectively etchable layers over the surface of substrate 18 which will be used in subsequent process steps.

In the steps of Figure 2, a single photomask and conventional photoresist and etching techniques are used to form in a single step a predetermined pattern of openings which are later employed for forming device regions. Opening 24 defines a base region, openings 26 and 28 define resistor preohmic contact regions and openings 30, 32 and 34 define isolation regions. Openings 30 and 32 are two portions of the same annular ring isolation region delineating the collector of a transistor. Because the openings in layer 22 have been formed using a single photomask in a single step, layer 22 provides a first master masking layer which allows the fabrication of device regions which are self aligned with respect to each other as will be evident by the subsequent process steps of the invention.

In the steps of Figure 3, conventional photoresist techniques an and "oversize" photomask, which has noncritical alignment, are used such that the surface of silicon dioxide layer 20 is exposed in isolation openings 30, 32 and 34 while the remaining openings in layer 22 remain covered with photoresist. This procedure allows the selective etching of the silicon dioxide such that the silicon surface of substrate 18 is exposed only at those locations where an isolation diffusion is to be performed. Using conventional techniques, a P-type impurity is now diffused through openings 30, 32 and 34 to form isolation regions 36, 38 and 30 which extend downward to contact P-type semiconductor body 14. Simultaneous with the

diffusion cycle used to form isolation regions 36, 38 and 40, a re-oxidation cycle forms silicon dioxide regions 42, 4 and 46 which reestablishes the silicon dioxide layer over the surface of silicon epitaxial layer 16. Regions 42, 44 and 46 prevent undercutting of silicon dioxide layer 20 during the subsequent "base washout" etching step described below. The re-oxidation cycle also resulhs in the growth of a small amount of additional silicon dioxide over the surface of silicon dioxide layer 20 in base opening 24 and resistor preohmic openings 26 and 28 as illustrated by regions 43, 45 and 47 in Figure 3.

In the process steps of Figure 4, a maskless etch is used such that the silicon dioxide regions underlying openings 24, 26, 28, 30, 32 and 34 of silicon nitride layer 22 are all removed to expose the surface of epitaxial layer 16. A base predeposition is then applied in all openings using a boron doped oxide which is deposited in a furnace tube at about 900°C such that the dopant enters the surface of epitaxial silicon layer 16 to a depth of approximately 1000 Å thereby creating regions 48, 50, 52, 54, 56 and 58. This process step wherein the base region of a device is formed by a "base washout" process which does not require a photoresist or masking step provides a key advantage in the process of the present invention.

In the process steps of Figure 5, the boron doped predeposition of oxide of process step 4, the silicon nitride layer 22 and the silicon dioxide layer 20 are completely removed from the surface of substrate 18. The removal of silicon nitride layer 22 and silicon dioxide layer 20 thus removes the first master mask layec which was used to define device regions in the previous process steps. Substrate 18 is then placed in a base diffusion furnace at a temperature of from 900°C to 1050°C causing the boron doped surface regions 48, 50, 52, 54, 56 and 58 (Fig. 4) to diffuse downward into silicon epitaxial layer 16. The prior base predeposition cycle and the base diffusion cycle are designed to produce a base region 60 having a thickness of approximately one micron and having the required resistivity simultaneously with the growth of a silicon dioxide layer 62 approximately 2000Å thick. Silicon dioxide layer 62 and ths subsequently deposited silicon nitride layer 64 (approximately 200 Å thick) form the composite layers required for the second master masking steps of the remainder of the process. An advantageous feature of the present invention is the process simplicity which results from designing the base diffusion cycle such that the formation of base region 60 having the required thickness and resistivity can occur simultaneous with the formation of silicon dioxide layer 62. Because of the "base washout" process steps previously discussed in conjunction with Figure 4, the base diffusion cycle causes the formation of diffused resistor contact regions 66 and 68 and diffused overlay regions 70, 72 and 74. Resistor contact regions 66 and 68 provide regions of high dopant concentration required for good ohmic contact to the resistor which will subsequently be formed between them. The diffused overlay regions 70, 72 and 74 associated respectively to previously formed isolation regions 35, 38 and 40 are not required but are simply a non-detrimental effect resulting from the use of the much simpler "base washout" process step previously described for Figure 4.

The process steps of Figure 6 illustrate the formation of a high value resistor using ion implantation. A photoresist layer 76 is applied over the surface of substrate 18, a resistor photomask is applied and exposed and the photoresist layer developed to form opening 78 which defines a region connecting previously diffused resistor contact regions 66 and 68. A source of high energy ions is now applied. Photoresist layer 76 inhibits the passage of these ions except through opening 78 where ions pass through silicon nitride layer 64 and silicon dioxide layer 62 to form a thin boron doped layer at the surface of epitaxial silicon layer 16. A key feature of this process step is the fact that although a photoresist step is required, the ion implantation is done through the oxide-nitride composite layer and thus no etching step is required to dope the silicon surface to provide for the formation of a resistor. It is also important to notice that the high resistance ion implanted resistor region 80 is very thin at this process step (less than 1000Å). The final depth of the resistor region will be formed in the later emitter diffusion process step discussed below.

In the process step of Figure 7, using conventional photoresist and nitride etch techniques, a photomask is used to create a second set of master mask openings. These include collector contact opening 82, base contact opening 84, emitter opening 86 and resistor contact openings 88 anf 90. Next, the upper surfaces are once again coated with photoresist and an oversized photomask is used so that only collector contact opening 82 and emitter contact opening 86 are exposed and an oxide etch can be used to selectively remove only portions of silicon dioxide layer 62 underlying these openings. The photoresist layer is removed and substrate 18 is placed in the diffusion furnace where an emitter diffusion cycle is used to form emitter region 92 which is about .7 microns deep and simultaneously to form collector contact 94. During the emitter diffusion cycle, the thin boron doped resistor region 80 previously formed by ion implantation is "annealed" such that the boron dopant diffuses downward to form a resistor region 96 which is approximately 5000Å thick. The emitter diffusion cycle of this process step includes incidental reoxidation whereby relatively thin

silicon dioxide layers 98 and 100, (approximately 200Å thick) are grown over the tope of emitter region 98 and collector contact region .4 simultaneous with the diffusion. These oxide layers will subsequently be etched away in the "washout" emitter process used to form the emitter contact prior to metallization, as described below.

In the process steps of Figure 8, photoresist and an oversized photomask are used to expose base contact opening 84 and resistor preohmic contact openings 88 and 90 of an oxide etch is used to selectively etch the portions of silicon dioxide layer 62 underlying these openings. After the photoresist is stripped away, an emitter "washout" process is used to etch away the thin silicon dioxide layers 98 and 100. Collector, base, emitter, and resistor contact regions are thus all cleared of oxide and ready for metal contact as formed in subsequent metallization process steps.

Figure 9 illustrates one particular metallization system that can be advantageously used with the process of the present invention. To form this metallization system, a layer of platinum is deposited over the surface of substrate 18 and into the silicon contact openings which have been cut through silicon dioxide layer 62 and silicon nitride layer 64 by the process previously described. The deposition of platinum is followed by a heat treatment at 400°C to 650°C causing silicon to migrate into the overlying platinum layer to form a platinum silicide region 102 in each of the contact openings. The platinum layer is stripped away and the substrate is returned to a metal deposition system where a layer of refractory metal 104 which may be tungsten, titanium, molybdenum or suitable alloys thereof, and an additional layer of aluminum 106 are deposited. Using conventional photoresist and metal etch techniques, a metal photomask is used to delineate a metal interconnection pattern.

The metallization system of Figure 9 is particularly useful because the formation of platinum silicide regions in all contact openings in conjunction with a barrier metal region of refractory metal effectively seals the substrate surface against the effects of further processing. If a processing problem occurs from this point on, the surface of the substrate can be completely stripped back, leaving the tungsten or titanium and silicon nitride surfaces uneffected. This is possible because the etchants used for subsequent photoresist applications are phosphoric acid or hydrofluoric acid based etchants which have little effect on the refractory metal barrier or on the silicon nitride. This rework capability is particularly useful in complex integrated circuit applications and in particular in integrated circuits which makes us of multiple level metal interconnections.

The process sequence of Figures 1–9 described above illustrates a particular embodiment of the present invention which combines the self-alignment and pinhole protection advantages of a first and a second master mask, the process simplification of "base washout" and the inherent doping level control of ion implantation. The process thus allows the fabrication of complex integrated circuit structure having high value resistors with closely controlled tolerances. The process allows fabrication of load resistors with resistivities as high as several thousand ohms per square and tolerances as small as ±5%. In memory integrated circuits, high value resistors with closely controlled tolerances allow the design of memory cells requiring a much smaller layout area on the chip. The inherent yield advantages resulting from the present invention process combined with its high value resistor capability thus allow the manufacture of larger memories requiring less total chip area and which are thus cheaper to manufacture.

In addition to the particular embodiment of the present invention illustrated above for high value resistors, alternative embodiments for low value resistors are also possible. In one embodiment, useful for resistor structures requiring resistivities in the range 300 ohms per square to 700 ohms per square, the process sequence above is modified by opening resistor regions during the "base washout" portion of the process. Diffused resistor regions of the required resistivity are then formed simultaneously with the diffusion of the deeper base regions. In a further embodiment, a shallower base enhancement diffusion overlays the deeper base diffusion to further lower resistivity. A feature of this embodiment of the invention is the fact thah since the resistor junctions are formed using a base diffusion, they have a lower grade constant which tends to reduce capacitance.

A convenient summarization of the advantages of the present invention which derive from the use of a first master mask (1st MM) and a second master mask (2nd MM) is provided by Table I which compares the mask alignment steps of a conventional process to those required by the process of the present invention. As shown in the Table, the total number of critical alignments required has been reduced by 50% and one alignment has been eliminated through the use of the "base washout" process step.

TABLE I

COMPARISON OF ALIGNMENT STEPS

CONVENTIONAL		SELF–ALIGNED	
ALIGNMENT	NATURE OF ALIGNMENT: CRITICAL=(C) NONCRITICAL =(NC)	ALIGNMENT	NATURE OF ALIGNMENT: CRITICAL=(C) NONCRITICAL =(NC)
ISOLATION–BURIED LAYER	C	1ST MASTER MASK TO BURIED LAYER	C
ISOLATION OVERSIZE TO ISOLATION	NC	ISOLATION OVERSIZE TO 1ST MM	NC
BASE TO ISOLATION	C	BASE WASHOUT ELIMINATES BASE OVERSIZE TO 1ST MM	
RESISTOR TO BASE	C	RESISTOR TO 1ST MM	C
EMITTER TO BASE	C	2ND MM TO 1ST MM	C
PREOHMIC TO BASE	C	EMITTER OVERSIZE TO 2ND MM	NC
OVERSIZE PREOHMIC TO PREOHMIC	NC	PREOHMIC OVERSIZE TO 2ND MM	NC
METAL TO PREOHMIC EMITTER	C	METAL TO 2ND MM	C
TOTAL 6 CRITICAL ALIGNMENTS AND 2 NONCRITICAL ALIGNMENTS		TOTAL 4 CRITICAL ALIGNMENTS AND 3 NONCRITICAL ALIGNMENTS	

WHAT WE CLAIM IS:–

1. A self-aligned method for manufacturing integrated circuits including the steps of providing a semiconductor substrate having a surface of a first conductivity type, forming a first masking means over said surface, forming a second masking means over said first masking means, said second masking means exhibiting a slow etch rate in an etchant for said first masking means, forming a predetermined pattern of openings in said second masking means, etching openings in said first masking means through some but not all of said openings in said second masking means, forming a first set of doped regions by selectively applying impurities of a second conductivity type opposite said first conductivity type through said openings in said first masking means, etching openings in said first masking means through the remainder of said openings in said second masking means, forming a second set of doped regions by applying impurities of said second conductivity type through all of said openings, removing said first and said second masking means from said surface, forming a third masking means over said surface and said doped regions, said third masking means having a second predetermined pattern of openings formed therein, forming a third set of doped regions by selectively applying impurities of said first conductivity type through some but not all of said openings of said second predetermined pattern of openings and applying contact means to said doped regios through said second predetermined pattern of openings.

2. A self-aligned method as claimed in Claim 1 wherein said semiconductor substrate

* C L M S *

(11)

TABLE I

COMPARISON OF ALIGNMENT STEPS

CONVENTIONAL		SELF–ALIGNED	
ALIGNMENT	NATURE OF ALIGNMENT: CRITICAL=(C) NONCRITICAL =(NC)	ALIGNMENT	NATURE OF ALIGNMENT: CRITICAL=(C) NONCRITICAL =(NC)
ISOLATION–BURIED LAYER	C	1ST MASTER MASK TO BURIED LAYER	C
ISOLATION OVERSIZE TO ISOLATION	NC	ISOLATION OVERSIZE TO 1ST MM	NC
BASE TO ISOLATION	C	BASE WASHOUT ELIMINATES BASE OVERSIZE TO 1ST MM	
RESISTOR TO BASE	C	RESISTOR TO 1ST MM	C
EMITTER TO BASE	C	2ND MM TO 1ST MM	C
PREOHMIC TO BASE	C	EMITTER OVERSIZE TO 2ND MM	NC
OVERSIZE PREOHMIC TO PREOHMIC	NC	PREOHMIC OVERSIZE TO 2ND MM	NC
METAL TO PREOHMIC EMITTER	C	METAL TO 2ND MM	C
TOTAL 6 CRITICAL ALIGNMENTS AND 2 NONCRITICAL ALIGNMENTS		TOTAL 4 CRITICAL ALIGNMENTS AND 3 NONCRITICAL ALIGNMENTS	

WHAT WE CLAIM IS:–

1. A self-aligned method for manufacturing integrated circuits including the steps of providing a semiconductor substrate having a surface of a first conductivity type, forming a first masking means over said surface, forming a second masking means over said first masking means, said second masking means exhibiting a slow etch rate in an etchant for said first masking means, forming a predetermined pattern of openings in said second masking means, etching openings in said first masking means through some but not all of said openings in said second masking means, forming a first set of doped regions by selectively applying impurities of a second conductivity type opposite said first conductivity type through said openings in said first masking means, etching openings in said first masking means through the remainder of said openings in said second masking means, forming a second set of doped regions by applying impurities of said second conductivity type through all of said openings, removing said first and said second masking means from said surface, forming a third masking means over said surface and said doped regions, said third masking means having a second predetermined pattern of openings formed therein, forming a third set of doped regions by selectively applying impurities of said first conductivity type through some but not all of said openings of said second predetermined pattern of openings and applying contact means to said doped regios through said second predetermined pattern of openings.

2. A self-aligned method as claimed in Claim 1 wherein said semiconductor substrate

comprises a body of said second conductivity type, a buried layer of said first conductivity type and an epitaxial layer having a surface of said first conductivity type.

3. A self-aligned method as claimed in Claim 1 comprising the further step of forming an additional doped region by applying impurities through portions of said third masking means not constituted by said second predetermined pattern of openings.

4. A self-aligned method of manufacturing a semiconductor device comprising the steps of providing a semiconductor substrate having a surface of a first conductivity type, forming a first masking layer over said surface, depositing a second masking layer on said first masking layer, forming a predetermined pattern of openings in said second masking layer, said predetermined pattern comprising a first and a second group of openings, forming a first group of semiconductor device regions by applying impurities through openings ethced in said first masking layer using said first group of openings as an etching mask, forming a second group of semiconductor device regions by applying impurities through openings etched in said first masking layer using said second group of openings as an etching mask, removing said first and second masking layers, forming a third masking layer over said surface, depositing a fourth masking layer over said third masking layer, forming a predetermined pattern of openings in said fourth masking layer, said predetermined pattern of openings comprising a third and a fourth group of openings, forming a third group of semiconductor device regions by applying impurities through openings etched in said third masking layer using said third group of openings as an etching mask and forming a group of contact openings in said third masking layer using said fourth vroup of openings as an etching mask.

5. A self-aligned method as claimed in Claim 4 wherein said step of forming said group of contact openings contacts said first, second and third group of semiconductor device regions.

6. A self-aligned method as claimed in Claim 4 wherein said first and second groups of semiconductor device regions are of the same conductivity type.

7. A self-aligned method as claimed in Claim 6 wherein said third group of semiconductor device regions is of the opposite conductivity type.

8. A self-aligned method as claimed in Claim 4 wherein said step of forming a second group of semiconductor device regions includes the reopening of said first group of openings simultaneous with the etching of openings using said second group of openings as an etching mask.

9. A self-aligned method of manufacturing integrated circuits substantially as hereinbefore described and shown in the accompanying drawings.

FOR THE APPLICANTS:
F. J. CLEVELAND & COMPANY
Chartered Patent Agents
Lincoln's Inn Chambers
40–43 Chancery Lane
London, WC2A 1JQ

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