

TECHNIQUES FOR PROVIDING A SEMICONDUCTOR MEMORY DEVICE**FIELD OF THE DISCLOSURE**

The present disclosure relates generally to semiconductor
5 memory devices and, more particularly, to techniques for
providing a semiconductor memory device.

BACKGROUND OF THE DISCLOSURE

The semiconductor industry has experienced technological
10 advances that have permitted increases in density and/or
complexity of semiconductor memory devices. Also, the
technological advances have allowed decreases in power
consumption and package sizes of various types of
semiconductor memory devices. There is a continuing trend to
15 employ and/or fabricate advanced semiconductor memory devices
using techniques, materials, and devices that improve
performance, reduce leakage current, and enhance overall
scaling. Silicon-on-insulator (SOI) and bulk substrates are
examples of materials that may be used to fabricate such
20 semiconductor memory devices. Such semiconductor memory
devices may include, for example, partially depleted (PD)
devices, fully depleted (FD) devices, multiple gate devices
(e.g., double, triple gate, or surrounding gate), and Fin-FET
devices.

25 A semiconductor memory device may include a memory cell
having a memory transistor with an electrically floating gate
region wherein electrical charge may be stored. When excess

majority electrical charges carriers are stored in the electrically floating body region, the memory cell may store a logic high (e.g., binary "1" data state). When the electrical floating gate region is depleted of majority electrical charge carriers, the memory cell may store a logic low (e.g., binary "0" data state). Also, a semiconductor memory device may be fabricated on silicon-on-insulator (SOI) substrates or bulk substrates (e.g., enabling body isolation). For example, a semiconductor memory device may be fabricated as a three-dimensional (3-D) device (e.g., a multiple gate device, a Fin-FET device, and a vertical pillar device).

In one conventional technique, the memory cell of the semiconductor memory device may be manufactured with many problems. For example, the conventional semiconductor memory device may have a channel length that may be susceptible to short-channel effects (SCE). Also, the conventional semiconductor memory device may experience interference between floating gates of adjacent memory cells. Further, the conventional semiconductor memory device may experience leakage of charge carriers stored in the memory cell due to memory cell noises and variations.

In view of the foregoing, it may be understood that there may be significant problems and shortcomings associated with conventional techniques for providing a semiconductor memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to facilitate a fuller understanding of the present disclosure, reference is now made to the accompanying drawings, in which like elements are referenced with like numerals. These drawings should not be construed as limiting the present disclosure, but are intended to be illustrative only.

Figure 1 shows a block diagram of a semiconductor memory device including a memory cell array, data write and sense circuitry, and memory cell selection and control circuitry in accordance with an embodiment of the present disclosure.

Figure 2 shows a top view of at least a portion of the memory cell array shown in Figure 1 in accordance with an embodiment of the present disclosure.

Figure 3 shows cross-sectional views of at least a portion of the memory cell array as shown in Figure 2 in accordance with an embodiment of the present disclosure.

Figure 4 shows a schematic view of at least a portion of the memory cell array having a plurality of memory cells in accordance with an embodiment of the present disclosure.

Figure 5 shows voltage potential levels of various methods for performing a write operation and a read operation on a memory cell as shown in Figures 2-4 in accordance with an embodiment of the present disclosure.

Figure 6 shows a top view of at least a portion of the memory cell array as shown in Figure 1 in accordance with an

alternate embodiment of the present disclosure.

Figure 7 shows cross-sectional views of at least a portion of the memory cell array as shown in Figure 6 in accordance with an embodiment of the present disclosure.

5 Figure 8 shows a schematic diagram of at least a portion of the memory cell array having a plurality of memory cells in accordance with an alternate embodiment of the present disclosure.

Figure 9 shows voltage potential levels of various
10 methods for performing a write operation and a read operation on a memory cell as shown in Figures 6-8 in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

15 Referring to Figure 1, there is shown a block diagram of a semiconductor memory device 10 comprising a memory cell array 20, data write and sense circuitry 36, and memory cell selection and control circuitry 38 in accordance with an embodiment of the present disclosure. The memory cell array
20 20 may comprise a plurality of memory cells 12 each coupled to the memory cell selection and control circuitry 38 via a word line (WL) 28, and to the data write and sense circuitry 36 via a bit line (CN) 30 and a source line (EN) 32. It may be appreciated that the bit line (CN) 30 and the source line (EN)
25 32 are designations used to distinguish between two signal lines and they may be used interchangeably.

The data write and sense circuitry 36 may read data from and may write data to selected memory cells 12. In a particular embodiment, the data write and sense circuitry 36 may include a plurality of data sense amplifier circuits.

5 Each data sense amplifier circuit may receive at least one bit line (CN) 30 and a current or voltage reference signal. For example, each data sense amplifier circuit may be a cross-coupled type sense amplifier to sense a data state stored in a memory cell 12. The data write and sense circuitry 36 may
10 include at least one multiplexer that may couple to a data sense amplifier circuit to at least one bit line (CN) 30. In a particular embodiment, the multiplexer may couple a plurality of bit lines (CN) 30 to a data sense amplifier circuit.

15 Each data sense amplifier circuit may employ voltage and/or current sensing circuitry and/or techniques. In a particular embodiment, each data sense amplifier circuit may employ current sensing circuitry and/or techniques. For example, a current sense amplifier may compare current from a
20 selected memory cell 12 to a reference current (e.g., the current of one or more reference cells). From that comparison, it may be determined whether the selected memory cell 12 stores a logic high (e.g., binary "1" data state) or a logic low (e.g., binary "0" data state). It may be appreciated by
25 one having ordinary skill in the art that various types or forms of the data write and sense circuitry 36 (including one

or more sense amplifiers, using voltage or current sensing techniques, to sense a data state stored in a memory cell 12) may be employed to read data stored in the memory cells 12.

The memory cell selection and control circuitry 38 may
5 select and/or enable one or more predetermined memory cells 12 to facilitate reading data therefrom by applying control signals on one or more word lines (WL) 28. The memory cell selection and control circuitry 38 may generate such control signals from address signals, for example, row address
10 signals. Moreover, the memory cell selection and control circuitry 38 may include a word line decoder and/or driver. For example, the memory cell selection and control circuitry 38 may include one or more different control/selection techniques (and circuitry thereof) to select and/or enable one
15 or more predetermined memory cells 12. Notably, all such control/selection techniques, and circuitry thereof, whether now known or later developed, are intended to fall within the scope of the present disclosure.

In a particular embodiment, the semiconductor memory
20 device 10 may implement a two step write operation whereby all the memory cells 12 in a row of memory cells 12 may be written to a predetermined data state by first executing a "clear" or a logic low (e.g., binary "0" data state) write operation, whereby all of the memory cells 12 in the row of memory cells
25 12 are written to logic low (e.g., binary "0" data state). Thereafter, selected memory cells 12 in the row of memory

cells 12 may be selectively written to the predetermined data state (e.g., a logic high (binary "1" data state)). The semiconductor memory device 10 may also implement a one step write operation whereby selected memory cells 12 in a row of
5 memory cells 12 may be selectively written to either a logic high (e.g., binary "1" data state) or a logic low (e.g., binary "0" data state) without first implementing a "clear" operation. The semiconductor memory device 10 may employ any of the illustrative writing, preparation, holding, refresh,
10 and/or reading techniques described herein.

The memory cells 12 may comprise N-type, P-type and/or both types of transistors. Circuitry that is peripheral to the memory cell array 20 (for example, sense amplifiers or comparators, row and column address decoders, as well as line
15 drivers (not illustrated herein)) may also include P-type and/or N-type transistors. Regardless of whether P-type or N-type transistors are employed in memory cells 12 in the memory cell array 20, suitable voltage potentials (for example, positive or negative voltage potentials) for reading from the
20 memory cells 12 will be described further herein.

Referring to Figure 2, there is shown a top view of at least a portion of the memory cell array 20 shown in Figure 1 in accordance with an embodiment of the present disclosure. As illustrated in the top view, the memory cell array 20 may
25 include a plurality of memory cells 12 arranged in a matrix of rows and columns including a plurality of word lines 28 (WL),

a plurality of bit lines (CN) 30, and/or a source line plate (EN) 32. Each bit line (CN) 30 may extend in a first orientation along a first plane of the memory cell array 20. The source line plate (EN) 32 may extend in the first orientation and a second orientation along a second plane of the memory cell array 20. Each word line (WL) 28 may extend in the second orientation along a third plane of the memory cell array 20. The first plane, the second plane, and the third plane of the memory cell array 20 may be arranged in different planes parallel to each other.

The plurality of word lines (WL) 28 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material), a metal material, and/or a combination of a polycide material and a metal material. In a particular embodiment, the word lines (WL) 28 may capacitively couple a voltage potential/current source of the memory cell selection and control circuitry 38 to the memory cells 12. The word line (WL) 28 may be formed of a plurality layers. Each layer of the word line (WL) 28 may be formed of different materials having various thicknesses. In a particular embodiment, the first layer (f) of the word line (WL) 28 may be formed of a silicon material having a thickness of approximately 10 nm. The second layer (g) of the word line (WL) 28 may be formed of a metal material having a thickness of approximately 10 nm. In a particular embodiment, the first word line (WL1) 28 may implement a write logic low (e.g., binary "0" data state)

operation on the memory cell 12, while the second word line (WL2) 28 may implement a write logic high (e.g., binary "1" data state) operation. In a particular embodiment, the first word line (WL1) 28 and the second word line (WL2) 28 may be spaced apart from each other at approximately 25 nm.

The plurality of word lines (WL) 28 may be an electrically capacitively coupled to a plurality of memory cells 12 via a tunneling insulating layer 202. The tunneling insulating layer 202 may comprise a plurality of insulating or dielectric layers. In a particular embodiment, the tunneling insulating layer 202 may comprise a thermal oxide layer 202(a), a nitride layer 202(b), an oxide layer 202(c), a charge trapping nitride layer 202(d) (e.g., silicon nitride), and/or a blocking oxide layer 202(e). The plurality of insulating or dielectric layers of the tunneling insulating layer 202 may comprise of various thickness. In a particular embodiment, the thermal oxide layer 202(a) may have a thickness of approximately 1.5 nm, the nitride layer 202(b) may have a thickness of approximately 2 nm, the oxide layer 202(c) may have a thickness of approximately 2.5 nm, the charge trapping nitride layer 202(d) (e.g., silicon nitride) may have a thickness of approximately 5 nm, and/or the blocking oxide layer 202(e) may have a thickness of approximately 5 nm.

The memory cell 12 may be configured to maximize scaling of memory cells 12 in the semiconductor memory device 10. In

a particular embodiment, the memory cell 12 may be configured to have a width (i) (e.g., along the direction of the bit line (CN) 30) of approximately 40 nm. The width (i) of the memory cell 12 may be limited by floating gate to floating gate interference and inversion layer interference. The spacing (K) between contiguous row of memory cells 12 (e.g., along the direction of the word line (WL) 28) may be approximately F nm, wherein F may be the minimum space possible. The memory cell 12 may be configured to have a width (j) (e.g., along the direction of the word line (WL) 28) of approximately F nm, wherein F may be the minimum space possible.

Referring to Figure 3, there are shown cross-sectional views of at least a portion of the memory cell array 20 as shown in Figure 2 in accordance with an embodiment of the present disclosure. Figure 3 illustrates a cross-sectional view of at least a portion of the memory cell array 20 along line A-A and a cross-sectional view of at least a portion of the memory cell array 20 along line B-B. The memory cells 12 of the memory cell array 20 may be implemented in a vertical configuration having various regions. For example, the memory cell 12 may comprise a source region 320, a body region 322, and a drain region 324. The source region 320, the body region 322, and/or the drain region 324 may be disposed in a sequential contiguous relationship, and may extend vertically from a plane defined by a P- substrate 130. The source region 320 of the memory cell 12 may be coupled to the source line

(EN) 32. The body region 322 may be an electrically floating body region of the memory cell 12 configured to accumulate/store charges, and may be spaced apart from and capacitively coupled to the plurality of word lines (WL) 28 via the tunneling insulating layer 202. The drain region 324 of the memory cell 12 may be coupled to the bit line (CN) 30.

The source region 320 of the memory cell 12 may be coupled to a corresponding source line (EN) 32. In a particular embodiment, the source region 320 may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the source region 320 may be formed of a silicon material doped with phosphorous or arsenic impurities. In a particular embodiment, the source region 320 may be formed of a silicon material doped with phosphorous or arsenic having a concentration of approximately 10^{20} atoms/cm³ or above. The source region 320 may comprise a plate having continuous planar region configured above the P- substrate 130. The source region 320 may also comprise a plurality of protrusions formed on the continuous planar region of the plate. The plurality of protrusions of the source region 320 may be oriented in a column direction and/or a row direction of the memory cell array 20. The plurality of protrusions of the source region 320 may form the base of the memory cell 12.

In a particular embodiment, the source line (EN) 32 may be configured as the plate having continuous planar region of the source region 320. In a particular embodiment, the source

line (EN) 32 may be formed of an N+ doped silicon layer. In another embodiment, the source line (EN) 32 may be formed of a metal material. In other embodiments, the source line (EN) 32 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). The source line (EN) 32 may couple a predetermined voltage potential to the memory cells 12 of the memory cell array 20. For example, the source line (EN) 32 may be coupled to a plurality of memory cells 12 (e.g., a column or a row of memory cell array 20).

The body region 322 of the memory cell 12 may be capacitively coupled to a corresponding word lines (WL) 28 via the tunneling insulating layer 202. In a particular embodiment, the body region 322 may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. The body region 322 may be formed of a silicon material doped with boron impurities. In a particular embodiment, the body region 322 may be formed of a silicon material with acceptor impurities having a concentration of 10^{15} atoms/cm³. In a particular embodiment, the body region 322 may comprise a first floating gate region 14a and a second floating gate region 14b. The first floating gate region 14a and the second floating gate region 14b may accumulate/store charge carriers in order to represent a data state (e.g., a logic low (e.g., binary "0" data state) and/or a logic high (e.g., binary "1" data state)). The first floating gate region 14a and the second floating gate region 14b may be

spaced apart and capacitively coupled to the plurality of word lines (WL) 28.

The word lines (WL) 28 may be capacitively coupled the body region 322. The word lines (WL) 28 may be oriented in a row direction of the memory cell array 20 and coupled to a plurality of memory cells 12. The word lines (WL) 28 may be arranged on the sides of the memory cells 12 (e.g., memory cells 12 located on a row direction of the memory cell array 20). For example, the word lines (WL) 28 may be arranged on at least two side portions of the memory cells 12. The first word line (WL1) 28 may be arranged on a first side portion of the memory cells 12 and the second word line (WL2) 28 may be arranged on a second side portion of the memory cells 12. The first side portion and the second side portion may be opposite side portions of the memory cells 12.

The drain region 324 of the memory cell 12 may be coupled to a corresponding bit line (CN) 30. In a particular embodiment, the drain region 324 of the memory cell 12 may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the drain region 324 may be formed of a silicon material doped with phosphorous or arsenic impurities. In a particular embodiment, the drain region 324 may be formed of a silicon material doped with phosphorous or arsenic having a concentration of approximately 10^{20} atoms/cm³ or above.

The bit line (CN) 30 may be coupled to the drain region

324 of the memory cell 12. The bit line (CN) 30 may be formed of a metal material. In another embodiment, the bit line (CN) 30 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other 5 embodiments, the bit line (CN) 30 may be formed of an N+ doped silicon layer. For example, the bit line (CN) 30 may be coupled to a plurality of memory cells 12. The bit line (CN) 30 may be configured above the drain region 324.

The bit line (CN) 30 may be connected to a plurality of 10 memory cells 12 (e.g., a column of memory cells 12) via a plurality of bit line contacts 326. For example, each bit line contact 326 may correspond to a memory cell 12 along a column direction of the memory cell array 20. Each bit line contact 326 may be formed of a metal layer or a polysilicon 15 layer in order to couple a voltage potential from the bit line (CN) 30 to the drain region 324 of the memory cell 12. For example, the bit line contact 326 may be formed of tungsten, titanium, titanium nitride, polysilicon or a combination thereof. The bit line contact 326 may have a height extending 20 from the bit line (CN) 30 to the drain region 324 of the memory cell 12.

In a particular embodiment, the P- substrate 130 may be made of a semiconductor material (e.g., silicon) comprising acceptor impurities and may form a base of the memory cell 25 array 20. For example, the P- substrate 130 may be made of a semiconductor material comprising boron impurities. In a

particular embodiment, the P- substrate 130 may be made of silicon comprising boron impurities having a concentration of approximately 10^{15} atoms/cm³. In alternative embodiments, a plurality of P- substrates 130 may form the base of the memory cell array 20 or a single P- substrate 130 may form the base of the memory cell array 20. Also, the P- substrate 130 may be made in the form of a P-well substrate.

Referring to Figure 4, there is shown a schematic view of at least a portion of the memory cell array 20 having a plurality of memory cells 12 in accordance with an embodiment of the present disclosure. The memory cells 12 may be coupled to a corresponding plurality of word lines (WL) 28, a corresponding bit line (CN) 30, and/or a corresponding source line (EN) 32. The plurality of word lines (WL) 28 may comprise a first word line (WL<0>) and a second word line (WL<1>) capacitively coupled to the memory cell 12 via the tunneling insulating layer 202. Each of the memory cells 12 may comprise a first floating gate region 14a and a second floating gate region 14b coupled to each other. The first floating gate region 14a and the second floating gate region 14b may be different regions of the body region 322 of the memory cell 12. In a particular embodiment, the first floating gate region 14a may be capacitively coupled to the first word line (WL1<0>) via the tunneling insulating layer 202. The second floating gate region 14b may be capacitively coupled to the second word line (WL1<1>) via the tunneling

insulating layer 202.

Data may be written to or read from a selected memory cell 12 by applying suitable control signals to a selected word line (WL) 28, a selected bit line (CN) 30, and/or a selected source line (EN) 32. For example, a data state (e.g., a logic low (e.g., binary "0" data state) and/or a logic high (e.g., binary "1" data state)) may be written to the first floating gate region 14a and the second floating gate region 14b. The same data state or different data state may be simultaneously written to the first floating gate region 14a and the second floating gate region 14b. The same data state or different data state may be sequentially written to the first floating gate region 14a and the second floating gate region 14b. Also, a data state may be simultaneously or sequentially read from the first floating gate region 14a and the second floating gate region 14b.

In a particular embodiment, one or more respective bit line (CN) 30 may be coupled to one or more data sense amplifiers of the data write and sense circuitry 36. For example, one or more control signals may be applied to one or more selected memory cells 12 via a selected plurality of word lines (WL) 28, a selected bit line (CN) 30, and/or a selected source line (EN) 32. A voltage and/or a current may be generated by the first floating gate region 14a and/or the second floating gate region 14b of the one or more selected memory cells 12 and outputted to the data write and sense

circuitry 36 via a corresponding bit line (CN) 30. Also, a data state may be written to the first floating gate region 14a and/or the second floating gate region 14b of the one or more selected memory cells 12 by applying one or more control signals via one or more corresponding plurality of word lines (WL) 28, one or more corresponding bit lines (CN) 30, and/or one or more corresponding source line (EN) 32. One or more control signals applied via the corresponding first word line (WL<0>) 28 may control the first floating gate region 14a of the memory cell 12 in order to write a desired data state to the memory cell 12. One or more control signals applied via the corresponding second word line (WL<1>) 28 may control the second floating gate region 14b of the memory cell 12 in order to write a desired data state to the memory cell 12. In the event that a data state is read from and/or written to the memory cell 12 via the bit line (CN) 30, the bit line (CN) 30 may be coupled to the data sense amplifier of the data write and sense circuitry 36 while the source line (EN) 32 may be separately controlled via a voltage/current source (e.g., a voltage/current driver) of the data write and sense circuitry 36. In a particular embodiment, the data sense amplifier of the data write and sense circuitry 36 and the voltage/current source of the data write and sense circuitry 36 may be configured on opposite sides of the memory cell array 20.

Referring to Figure 5, there is shown voltage potential levels of various methods for performing a write operation and

a read operation on a memory cell 12 as shown in Figures 2-4 in accordance with an embodiment of the present disclosure. The write operation may include a write logic low (e.g., binary "0" data state) operation and a write logic high (e.g., binary "1" data state) operation. In a particular embodiment, the various methods of performing a write logic low (e.g., binary "0" data state) operation may comprise an erase forward node tunneling write operation and/or an erase hot-hole write operation. In another embodiment, the various methods of performing a write logic high (e.g., binary "1" data state) operation may comprise a program forward node tunneling write operation and/or a program hot-electron write operation.

The erase forward node tunneling write operation may perform a write logic low (e.g., binary "0" data state) operation by depleting charge carriers (e.g., electrons) stored in the memory cell 12. During the erase forward node tunneling write operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V). The plurality of bit lines (CN) 30 may be decoupled from a voltage potential source and/or current source and may be electrical open or electrically floating. A negative voltage potential may be applied to the source region 320. The negative voltage potential applied to the source region 320 may forward bias the junction between the source region 320 and the P- substrate 130. In a particular embodiment, the negative voltage potential applied to the source region 320 may be -

1.0V. Simultaneously to or after forward biasing the junction between the source region 320 and the P- substrate 130, a negative voltage potential may be applied to the plurality of word lines (WL) 28 (e.g., that may be capacitively coupled to the floating gate regions 14a and 14b of the body region 322). The negative voltage potential applied to the plurality of word lines (WL) 28 may tunnel electrons that may have accumulated/stored in the charge trapping region 202(d) via the forward biased junction between the source region 320 and the P- substrate 130. By driving out the electrons that may have accumulated/stored in the charge trapping region 202(d), a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

The erase hot-hole write operation may perform a write logic low (e.g., binary "0" data state) operation by accumulate/store minority charge carriers (e.g., holes) in order to compensate for the majority charge carriers (e.g., electrons) that may have accumulated/stored in the memory cell 12. During the erase hot-hole operation, the P- substrate 130 and the source region 320 may be coupled to an electrical ground (e.g., 0V). Thus, the junction between the P- substrate 130 and the source region 320 may remain in reversed biased or weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A positive voltage potential may be applied to the drain region 324 via the bit line (CN) 30. In a particular

embodiment, the positive voltage potential applied to the drain region 324 may be 5.0V. Also, a negative voltage potential may be applied to the plurality of word lines (WL) 28 (e.g., that are capacitively coupled to the body region 322 via the tunneling insulating layer 202). In a particular embodiment, the negative voltage potential applied to the plurality of word lines (WL) 28 (e.g., that may be capacitively coupled to the body region 322 via the tunneling insulating layer 202) may be -11.0V.

The positive voltage potential applied to the drain region 324 and the negative voltage potential applied to the plurality of word lines (WL) 28 may create a band-to-band tunneling (gate-induced drain leakage "GIDL") effect between the drain region 324 and the body region 322. Due to the band-to-band tunneling (gate-induced drain leakage "GIDL") effect, minority charge carriers (e.g., holes) may be injected into the charge trapping layer 202(d) by the negative voltage potential applied to the plurality of word lines (WL) 28. A predetermined amount of minority charge carriers (e.g., holes) may be accumulated/stored in the charge trapping region 202(d) of the memory cell 12. The predetermined amount of minority charge carriers (e.g., holes) that may be accumulated/stored in the charge trapping region 202(d) may outnumber the amount of majority charge carriers (e.g., electrons) that may be accumulated/stored in the charge trapping region 202(d). The predetermined amount of minority charge carriers (e.g., holes)

accumulated/stored in the charge trapping region 202(d) of the memory cell 12 may represent that a logic low (e.g., binary "0" data state) may be stored in the memory cell 12.

The program forward node tunneling write operation may perform a write logic high (e.g., binary "1" data state) operation by injecting majority charge carriers into the memory cell 12. During the program forward node tunneling write operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V) and the drain region 324 may be coupled to an electrical ground (e.g., 0V). The source region 320 of the memory cell 12 may be decoupled from a voltage potential source/current source and may be electrically floating (e.g., open). A positive voltage potential may be applied to the plurality of word lines (WL) 28 (e.g., that may be capacitively coupled the body region 322 of the memory cell 12 via the tunneling insulating layer 202). In a particular embodiment, the positive voltage potential applied to the plurality of word lines (WL) 28 may be 16.0V.

The positive voltage potential applied to the plurality of word lines (WL) 28 may switch the memory transistor (e.g., comprising source region 320, body region 322, and/or drain region 324) to an "ON" state. The positive voltage potential applied to the plurality of word lines (WL) 28 may cause a predetermined amount of majority charge carriers (e.g., electrons) to be injected into the body region 322 of the memory cell 12 when the memory transistor (e.g., comprising

the source region 320, the body region 322, and/or the drain region 324) is turned to an "ON" state. The predetermined amount of majority charge carriers (e.g., electrons) may be tunneled into and accumulated/stored in the charge trapping region 202(d) to represent that a logic high (e.g., binary "1" data state) is stored in the memory cell 12.

For an unselected memory cell 12, the voltage potential applied to the plurality of word lines (WL) 28 may be coupled to an electrical ground (e.g., 0V). A positive voltage potential may be applied to the drain region 324 via the bit line (CN) 30. In a particular embodiment, the positive voltage potential applied to the drain region 324 may be 3.0V. The memory transistor (e.g., comprising the source region 320, the body region 322, and the drain region 324) may be turned to an "OFF" state. No majority charge carriers or a small amount of majority charge carriers (e.g., electrons) may be injected into the body region 322 of the memory cell 12. Thus, the program forward node tunnel write operation may not be performed on the unselected memory cell 12.

The program hot-electron write operation may perform a write logic high (e.g., binary "1" data state) operation by accumulating/storing majority charge carriers (e.g., electrons) in the memory cell 12. During the program hot-electron write operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V) and the source region 320 may be coupled to an electrical ground (e.g., 0V). The

junction between the P- substrate 130 and the source region 320 may be reversed biased or weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A positive voltage potential 5 may be applied to the drain region 324 via the bit line (CN) 30. In a particular embodiment, the positive voltage potential applied to the drain region 324 via the bit line (CN) 30 may be 5.0V.

A positive voltage potential may be applied to the first 10 word line (WL1<0>) 28 that may be capacitively coupled to the first floating gate region 14a of the body region 322. A negative voltage potential may be applied to the second word line (WL1<1>) 28 that may be capacitively coupled to the second floating gate region 14b of the body region 322. The 15 positive voltage potential applied to the drain region 324 and the word line (WL1<0>) 28 may create a band-to-band tunneling (gate-induced drain leakage "GIDL") effect between the drain region 324 and the body region 322. A predetermined amount of majority charge carrier (e.g., electrons) may be tunneled into 20 the charge trapping region 202(d). The positive voltage potential applied to the first word line (WL1<0>) (e.g., that may be capacitively coupled to the first floating gate region 14a of the body region 322) may accumulate/store the majority charge carriers (e.g., electrons) in the charge trapping 25 region 202(d) of the first floating gate region 14a. The negative voltage potential applied to the second word line

(WL1<1>) 28 may repel majority charge carriers (e.g., electrons) injected into the first floating gate region 14a of the body region 322. The predetermined amount of majority charge carriers (e.g., electrons) stored in the first floating gate region 14a of the body region 322 may represent that a logic high (e.g., binary "1" data state) is stored in the memory cell 12.

A read operation may be performed to read a data state (e.g., a logic low (e.g., binary "0" data state) and/or a logic high (e.g., binary "1" data state)) stored in the memory cell 12. During a read operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V) and the source region 320 may be coupled to an electrical ground (e.g., 0V). A positive voltage potential may be applied to the drain region 324 of the memory cell 12 via the bit line (CN) 30. In a particular embodiment, the positive voltage potential applied to the drain region 324 may be 1.0V. A positive voltage potential may be applied to the first word line (WL1<0>) 28 that may be capacitively coupled to the first floating gate region 14a of the body region 322 via the tunneling insulating layer 202. A negative voltage potential may be applied to the second word line (WL1<1>) 28 that may be capacitively coupled to the second floating gate region 14b of the body region 322 via the tunneling insulating layer 202. In a particular embodiment, the positive voltage potential applied to the first word line (WL1<0>) 28 that may be

capacitively coupled to the first floating gate region 14a may be 3.0V. In another embodiment, the negative voltage potential applied to the second word line (WL1<1>) 28 that may be capacitively coupled to the second floating gate region 14b may be -3.0V.

Under such biasing, the memory transistor (e.g., comprising the source region 320, the body region 322, and/or the drain region 324) may be turned to an "ON" state via the first floating gate region 14a and the drain region 324. The memory transistor may be turned to an "OFF" state via the second floating gate region 14b and the drain region 324. The majority charge carriers (e.g., electrons) may flow from the first floating gate region 14b to the drain region 324 when the memory transistor (e.g., comprising the source region 320, the body region 322, and/or the drain region 324) is turned to an "ON" state. In a particular embodiment, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12, a predetermined amount of voltage potential and/or current may be detected at the drain region 324. In another embodiment, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12, no voltage potential and/or current may be detected at the drain region 324.

Referring to Figure 6, there is shown a top view of at least a portion of the memory cell array 20 as shown in Figure 1 in accordance with an alternate embodiment of the present disclosure. As illustrated in the top view, the memory cell

array 20 may include a plurality of memory cells 12 arranged in a matrix of rows and columns including a plurality of word lines 28 (WL), a plurality of bit lines (CN) 30, and/or a source line stripe (EN) 32. Each bit line (CN) 30 may extend
5 in a first orientation along a first plane of the memory cell array 20. The source line strip (EN) 32 may extend in a second orientation along a second plane of the memory cell array 20. Each word line (WL) 28 may extend in the second orientation along a third plane of the memory cell array 20.
10 The first plane, the second plane, and the third plane of the memory cell array 20 may be arranged in different planes parallel to each other.

The plurality of word lines (WL) 28 may be formed of a polycide material (e.g., a combination of a metal material and
15 a silicon material), a metal material, and/or a combination of a polycide material and a metal material. In a particular embodiment, the word lines (WL) 28 may capacitively couple a voltage potential/current source of the memory cell selection and control circuitry 38 to the memory cells 12. The word
20 line (WL) 28 may be formed of a plurality layers. Each layer of the word line (WL) 28 may be formed of different materials having various thicknesses. In a particular embodiment, the first layer (f) of the word line (WL) 28 may be formed of a silicon material having a thickness of approximately 1 nm.
25 The second layer (g) of the word line (WL) 28 may be formed of a metal material having a thickness of approximately 10 nm.

In a particular embodiment, the word line (WL) 28 may be arranged between two contiguous memory cells 12 and capacitively coupled to the two contiguous memory cells 12. For example, the word line (WL) 28 may implement an operation
5 simultaneously to the two contiguous memory cells 12.

The plurality of word lines (WL) 28 may be an electrically capacitively coupled to a plurality of memory cells 12 via a tunneling insulating layer 202. The tunneling insulating layer 202 may comprise a plurality of insulating or
10 dielectric layers. In a particular embodiment, the tunneling insulating layer 202 may comprise a thermal oxide layer 202(a), a nitride layer 202(b), an oxide layer 202(c), a charge trapping nitride layer 202(d) (e.g., silicon nitride), and/or a blocking oxide layer 202(e). The plurality of
15 insulating or dielectric layers of the tunneling insulating layer 202 may comprise of various thickness. In a particular embodiment, the thermal oxide layer 202(a) may have a thickness of approximately 1.5 nm, the nitride layer 202(b) may have a thickness of approximately 2 nm, the oxide layer
20 202(c) may have a thickness of approximately 2.5 nm, the charge trapping nitride layer 202(d) (e.g., silicon nitride) may have a thickness of approximately 5 nm, and/or the blocking oxide layer 202(e) may have a thickness of approximately 5 nm.

25 The memory cell 12 may be configured to maximize scaling of memory cells 12 in the semiconductor memory device 10. In

a particular embodiment, the memory cell 12 may be configured to have a width (i) (e.g., along the direction of the bit line (CN) 30) of approximately 40 nm. The width (i) of the memory cell 12 may be limited by floating gate to floating gate interference and inversion layer interference. The spacing (K) between contiguous row of memory cells 12 (e.g., along the direction of the word line (WL) 28) may be approximately F nm, wherein F may be the minimum space possible. The memory cell 12 may be configured to have a length (j) (e.g., along the direction of the word line (WL) 28) of approximately F, wherein F may be the minimum space possible nm.

Referring to Figure 7, there are shown cross-sectional views of at least a portion of the memory cell array 20 as shown in Figure 6 in accordance with an embodiment of the present disclosure. Figure 7 illustrates a cross-sectional view of at least a portion of the memory cell array 20 along line A-A and a cross-sectional view of at least a portion of the memory cell array 20 along line B-B. The memory cells 12 of the memory cell array 20 may be implemented in a vertical configuration having various regions. For example, the memory cell 12 may comprise a source region 720, a body region 722, and a drain region 724. The source region 720, the body region 722, and/or the drain region 724 may be disposed in a sequential contiguous relationship, and may extend vertically from a plane defined by a P- substrate 130. The source region 720 of the memory cell 12 may be coupled to the source line

(EN) 32. The body region 722 may be an electrically floating body region of the memory cell 12 configured to accumulate/store charges, and may be spaced apart from and capacitively coupled to the plurality of word lines (WL) 28 via the tunneling insulating layer 202. The drain region 724 of the memory cell 12 may be coupled to the bit line (CN) 30.

The source region 720 of the memory cell 12 may be coupled to a corresponding source line (EN) 32. In a particular embodiment, the source region 720 may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the source region 720 may be formed of a silicon material doped with phosphorous or arsenic impurities. In a particular embodiment, the source region 720 may be formed of a silicon material doped with phosphorous or arsenic having a concentration of approximately 10^{20} atoms/cm³ or above. The source region 720 may comprise a strip region having an elongated continuous planar region configured above the P- substrate 130. The elongated continuous planar region of the source region 720 may form a column or a row of the memory cell array 20. The source region 720 may also comprise a plurality of protrusions formed on the elongated continuous planar region. The plurality of protrusions of the source region 720 may be oriented in a column direction and/or a row direction of the memory cell array 20. The plurality of protrusions of the source region 720 may form the base of the memory cell 12.

In a particular embodiment, the source line (EN) 32 may be coupled to the elongated continuous planar region of the source region 720. In a particular embodiment, the source line (EN) 32 may be formed of an N⁺ doped silicon layer. In another embodiment, the source line (EN) 32 may be formed of a metal material. In other embodiments, the source line (EN) 32 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). The source line (EN) 32 may couple a predetermined voltage potential to the memory cells 12 of the memory cell array 20. For example, the source line (EN) 32 may be coupled to a plurality of memory cells 12 (e.g., a column or a row of memory cell array 20).

The body region 722 of the memory cell 12 may be capacitively coupled to a corresponding word lines (WL) 28 via the tunneling insulating layer 202. The tunneling insulating layer 202 may be formed between contiguous memory cells 12 surrounding the corresponding word line (WL) 28 configured between the contiguous memory cells 12. In a particular embodiment, the body region 722 may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. The body region 722 may be formed of a silicon material doped with boron impurities. In a particular embodiment, the body region 722 may be formed of a silicon material with acceptor impurities having a concentration of approximately 10^{15} atoms/cm³. In a particular embodiment, the body region 722 may comprise a first floating gate region 14a

and a second floating gate region 14b. The first floating gate region 14a and the second floating gate region 14b may accumulate/store charge carriers in order to represent a data state (e.g., a logic low (e.g., binary "0" data state) and/or
5 a logic high (e.g., binary "1" data state)).

The word lines (WL) 28 may be capacitively coupled the body region 722. The word lines (WL) 28 may be oriented in a row direction of the memory cell array 20 and coupled to a plurality of memory cells 12. The word lines (WL) 28 may be
10 arranged on the sides of the memory cells 12 (e.g., memory cells 12 located on a row direction of the memory cell array 20). For example, the word lines (WL) 28 may be arranged on a side portion of the memory cells 12. For example, the word line (WL) 28 may be capacitively coupled to a first floating
15 gate region 14a of the body region 722 of the first memory cell 12 and capacitively coupled to a second floating gate region 14b of the body region 722 of the second memory cell 12. Thus, the word line (WL) 28 may be arranged between the first memory cell 12 and the second memory cell 12.

20 The drain region 724 of the memory cell 12 may be coupled to a corresponding bit line (CN) 30. In a particular embodiment, the drain region 724 of the memory cell 12 may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the drain region 724 may be
25 formed of a silicon material doped with phosphorous or arsenic impurities. In a particular embodiment, the drain region 724

may be formed of a silicon material doped with phosphorous or arsenic having a concentration of approximately 10^{20} atoms/cm³ or above.

The bit line (CN) 30 may be coupled to the drain region 724 of the memory cell 12. The bit line (CN) 30 may be formed of a metal material. In another embodiment, the bit line (CN) 30 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other embodiments, the bit line (CN) 30 may be formed of an N+ doped silicon layer. For example, the bit line (CN) 30 may be coupled to a plurality of memory cells 12. The bit line (CN) 30 may be configured above the drain region 724.

The bit line (CN) 30 may be connected to a plurality of memory cells 12 (e.g., a column of memory cells 12) via a plurality of bit line contacts 726. For example, each bit line contact 726 may correspond to a memory cell 12 along a column direction of the memory cell array 20. Each bit line contact 726 may be formed of a metal layer or a polysilicon layer in order to couple a voltage potential from the bit line (CN) 30 to the drain region 724 of the memory cell 12. For example, the bit line contact 726 may be formed of tungsten, titanium, titanium nitride, polysilicon or a combination thereof. The bit line contact 726 may have a height extending from the bit line (CN) 30 to the drain region 724 of the memory cell 12.

In a particular embodiment, the P- substrate 130 may be

made of a semiconductor material (e.g., silicon) comprising acceptor impurities and may form a base of the memory cell array 20. For example, the P- substrate 130 may be made of a semiconductor material comprising boron impurities. In a particular embodiment, the P- substrate 130 may be made of silicon comprising boron impurities having a concentration of approximately 10^{15} atoms/cm³. In alternative embodiments, a plurality of P- substrates 130 may form the base of the memory cell array 20 or a single P- substrate 130 may form the base of the memory cell array 20. Also, the P- substrate 130 may be made in the form of a P-well substrate.

Referring to Figure 8, there is shown a schematic diagram of at least a portion of the memory cell array 20 having a plurality of memory cells 12 in accordance with an alternate embodiment of the present disclosure. The memory cells 12 may be coupled to a corresponding word line (WL) 28, a corresponding bit line (CN) 30, and/or a corresponding source line (EN) 32. The word line (WL) 28 may be capacitively coupled to a plurality of memory cells 12 via the tunneling insulating layer 202. In a particular embodiment, the word line (WL1) 28 may be capacitively coupled to the second floating gate region 14b of the first memory cell 12a. Also, the word line (WL1) may be capacitively coupled to the first floating gate region 14a of the second memory cell 12b.

Data may be written to or read from a selected memory cell 12 by applying suitable control signals to a selected

word line (WL) 28, a selected bit line (CN) 30, and/or a selected source line (EN) 32. For example, a data state (e.g., a logic low (e.g., binary "0" data state) and/or a logic high (e.g., binary "1" data state)) may be written to the first floating gate region 14a and the second floating gate region 14b. The same data state or different data state may be simultaneously written to two contiguous memory cells 12. In a particular embodiment, the same data state or different data state may be simultaneously written to the second floating gate region 14b of the first memory cell 12b and the first floating gate region 14b of the second memory cell 12b. The same data state or different data state may be sequentially written to contiguous memory cells 12. In a particular embodiment, the same data state or different data state may be sequentially written to the second floating gate region 14b of the first memory cell 12a and the first floating gate region 14a of the second memory cell 12b. Also, a data state may be simultaneously or sequentially read from the first floating gate region 14a and the second floating gate region 14b.

In a particular embodiment, one or more respective bit line (CN) 30 may be coupled to one or more data sense amplifiers of the data write and sense circuitry 36. For example, one or more control signals may be applied to one or more selected memory cells 12 via a selected word line (WL) 28, a selected bit line (CN) 30, and/or a selected source line

(EN) 32. A voltage potential and/or a current may be generated by the first floating gate region 14a and/or the second floating gate region 14b of the one or more selected memory cells 12 and outputted to the data write and sense circuitry 36 via a corresponding bit line (CN) 30. Also, a data state may be written to the first floating gate region 14a and/or the second floating gate region 14b of the one or more selected memory cells 12 by applying one or more control signals via one or more corresponding word lines (WL) 28, one or more corresponding bit lines (CN) 30, and/or one or more corresponding source line (EN) 32. One or more control signals applied via a corresponding word line (WL1) 28 may control the second floating gate region 14b of the first memory cell 12a and the first floating gate region 14a of the second memory cell 12b in order to write a desired data state to the memory cell 12. One or more control signals applied via the corresponding second word line (WL2) 28 may control the second floating gate region 14b of the second memory cell 12b and the first floating gate region 14a of the third memory cell 12c in order to write a desired data state to the memory cells 12. In the event that a data state is read from and/or written to the memory cell 12 via the bit line (CN) 30, the bit line (CN) 30 may be coupled to the data sense amplifier of the data write and sense circuitry 36 while the source line (EN) 32 may be separately controlled via a voltage/current source (e.g., a voltage/current driver) of the data write and

sense circuitry 36. In a particular embodiment, the data sense amplifier of the data write and sense circuitry 36 and the voltage/current source of the data write and sense circuitry 36 may be configured on opposite sides of the memory cell array 20.

Referring to Figure 9, there is shown voltage potential levels of various methods for performing a write operation and a read operation on a memory cell 12 as shown in Figures 6-8 in accordance with an embodiment of the present disclosure.

The write operation may include a write logic low (e.g., binary "0" data state) operation and a write logic high (e.g., binary "1" data state) operation. In a particular embodiment, the various methods of performing a write logic low (e.g., binary "0" data state) operation may comprise an erase forward node tunneling write operation and/or an erase hot-hole write operation. In another embodiment, the various methods of performing a write logic high (e.g., binary "1" data state) operation may comprise a program forward node tunneling write operation and/or a program hot-electron write operation.

The erase forward node tunneling write operation may perform a write logic low (e.g., binary "0" data state) operation by depleting charge carriers (e.g., electrons) stored in the memory cell 12. During the erase forward node tunneling write operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V). The plurality of bit lines (CN) 30 may be decoupled from a voltage potential source

and/or current source and may be electrical open or electrically floating. A negative voltage potential may be applied to the source region 720. The negative voltage potential applied to the source region 720 may forward bias the junction between the source region 720 and the P-substrate 130. In a particular embodiment, the negative voltage potential applied to the source region 720 may be -1.0V. Simultaneously to or after forward biasing the junction between the source region 720 and the P-substrate 130, a negative voltage potential may be applied to the plurality of word lines (WL) 28 (e.g., that may be capacitively coupled to the floating gate regions 14a and 14b of the body region 722). The negative voltage potential applied to the plurality of word lines (WL) 28 may tunnel electrons that may have accumulated/stored the charge trapping region 202(d) via the forward biased junction between the source region 720 and the P-substrate 130. By driving out the electrons that may have accumulated/stored in the charge trapping region 202(d), a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

The erase hot-hole write operation may perform a write logic low (e.g., binary "0" data state) operation by accumulate/store minority charge carriers (e.g., holes) in order to compensate for the majority charge carriers (e.g., electrons) that may have accumulated/stored in the memory cell 12. During the erase hot-hole operation, the P-substrate 130

and the source region 720 may be coupled to an electrical ground (e.g., 0V). Thus, the junction between the P-substrate 130 and the source region 720 may remain in reversed biased or weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A positive voltage potential may be applied to the drain region 724 via the bit line (CN) 30. In a particular embodiment, the positive voltage potential applied to the drain region 724 may be 5.0V. Also, a negative voltage potential may be applied to the plurality of word lines (WL) 28 (e.g., that are capacitively coupled to the body region 722 via the tunneling insulating layer 202). In a particular embodiment, the negative voltage potential applied to the plurality of word lines (WL) 28 (e.g., that may be capacitively coupled to the body region 722 via the tunneling insulating layer 202) may be -11.0V.

The positive voltage potential applied to the drain region 724 and the negative voltage potential applied to the plurality of word lines (WL) 28 may create a band-to-band tunneling (gate-induced drain leakage "GIDL") effect between the drain region 724 and the body region 722. Due to the band-to-band tunneling (gate-induced drain leakage "GIDL") effect, minority charge carriers (e.g., holes) may be injected into the charge trapping region 202(d) by the negative voltage potential applied to the plurality of word lines (WL) 28. A predetermined amount of minority charge carriers (e.g., holes)

may be accumulated/stored in the charge trapping region 202(d) of the memory cell 12. The predetermined amount of minority charge carriers (e.g., holes) that may be accumulated/stored in the charge trapping region 202(d) may outnumber the amount of majority charge carriers (e.g., electrons) that may be accumulated/stored in the charge trapping region 202(d). The predetermined amount of minority charge carriers (e.g., holes) accumulated/stored in the charge trapping region 202(d) of the memory cell 12 may represent that a logic low (e.g., binary "0" data state) may be stored in the memory cell 12.

The program forward node tunneling write operation may perform a write logic high (e.g., binary "1" data state) operation by injecting majority charge carriers (e.g., electrons) into the memory cell 12. During the program forward node tunneling write operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V), the selected source region (Src<1>) 720 may be coupled to an electrical ground (e.g., 0V), and the selected drain region (CN1) 724 may be coupled to an electrical ground (e.g., 0V). The unselected source region (Src<n>) 720 of the memory cell 12 may be decoupled from a voltage potential source/current source and may be electrically floating (e.g., open). A positive voltage potential may be applied to the selected word line (WL0) 28 (e.g., that may be capacitively coupled the body region 722 of the memory cell 12 via the tunneling insulating layer 202). In a particular embodiment, the positive voltage

potential applied to the selected word line (WL0) 28 may be 16.0V.

The positive voltage potential applied to the selected word line (WL0) 28 may turn the memory transistor (e.g., comprising the source region 720, the body region 722, and/or the drain region 724) to an "ON" state. The positive voltage potential applied to the selected word line (WL0) 28 may cause a predetermined amount of majority charge carriers (e.g., electrons) to be injected into the body region 722 of the memory cell 12 when the memory transistor (e.g., comprising the source region 720, the body region 722, and/or the drain region 724) is turned to an "ON" state. The predetermined amount of majority charge carriers (e.g., electrons) may be tunneled into and/or accumulated/stored in the charge trapping region 202(d) to represent that a logic high (e.g., binary "1" data state) is stored in the memory cell 12.

For an unselected memory cell 12, the voltage potential applied to the plurality of word lines (WL) 28 may be coupled to an electrical ground (e.g., 0V). A positive voltage potential may be applied to the drain region 724 via the bit line (CNn) 30. In a particular embodiment, the positive voltage potential applied to the drain region 724 via the unselected bit line (CNn) 30 may be 3.0V. The memory transistor (e.g., comprising the source region 720, the body region 722, and/or the drain region 724) may be turned to an "OFF" state. No majority charge carriers or a small amount of

majority charge carriers (e.g., electrons) may be injected into the body region 722 of the memory cell 12. Thus, the program forward node tunnel write operation may not be performed on the unselected memory cell 12.

5 The program hot-electron write operation may perform a write logic high (e.g., binary "1" data state) operation by accumulating/storing majority charge carriers (e.g., electrons) in the memory cell 12. During the program hot-electron write operation, the P- substrate 130 may be coupled
10 to an electrical ground (e.g., 0V) and the selected source region (Src<1>) 720 may be coupled to an electrical ground (e.g., 0V). The junction between the P- substrate 130 and the source region 720 may be reversed biased or weakly forward biased (e.g., above a reverse bias voltage and below a forward
15 bias threshold voltage potential). A positive voltage potential may be applied to the drain region 724 via the bit line (CN1) 30. In a particular embodiment, the positive voltage potential applied to the drain region 724 via the bit line (CN1) 30 may be 5.0V.

20 A positive voltage potential may be applied to the first word line (WL<0>) 28 that may be capacitively coupled to the first floating gate region 14a of the body region 722. A negative voltage potential may be applied to the second word line (WL<1>) 28 that may be capacitively coupled to the second
25 floating gate region 14b of the body region 722. The positive voltage potentials applied to the drain region 724 and/or the

word line (WL<0>) 28 may create a band-to-band tunneling (gate-induced drain leakage "GIDL") effect between the drain region 724 and the body region 722. A predetermined amount of majority charge carrier (e.g., electrons) may be tunneled into
5 the charge trapping region 202(d). The positive voltage potential applied to the first word line (WL<0>) 28 (e.g., that may be capacitively coupled to the first floating gate region 14a of the body region 722) may cause an accumulation/storage of majority charge carriers (e.g.,
10 electrons) in the charge trapping region 202(d) of the first floating gate region 14a. The negative voltage potential applied to the second word line (WL<1>) 28 may repel majority charge carriers (e.g., electrons) injected into the second floating gate region 14b of the body region 722. The
15 predetermined amount of majority charge carriers (e.g., electrons) stored in the first floating gate region 14a of the body region 722 may represent that a logic high (e.g., binary "1" data state) is stored in the memory cell 12.

A read operation may be performed to read a data state
20 (e.g., a logic low (e.g., binary "0" data state) and/or a logic high (e.g., binary "1" data state)) stored in the memory cell 12. During a read operation, the P- substrate 130 may be coupled to an electrical ground (e.g., 0V) and the selected source region (Src<1>) 720 may be coupled to an electrical
25 ground (e.g., 0V). A positive voltage potential may be applied to the drain region 724 of the memory cell 12 via the

bit line (CN) 30. In a particular embodiment, the positive voltage potential applied to the drain region 724 may be 1.0V. A positive voltage potential may be applied to the first word line (WL<0>) 28 that may be capacitively coupled to the first floating gate region 14a of the body region 722 via the tunneling insulating layer 202. A negative voltage potential may be applied to the second word line (WL<1>) 28 that may be capacitively coupled to the second floating gate region 14b of the body region 722 via the tunneling insulating layer 202.

10 In a particular embodiment, the positive voltage potential applied to the first word line (WL<0>) 28 that may be capacitively coupled to the first floating gate region 14a may be 3.0V. In another embodiment, the negative voltage potential applied to the second word line (WL<1>) 28 that may

15 be capacitively coupled to the second floating gate region 14b may be -3.0V.

Under such biasing, the memory transistor (e.g., comprising the source region 720, the body region 722, and/or the drain region 724 may be turned to an "ON" state via the first floating gate region 14a and/or the drain region 724. The memory transistor (e.g., comprising the source region 720, the body region 722, and/or the drain region 724) may be turned to an "OFF" state via the second floating gate region 14b and the drain region 724. The majority charge carriers

25 (e.g., electrons) may flow from the first floating gate region 14a to the drain region 724 when the memory transistor (e.g.,

comprising the source region 720, the body region 722, and/or the drain region 724) is turned to an "ON" state. In a particular embodiment, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12, a predetermined amount of voltage potential and/or current may be detected at the drain region 724. In another embodiment, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12, no voltage potential and/or current may be detected at the drain region 724.

At this point it should be noted that providing a semiconductor memory device in accordance with the present disclosure as described above may involve the processing of input data and the generation of output data to some extent. This input data processing and output data generation may be implemented in hardware or software. For example, specific electronic components may be employed in a semiconductor memory device or similar or related circuitry for implementing the functions associated with providing a semiconductor memory device in accordance with the present disclosure as described above. Alternatively, one or more processors operating in accordance with instructions may implement the functions associated with providing a semiconductor memory device in accordance with the present disclosure as described above. If such is the case, it is within the scope of the present disclosure that such instructions may be stored on one or more non-transitory processor readable storage media (e.g., a

magnetic disk or other storage medium), or transmitted to one or more processors via one or more signals embodied in one or more carrier waves.

The present disclosure is not to be limited in scope by
5 the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Thus, such
10 other embodiments and modifications are intended to fall within the scope of the present disclosure. Further, although the present disclosure has been described herein in the context of at least one particular implementation in at least one particular environment for at least one particular
15 purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in
20 view of the full breadth and spirit of the present disclosure as described herein.

CLAIMS

1. A semiconductor memory device comprising:

a plurality of memory cells arranged in an array of rows and columns, each memory cell comprising:

5 a first region coupled to a source line;

a second region coupled to a bit line; and

a body region capacitively coupled to at least one word line via a tunneling insulating layer and disposed between the first region and the second region.

10

2. The semiconductor memory device according to claim 1, wherein the first region and the second region are doped with donor impurities.

15 3. The semiconductor memory device according to claim 1, wherein the body region is doped with acceptor impurities.

4. The semiconductor memory device according to claim 1, wherein the tunneling insulating layer comprises a plurality
20 of insulating or dielectric layers.

5. The semiconductor memory device according to claim 4, wherein the plurality of insulating or dielectric layers comprise at least one of a thermal oxide layer, a nitride
25 layer, an oxide layer, a charge trapping nitride layer, and a

blocking oxide layer.

6. The semiconductor memory device according to claim 5,
wherein the plurality of insulating or dielectric layers
5 comprise of various thicknesses.

7. The semiconductor memory device according to claim 1,
wherein the at least one word line comprises a plurality of
layers.

10

8. The semiconductor memory device according to claim 7,
wherein the plurality of layers of the word line comprise a
first silicon layer having a thickness of approximately one
tenth of a thickness of a second metal layer.

15

9. The semiconductor memory device according to claim 1,
wherein the first region, the second region, and the body
region are disposed in a sequential contiguous relationship
and extend vertically from a plane defined by a P- substrate.

20

10. The semiconductor memory device according to claim 1,
wherein the body region comprises a first floating gate region
and a second floating gate region.

25 11. The semiconductor memory device according to claim 10,

wherein the first floating gate region is capacitively coupled to a first word line of the at least one word line and the second floating gate region is capacitively coupled to a second word line of the at least one word line.

5

12. The semiconductor memory device according to claim 1, wherein the at least one word line is capacitively coupled a second body region.

10 13. The semiconductor memory device according to claim 12, wherein the at least one word line is capacitively coupled to a first floating gate region of the body region and a second floating gate region of the second body region.

15 14. The semiconductor memory device according to claim 1, wherein the first region comprises a continuous planar region.

15. The semiconductor memory device according to claim 14, wherein the first region further comprises a plurality of
20 protrusions formed on the continuous planar region.

16. The semiconductor memory device according to claim 1, wherein the first region comprises an elongated continuous planar region.

25

17. The semiconductor memory device according to claim 15, wherein the elongated continuous planar region forms a column or a row of the array.

5 18. A method for biasing a semiconductor memory device comprising the steps of:

applying a plurality of voltage potentials to a plurality of memory cells arranged in an array of rows and columns, wherein applying the plurality of voltage potentials to the
10 plurality of memory cells comprises:

applying a first voltage potential to a first region of each of the plurality of memory cells;

applying a second voltage potential to a second region of each of the plurality of memory cells; and

15 applying a third voltage potential to a body region of each of the plurality of memory cells via at least one respective word line of the array that is capacitively coupled to the body region via a tunneling insulating layer.

20 19. The method according to claim 18, further comprising coupling a P- substrate to an electrical ground.

20. The method according to claim 19, wherein the first voltage potential is applied to the first region to perform a
25 write logic low operation.

21. The method according to claim 20, wherein the third voltage potential applied to the body region is a negative voltage potential to repel majority charge carriers from the body region in order to perform the write logic low operation.

22. The method according to claim 19, wherein second voltage potential applied to the second region and the third voltage potential applied to the body region are to perform a write logic low operation.

23. The method according to claim 22, wherein the third voltage potential applied to the body region is a negative voltage potential that tunnels minority charge carriers into the body region in order to perform the write logic low operation.

24. The method according to claim 19, wherein the second voltage potential applied to the second region and the third voltage potential applied to the body region are positive voltage potentials in order to perform a write logic high operation.

25. The method according to claim 24, wherein the positive voltage potentials applied to the second region and the body

region creates a band-to-band tunneling effect to tunnel majority charge carriers to the body region in order to perform the write logic high operation.

5 26. The method according to claim 19, wherein the second voltage potential applied to the second region and the third voltage potential applied to the body region are to perform a write logic high operation.

10 27. The method according to claim 26, wherein majority charge carriers are injected into the body region to perform the write logic high operation.

28. The method according to claim 19, wherein the second
15 voltage potential applied to the second region and the third voltage potential applied to the body region are positive voltage potentials in order to perform a read operation.

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