Abstract

A METHOD FOR INCREASING INTERCONNECT PACKING DENSITY IN INTEGRATED CIRCUITS

The present invention provides a method of forming closely spaced interconnections over a semiconductor structure using conventional photolithographic and etching methods and tools. The process which begins by providing an insulating layer 14 over a semiconductor structure10. A conductive layer and an isolation layer are sequentially formed over the insulating layer 14. The conductive layer is patterned forming spaced first interconnects 16 covered by isolation layer blocks 20. Sidewall spacers are then formed on the sidewalls of the first interconnects and the isolation layer blocks 20. A second conductive layer is formed over the resulting surface. The second conductive layer is planarized forming second interconnects 30 and excess conductive pieces 31 between the sidewall spacers. The excess conductive pieces 31 are intended to be removed. The planarization of the second conductive layer can be performed by etching back the second conductive layer or by chemical-mechanical polishing (CMP) back the second conductive layer. The excess conductive pieces 31 are removed using a photo/etch process leaving closely spaced first and second interconnects 16 30.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)