

CONTROL METHOD, SEMICONDUCTOR MEMORY, AND ELECTRONIC DEVICE

ABSTRACT

Embodiments of the present disclosure provide a control method, a semiconductor memory, and an electronic device. The method includes: decoding a third Operand (OP) in a third Mode Register (MR) and a fourth OP in a first MR; and in response to the semiconductor memory being in a preset test mode, controlling, in a case where the third OP meets a first decoding condition, the impedance of a Data Mask (DM) pin to be a first value; or controlling, in a case where the third OP meets a second decoding condition, the impedance of the DM pin to be a second value according to the fourth OP; wherein the third OP is configured to indicate whether the DM pin is a test object in the preset test mode, and the fourth OP is configured to indicate whether the DM pin is enabled.

[Fig. 6]