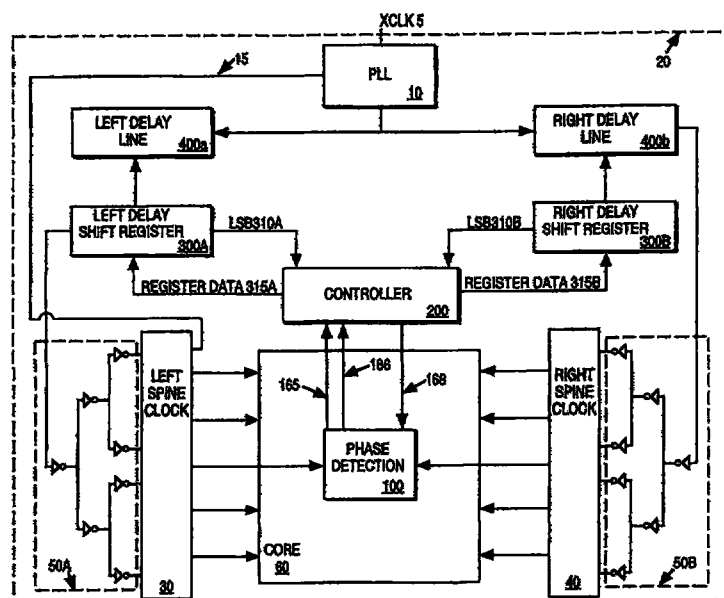




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(54) Title: METHOD AND APPARATUS FOR DESKEWING CLOCK SIGNALS



(57) Abstract

An apparatus (20) for deskewing clock signals in a synchronous digital system. The apparatus (20) contains a phase detector (100) that receives a plurality of clock signals and generates an output based on a phase relationship between those clock signals. A controller (200) then receives the output of the phase detector (100) and determines which one of the plurality of clock signals requires adjustment based on the output of the phase detector (100) and a bit from a delay shift register (300A, 300B). The controller (200) transmits a delay signal to one of a plurality of delay circuit (400a, 400b) which modifies the delay of the clock signal that the controller (200) determined to require adjustment.