Claims:

1. A microelectronic substrate, comprising:

at least one dielectric layer; and

at least one copper alloy conductive route including a first surface abutting the dielectric layer and an opposing second surface, wherein the at least one copper alloy conductive route comprises copper and an alloying metal of tungsten, molybdenum, or a combination thereof;

wherein the at least one copper alloy conductive route comprises at least one graded copper alloy conductive route comprising between about 90% and 100% copper proximate one of the graded copper alloy layer first surface and the graded copper alloy layer second surface, and between about 0% and 10% copper proximate the other of the graded copper alloy layer first surface and the graded copper alloy layer second surface.

2. The microelectronic substrate of claim 1, wherein the at least one copper alloy conductive route comprises between about 20% and 60% copper with the remainder being the alloying metal.

3. The microelectronic substrate of claim 1, wherein the copper of the at least one graded copper alloy conductive route has a substantially linear concentration gradient.

4. The microelectronic substrate of claim 1, wherein the at least one copper alloy conductive route further includes a co-deposition metal.

5. The microelectronic substrate of claim 4, wherein the co-deposition metal comprises nickel, cobalt, iron, or a combination thereof.

6. The microelectronic substrate of claim 4, wherein the at least one copper alloy conductive route comprises between about 20% and 60% copper with the remainder being the alloying metal and the co-deposition metal.

7. The microelectronic substrate of claim 4, wherein the at least one graded copper alloy conductive route comprises a concentration of copper proximate one of the graded copper alloy layer first surface and the graded copper alloy second surface between about 90% and 100%

and the remained being the alloying metal and the co-deposition metal, wherein the co-deposition metal has a concentration between about trace levels and 10% and, proximate the other of the graded copper alloy layer first surface and the graded copper alloy layer second surface, having a concentration of copper between about 0% and 10% and the remainder being the alloying metal and the co-deposition metal, wherein the co-deposition metal has a concentration is between about trace levels and 10%.

8. The microelectronic substrate of claim 1, wherein the at least one copper alloy conductive route is substantially trapezoidal shape in cross-section.

9. The microelectronic substrate of claim 1, further comprising a core layer having at least one conductive through via, where the at least one copper alloy conductive route is in electrical contact with the at least one conductive through via.

10. The microelectronic substrate of claim 1, further comprising a microelectronic die, where the microelectronic die is in electrical contact with the at least one conductive through via.

11. A computing device, comprising:
a board; and
a microelectronic component attached to the board,
wherein the microelectronic component includes a microelectronic substrate that comprises at least one dielectric layer; and
at least one copper alloy conductive route including a first surface abutting the dielectric layer and an opposing second surface, wherein the at least one copper alloy conductive route comprises copper and an alloying metal of tungsten, molybdenum, or a combination thereof, wherein the at least one copper alloy conductive route comprises at least one graded copper alloy conductive route comprising between about 90% and 100% copper proximate one of the graded copper alloy layer first surface and the graded copper alloy layer second surface, and between about 0% and 10% copper proximate the other of the graded copper alloy layer first surface and the graded copper alloy layer second surface.

12. The computing device of claim 11, wherein the at least one copper alloy conductive route comprises between about 20% and 60% copper with the remainder being the alloying metal.

13. The computing device of claim 11, wherein the copper of the at least one graded copper alloy conductive route has a substantially linear concentration gradient.

14. The computing device of claim 11, wherein the at least one copper alloy conductive route further comprises a co-deposition metal.

15. The computing device of claim 14, wherein the co-deposition metal comprises nickel, cobalt, iron, or a combination thereof.

16. The computing device of claim 14, wherein the at least one copper alloy conductive route comprises between about 20 to 60% copper with the remainder being the alloying metal and the co-deposition metal.

17. The computing device of claim 14, wherein the at least one graded copper alloy conductive route comprises a concentration of copper proximate one of the graded copper alloy layer first surface and the graded copper alloy second surface between about 90% and 100% and the remained being the alloying metal and the co-deposition metal, wherein the co-deposition metal has a concentration between about trace levels and 10% and, proximate the other of the graded copper alloy layer first surface and the graded copper alloy layer second surface, having a concentration of copper between about 0% and 10% and the remainder being the alloying metal and the co-deposition metal, wherein the co-deposition metal has a concentration is between about trace levels and 10%.

18. The computing device of claim 11, wherein the at least one copper alloy conductive route is substantially trapezoidal shape in cross-section.

19. The computing device of claim 11, further comprising a core layer having at least one conductive through via, where the at least one copper alloy conductive route is in electrical contact with the at least one conductive through via.

20. The computing device of claim 11, further comprising a microelectronic die, where the microelectronic die is in electrical contact with the at least one conductive through via.