What is claimed is:

1. A semiconductor structure (100) having at least one corner (100a) includes:

a carrier (110) having a carrier surface (111), the carrier surface (111) comprises a protection-layered disposing zone (111a) and a protection-layered exposing zone (111b) located outside the protection-layered disposing zone (111a);

a first protective layer (120) disposed at the protection-layered disposing zone (111a) and having a first surface (121), the first surface (121) comprises a first disposing zone (121a), at least one first anti-stress zone (121b) and a first exposing zone (121c) located outside the first disposing zone (121a) and the at least one first anti-stress zone (121b), the at least one first anti-stress zone (121b) is located at the at least one corner (100a);

a second protective layer (130) disposed at the first disposing zone (121a) and revealing the at least one first anti-stress zone (121b) and the first exposing zone (121c), the second protective layer (130) comprises a second surface (131), a first lateral surface (132) and a second lateral surface (133), the second surface (131) comprises a second disposing zone (131a) and a second exposing zone (131c) located outside the second disposing zone (131a), the first lateral surface (132) comprises a first bottom edge (132a), the second lateral surface (133) comprises a second bottom edge (133a), wherein a first extension line (L1) extended from the first bottom edge (132a) intersects with a second extension line (L2) extended from the second bottom edge (133a) to form a first base point (A1); and

a third protective layer (140) disposed at the second disposing zone (131a) and having a third lateral surface (141) and a fourth lateral surface (142), the third lateral surface (141) comprises a third bottom edge (141a), the fourth lateral surface (142) comprises a fourth bottom edge (142a), wherein the third bottom edge (141a) is projected on the first surface (121) of the first protective layer (120) to form a first projection line (P1) situated on the first surface (121), an extension line of the first projection line (P1) intersects with the second bottom edge (133a) of the second lateral surface (133) to form a first intersection point (I1), wherein the fourth bottom edge (142a) is projected on the first surface (121) of the first protective layer (120) to form a second projection line (I2) situated on the first surface (121), an extension line of the second projection

line (P2) intersects with the first bottom edge (132a) of the first lateral surface (132) to form a second intersection point (I2), and a zone formed by connecting the first base point (A1), the first intersection point (I1) and the second intersection point (I2) is the at least one first anti-stress zone (121b).

2. The semiconductor structure (100) in accordance with claim 1, wherein the first extension line (L1) is perpendicular to the second extension line (L2).

3. The semiconductor structure (100) in accordance with claim 1, wherein the second surface (131) of the second protective layer (130) further comprises at least one second anti-stress zone (131b) located at a corner of the second disposing zone (131a), the second exposing zone (131c) is located outside the at least one second anti-stress zone(131b), the third protective layer (140) reveals the at least one second anti-stress zone(131b), the at least one second anti-stress zone (131b) and the at least one first anti-stress zone (121b) are located at the at least one corner (100a), and the area of the at least one first anti-stress zone (121b) is not smaller than that of the at least one second anti-stress zone (131b).

4. The semiconductor structure (100) in accordance with claim 3, wherein the third bottom edge (141a) of the third lateral surface (141) comprises a first point (T1), the fourth bottom edge (142a) of the fourth lateral surface (142) comprises a second point (T2), wherein a third extension line (L3) extended from the third bottom edge (141a) and a fourth extension line (L4) extended from the fourth bottom edge (142a) intersect to form a second base point (A2), wherein a zone formed by connecting the second base point (A2), the first point (T1) and the second point (T2) is the at least one second anti-stress zone (131b).

5. The semiconductor structure (100) in accordance with claim 4, wherein a first distance (D1) is spaced apart between the second base point (A2) and the first point (T1), a second distance (D2) is spaced apart between the second base point (A2) and the second point (T2), and the first distance (D1) is equal to the second distance (D2).

6. The semiconductor structure (100) in accordance with claim 1, wherein the second protective layer (130) further comprises a first connection surface (134) connected to the first lateral surface (132) and the second lateral surface (133), and the first connection surface (134) is a flat surface or an arc surface.

7. The semiconductor structure (100) in accordance with claim 1, wherein the third protective layer (140) further comprises a second connection surface (143) connected to the third lateral surface (141) and the fourth lateral surface (142), and the second connection surface (143) is a flat surface or an arc surface.

8. A semiconductor structure (100) having at least one corner (100a) includes:

a carrier (110) having a carrier surface (111), the carrier surface (111) comprises a protection-layered disposing zone (111a) and a protection-layered exposing zone (111b) located outside the protection-layered disposing zone (111a);

a first protective layer (120) disposed at the protection-layered disposing zone (111a) and having a first surface (121), the first surface (121) comprises a first disposing zone (121a), at least one first anti-stress zone (121b) and a first exposing zone (121c) located outside the first disposing zone (121a) and the at least one first anti-stress zone (121b), the at least one first anti-stress zone (121b) is located at the at least one corner (100a);

a second protective layer (130) disposed at the first disposing zone (121a) and revealing the at least one first anti-stress zone (121b) and the first exposing zone (121c), the second protective layer (130) comprises a second surface (131), a first lateral surface (132), a second lateral surface (133) and a first connection surface (134) connected to the first lateral surface (132) and the second lateral surface (133), wherein the first connection surface (134) is a flat surface, the second surface (131) comprises a second disposing zone (131a) and a second exposing zone (131b) located outside the second disposing zone (131a), the first lateral surface (132) comprises a first bottom edge (132a), the second lateral surface (133) comprises a second bottom edge (133a), wherein a first extension line (L1) extended from the first bottom edge (132a) intersects with a second extension line (L2) extended from the second bottom edge (133a) to form a first base point (A1); and

a third protective layer (140) disposed at the second disposing zone (131a) and having a third lateral surface (141), a fourth lateral surface (142) and a second connection surface (143) connected to the third lateral surface (141) and the fourth lateral surface (142), wherein the second connection surface (143) is a flat surface, the third lateral surface (141) comprises a third bottom edge (141a), the fourth lateral surface (142)

comprises a fourth bottom edge (142a), wherein the third bottom edge (141a) is projected on the first surface (121) of the first protective layer (120) to form a first projection line (P1) situated on the first surface (121), an extension line of the first projection line (P1) intersects with the second bottom edge (133a) of the second lateral surface (133) to form a first intersection point (I1), wherein the fourth bottom edge (142a) is projected on the first surface (121) of the first protective layer (120) to form a second projection line (P2) situated on the first surface (121), an extension line of the second projection line (P2) intersects with the first bottom edge (132a) of the first lateral surface (132) to form a second intersection point (I2), and a zone formed by connecting the first base point (A1), the first intersection point (I1) and the second intersection point (I2) is the at least one first anti-stress zone (121b).

What is claimed is:

1. A semiconductor structure having at least one corner includes:

a carrier having a carrier surface, the carrier surface comprises a protection-layered disposing zone and a protection-layered exposing zone located outside the protection-layered disposing zone;

a first protective layer disposed at the protection-layered disposing zone and having a first surface, the first surface comprises a first disposing zone, at least one first anti-stress zone and a first exposing zone located outside the first disposing zone and the at least one first anti-stress zone, the at least one first anti-stress zone is located at the at least one corner;

a second protective layer disposed at the first disposing zone and revealing the at least one first anti-stress zone and the first exposing zone, the second protective layer comprises a second surface, a first lateral surface and a second lateral surface, the second surface comprises a second disposing zone and a second exposing zone located outside the second disposing zone, the first lateral surface comprises a first bottom edge, the second lateral surface comprises a second bottom edge, wherein a first extension line extended from the first bottom edge intersects with a second extension line extended from the second bottom edge to form a first base point; and

a third protective layer disposed at the second disposing zone and having a third lateral surface and a fourth lateral surface, the third lateral surface comprises a third bottom edge, the fourth lateral surface comprises a fourth bottom edge, wherein the third bottom edge is projected on the first surface of the first protective layer to form a first projection line situated on the first surface, an extension line of the first projection line

intersects with the second bottom edge of the second lateral surface to form a first intersection point, wherein the fourth bottom edge is projected on the first surface of the first protective layer to form a second projection line situated on the first surface, an extension line of the second projection line intersects with the first bottom edge of the first lateral surface to form a second intersection point, and a zone formed by connecting the first base point, the first intersection point and the second intersection point is the at least one first anti-stress zone.

2. The semiconductor structure in accordance with claim 1, wherein the first extension line is perpendicular to the second extension line.

3. The semiconductor structure in accordance with claim 1, wherein the second surface of the second protective layer further comprises at least one second anti-stress zone located at a corner of the second disposing zone, the second exposing zone is located outside the at least one second anti-stress zone, the third protective layer reveals the at least one second anti-stress zone, the at least one second anti-stress zone and the at least one first anti-stress zone are located at the at least one corner, and the area of the at least one first anti-stress zone is not smaller than that of the at least one second anti-stress zone.

4. The semiconductor structure in accordance with claim 3, wherein the third bottom edge of the third lateral surface comprises a first point, the fourth bottom edge of the fourth lateral surface comprises a second point, wherein a third extension line extended from the third bottom edge and a fourth extension line extended from the fourth bottom edge intersect to form a second base point, wherein a zone formed by connecting the second base point, the first point and the second point is

the at least one second anti-stress zone.

5. The semiconductor structure in accordance with claim 4, wherein a first distance is spaced apart between the second base point and the first point, a second distance is spaced apart between the second base point and the second point, and the first distance is equal to the second distance.

6. The semiconductor structure in accordance with claim 1, wherein the second protective layer further comprises a first connection surface connected to the first lateral surface and the second lateral surface, and the first connection surface is a flat surface or an arc surface.

7. The semiconductor structure in accordance with claim 1, wherein the third protective layer further comprises a second connection surface connected to the third lateral surface and the fourth lateral surface, and the second connection surface is a flat surface or an arc surface.