What is claimed is:

1. A semiconductor module, comprising:

a module substrate having a first side extending in a first direction, and a second side opposite to the first side;

a plurality of upper packages disposed on a top surface of the module substrate, and arranged in a plurality of rows extending in the first direction;

a plurality of tabs disposed on the top surface of the module substrate adjacent to the first side; and

a passive element disposed on the top surface of the module substrate,

wherein at least a portion of the passive element overlaps one of the upper packages when viewed in a plan view,

wherein the upper packages of a first row belonging to the plurality of rows are arranged to be shifted with respect to the upper packages of a second row belonging to the plurality of rows in the first direction, and

wherein a minimum distance between the plurality of tabs and the upper packages is less than a minimum distance between the second side of the module substrate and the upper packages.

2. The semiconductor module of claim 1, wherein the passive element comprises:

a first portion that overlaps the one of the upper packages; and

a second portion that does not overlap the upper packages.

3. The semiconductor module of claim 1 or claim 2, wherein the module substrate comprises:

a first region disposed between the plurality of tabs and the upper packages of the second row when viewed in the plan view;

a second region disposed between the upper packages of the first row and the upper packages of the second row; and

a third region disposed between another side of the module substrate and an outermost upper package of the first row and between the another side and an outermost upper package of the second row,

wherein the second portion of the passive element overlaps at least one of the first region, the second region or the third region of the module substrate when viewed in the plan view,

wherein the upper packages of the second row are closer to the plurality of tabs than the upper packages of the first row, and

wherein the another side of the module substrate extends in a different direction than the first direction and is adjacent to the first side.

4. The semiconductor module of any one of claims 1 to 3,

wherein each of the upper packages of the first row has a long axis parallel to a second direction,

wherein each of the upper packages of the second row has a long axis parallel to the first direction,

wherein the upper packages of the second row are closer to the plurality of tabs than the upper packages of the first row, and

wherein the second direction is substantially perpendicular to the first direction.

5. The semiconductor module of any of claims 1 to 4, further comprising:

a plurality of lower packages disposed on a bottom surface of the module substrate, and arranged in a plurality of additional rows extending in the first direction,

wherein the lower packages of a first row belonging to the plurality of additional rows are arranged to be shifted with respect to the lower packages of a second row belonging to the plurality of additional rows in the first direction.

6. The semiconductor module of any of claims 1 to 5, wherein each of the upper packages comprises:

a package substrate;

a memory chip mounted on the package substrate; and

a molding layer covering the memory chip on the package substrate.

7. The semiconductor module of any of claims 1 to 6, further comprising:

a connection portion disposed between the one upper package and the passive element,

wherein the passive element is connected to the one upper package through the connection portion.

8. A semiconductor module, comprising:

a module substrate having a first side, a second side opposite to the first side, a third side adjacent to the first side, and a fourth side opposite to the third side;

a plurality of tabs disposed on a top surface of the module substrate adjacent to the first side;

a plurality of memory packages mounted on the top surface of the module substrate and arranged in a plurality of rows extending in a first direction; and

a passive element mounted on the top surface of the module substrate,

wherein the first side and the second side of the module substrate extends in the first direction,

wherein at least a portion of the passive element overlaps one of the plurality of memory packages when viewed in a plan view,

wherein the plurality of memory packages comprise:

a plurality of first packages disposed in a first row belonging to the plurality of rows in the plan view; and

a plurality of second packages disposed in a second row belonging to the plurality of rows in the plan view, wherein the second packages are closer to the plurality of tabs than the first packages,

wherein a minimum distance between the plurality of tabs and the plurality of second packages is less than a minimum distance between the second side of the module substrate and the plurality of first packages,

wherein a minimum distance between the third side and the first packages is less than a minimum distance between the third side and the second packages, and

wherein a minimum distance between the fourth side and the first packages is less than a minimum distance between the fourth side and the second packages.

9. The semiconductor module of claim 8,

wherein some of the plurality of memory packages belong to a first group and others of the plurality of memory packages belong to a second group, and the memory packages of the second group are closer to the fourth side of the module substrate than the memory packages of the first group,

wherein the plurality of tabs comprise:

a plurality of first tabs adjacent to the third side; and

a plurality of second tabs closer to the fourth side than the first tabs,

wherein the first tabs are electrically connected to the memory packages of the first group, and the second tabs are electrically connected to the memory packages of the second group.

10. The semiconductor module of claim 9,

wherein the plurality of first packages are shifted with respect to the plurality of second packages in the first direction in the first group, and the plurality of first packages are shifted with respect to the plurality of second packages in an opposite direction to the first direction in the second group.

11. The semiconductor module of claim 9 or claim 10, further comprising:

a logic package mounted on the top surface of the module substrate,

wherein the logic package is disposed between the memory packages of the first group and the memory packages of the second group when viewed in the plan view.

12. The semiconductor module of claim 11, wherein the plurality of tabs further comprise:

a third tab disposed between the first tabs and the second tabs, wherein the third tab is electrically connected to the logic package.

13. The semiconductor module of any one of claims 9 to 12, further comprising:

a semiconductor device mounted on the top surface of the module substrate, wherein the semiconductor device comprises a serial presence detection (SPD) chip.

14. A semiconductor module, comprising:

a module substrate having a first side extending in a first direction and a second side extending in the first direction;

a plurality of tabs disposed on a top surface of the module substrate adjacent to the first side;

a plurality of memory packages mounted on the top surface of the module substrate and arranged in a plurality of rows extending in the first direction; and

a passive element mounted on the top surface of the module substrate,

wherein at least a portion of the passive element overlaps one of the memory packages when viewed in a plan view,

wherein a minimum distance between the plurality of tabs and the memory packages is less than a minimum distance between the second side of the module substrate and the memory packages,

wherein the memory packages comprise:

a plurality of first packages disposed in a first row belonging to the plurality of rows in the plan view; and

a plurality of second packages disposed in a second row belonging to the plurality of rows in the plan view,

wherein the second packages are closer to the plurality of tabs than the first packages, each of the first packages has a long axis parallel to a second direction that is substantially perpendicular to the first direction, and each of the second packages has a long axis parallel to the first direction.

15. The semiconductor module of claim 14, wherein the passive element comprises:

a first portion that overlaps the one memory package when viewed in the plan view; and

a second portion connected to the first portion, wherein the second portion does not overlap the memory packages.

16. The semiconductor module of claim 15, wherein the module substrate comprises:

a first region disposed between the plurality of tabs and the second packages when viewed in the plan view;

a second region disposed between the first packages and the second packages; and

a third region disposed between a third side of the module substrate and an outermost one of the first packages and between the third side and an outermost one of the second packages,

wherein the second portion of the passive element overlaps one of the first region, the second region or the third region of the module substrate when viewed in the plan view, and the third side is adjacent to the first side.

17. The semiconductor module of claim 14,

wherein the module substrate further has a third side adjacent to the first side, and a fourth side opposite to the third side, and

wherein a minimum distance between the third side and the first packages is less than a minimum distance between the third side and the second packages.

18. The semiconductor module of claim 17, wherein a minimum distance between the fourth side and the first packages is less than a minimum distance between the fourth side and the second packages.