

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
25 March 2004 (25.03.2004)

PCT

(10) International Publication Number
WO 2004/025457 A2

(51) International Patent Classification⁷: **G06F 9/00**

(21) International Application Number:
PCT/US2003/027716

(22) International Filing Date:
6 September 2003 (06.09.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/244,250 16 September 2002 (16.09.2002) US

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200
Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: **SPRANGLE, Eric**; 10290 SW Arborcrest
Way, Portland, OR 97225 (US). **ROHILLAH, Anwar**;
7162 NE Ronler Way, #2512, Hillsboro, OR 97124 (US).

(74) Agent: **MALLIE, Michael J.**; Blakely Sokoloff Taylor &
Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Ange-
les, CA 90025 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC,
SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA,
UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished
upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: PREFETCHING DATA IN COMPUTER SYSTEM

(57) Abstract: A method and apparatus to detect and filter out redundant cache line addresses in a prefetch input queue, and to adjust the detector window size dynamically according to the number of detector entries in the queue for the cache-to-memory controller bus. Detectors correspond to cache line addresses that may represent cache misses in various levels of cache memory.

WO 2004/025457 A2