(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 June 2004 (10.06.2004)

PCT

(10) International Publication Number
WO 2004/049445 A1

(51) International Patent Classification[7]: H01L 27/088, 27/092

(21) International Application Number: PCT/US2003/032782

(22) International Filing Date: 14 October 2003 (14.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/301,617 22 November 2002 (22.11.2002) US

(71) Applicant: ADVANCED MICRO DEVICES INC. [US/US]; One AMD Place, Mail stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: KRIVOKAPIC, Zoran; 2321 De Verona Place, Santa Clara, CA 95050 (US). AN, Judy, Xilin; 905 Raintree Court, San Jose, CA 95129 (US). LIN, Ming-Ren; 10970 Santa Teresa Drive, Cupertino, CA 95014 (US). WANG, Haihong; 34170 Donahue Terrace, Fremont, CA 94555 (US).

(74) Agent: COLLOPY, Daniel, R.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

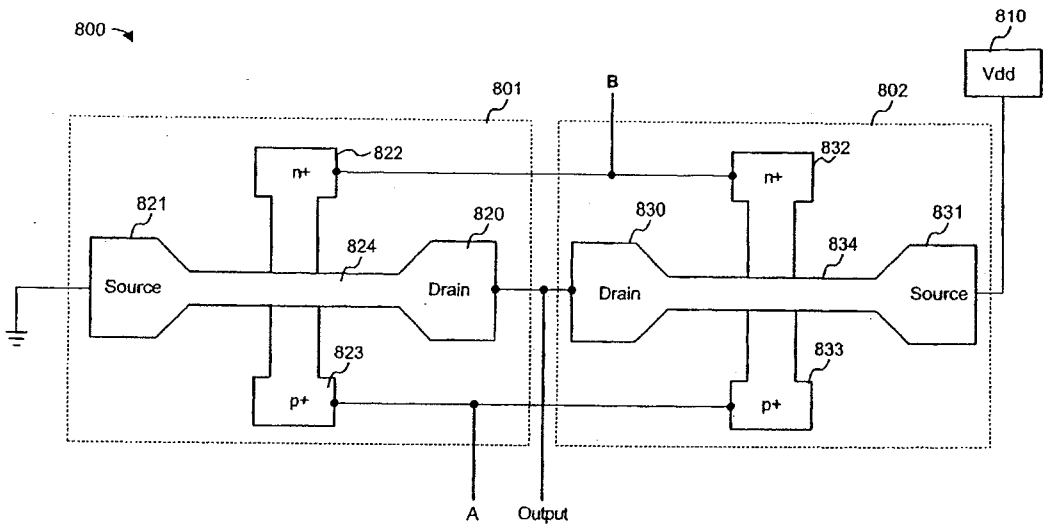
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: TWO TRANSISTOR NOR DEVICE



(57) Abstract: A NOR gate includes is constructed with two asymmetric FinFET type transistors (801, 802) instead of the conventional four-transistor NOR gate. The reduction in the number of transistors from four down to two allows for significant improvements in integrated semiconductor circuits.

WO 2004/049445 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.