so as to cross the memory region MA and the hookup areas HA1 and HA2. The stacked interconnect structure divided by two members SLTa corresponds to one block BLK.

[0040]

Each of the plurality of members SLTb is a plate-shaped insulator extending along the X direction. Three members SLTb are arranged in the Y direction between two adjacent members SLTa. Each member SLTb divides the stacked interconnect structure so as to cross the memory region MA and the hookup areas HA1 and HA2. The stacked interconnect structure divided by two members SLTb or one member SLTa and one member SLTb corresponds to one string unit SU.

[0041]

The planar layout of the memory cell array 16 described above is repeatedly arranged in the Y direction. The planar layout of the memory cell array 16 is not limited to the above-described planar layout. For example, the number of members SLTb disposed between two members SLTa is changed according to the number of string units SU included in one block BLK.

[0042]

1.4.2 Memory Area

Next, a configuration of the memory area of the memory cell array according to the embodiment is described.

[0043]

1.4.2.1 Planar Layout

FIG. 4 is a plan view showing an example of a detailed

The voltage VSS is applied to all bit lines BL other than the selected bit line BL9 (the non-selected bit lines BL0 to BL8 and BL10 to BL13). In this way, the potential difference |VS2 – VSS| = 1 V is applied between the source and the drain of all memory cell transistors MT coupled to the non-selected source lines BL0 to BL8 and BL10 to BL13. Therefore, a current may flow through the non-selected bit lines BL0 to BL8 and BL10 to BL13. However, since the current flowing through the non-selected bit lines BL0 to BL8 and BL10 to BL13 is independent of the read current flowing to the read target via the selected bit line BL9, the current can be ignored in a read operation.

[0099]

2.3 Erase Operation

Next, an erase operation in the memory device according to the embodiment is described.

[0100]

2.3.1 First Example

FIG. 11 is a circuit diagram showing an example of an erase operation in the memory device according to the embodiment. FIG. 11 illustrates an example of voltages applied to the word line WL, the bit line BL, and the source line SL in a case where memory cell transistor MT1 of the NOR string NS1 of the string unit SU0 is set as an erase target. In other words, FIG. 11 shows a case where the selected word line WL and the selected source line SL for specifying an erase target are WL1 and SL1,

target.

[0105]

As shown in FIG. 12, the voltage VSS is applied to all word lines WL0 to WL3. The voltage VERA is applied to all source lines SL0 to SLm. All bit lines BL0 to BL15 are set to an open state. Thus, FN tunneling can be generated in all memory cell transistors MT in one block BLK. Therefore, electrons can be extracted from the charge storage films 32b of all memory cell transistors MT in the block BLK to be erased.

[0106]

3. Manufacturing Method

FIGS. 13 to 19 each illustrate an example of a cross-sectional structure of the memory cell array according to the embodiment during manufacturing. The cross-sectional structures illustrated in FIGS. 13 to 16 show regions corresponding to FIG. 8. The cross-sectional structures illustrated in FIGS. 17 to 19 show regions corresponding to FIG. 5. An example of a manufacturing process of the stacked wiring structure in the memory cell array 16 in the memory device 3 is described hereinafter.

[0107]

First, as shown in FIG. 13, a stacked structure including the sacrificial member SM is formed. Specifically, the insulating layer 30 is formed on the semiconductor substrate 20. The multilayer structure corresponding to the layers L0 to L3 is stacked on the

CLAIMS

1. A memory device comprising:

a first semiconductor layer, a first conductive layer, a second semiconductor layer, and a second conductive layer that are arranged in this order in a first direction, spaced apart from each other;

a first semiconductor film extending in the first direction, being in contact with the first semiconductor layer and the second semiconductor layer, and intersecting the first conductive layer and the second conductive layer;

a first memory film provided between the first conductive layer and the first semiconductor film; and

a second memory film provided between the second conductive layer and the first semiconductor film.

2. The memory device according to claim 1, wherein

the first memory film and the second memory film are a charge storage film.

3. The memory device according to claim 2, wherein

the charge storage film includes silicon nitride.

4. The memory device according to claim 1, wherein

the first memory film and the second memory film are a ferroelectric film.

5. The memory device according to claim 4, wherein

the ferroelectric film includes at least one material selected from lead zirconate titanate, strontium tantalate bismuthate, and polyvinylidene fluoride-trifluoroethylene (P(VDF-TrFE)).

6. The memory device according to claim 1, wherein the first semiconductor layer and the second semiconductor layer contain an N-type impurity.

7. The memory device according to claim 6, wherein the first semiconductor film contains an N-type impurity.

8. The memory device according to claim 7, wherein a concentration of the N-type impurity contained in the first semiconductor layer and the second semiconductor layer is equal to or higher than a concentration of the N-type impurity contained in the first semiconductor film.

9. The memory device according to claim 6, wherein the first semiconductor film contains a P-type impurity.

10. The memory device according to claim 1, wherein each of the first semiconductor layer, the first conductive layer, the second semiconductor layer, and the second conductive layer surrounds the first semiconductor film when viewed in the first direction.

11. The memory device according to claim 1, further comprising:

a second semiconductor film extending in the first direction, being in contact with the first semiconductor layer and the second semiconductor layer, intersecting the first conductive layer and the second conductive layer, and provided apart from the first semiconductor film.

12. The memory device according to claim 1, further

comprising:

a third semiconductor layer, a third conductive layer, a fourth semiconductor layer, and a fourth conductive layer that are arranged in this order in the first direction, spaced apart from each other;

an insulating film extending in the first direction and provided between the first semiconductor layer and the third semiconductor layer, between the first conductive layer and the third conductive layer, between the second semiconductor layer and the fourth semiconductor layer, and between the second conductive layer and the fourth conductive layer;

a third semiconductor film extending in the first direction, being in contact with the third semiconductor layer and the fourth semiconductor layer, and intersecting the third conductive layer and the fourth conductive layer;

a third memory film provided between the third conductive layer and the third semiconductor film; and

a fourth memory film provided between the fourth conductive layer and the third semiconductor film.

13. A memory device comprising:

a first memory cell transistor and a second memory cell transistor coupled in series;

a first source line electrically coupled to a first end of the first memory cell transistor;

a first bit line electrically coupled to a second end of the first memory cell transistor and a first end of the

second memory cell transistor;

a second bit line electrically coupled to a second end of the second memory cell transistor;

a first word line electrically coupled to a gate of the first memory cell transistor; and

a second word line electrically coupled to a gate of the second memory cell transistor.

14. The memory device according to claim 13, further comprising:

a third memory cell transistor and a fourth memory cell transistor coupled in series;

a third bit line electrically coupled to a second end of the third memory cell transistor and a first end of the fourth memory cell transistor; and

a fourth bit line electrically coupled to a second end of the fourth memory cell transistor,

wherein

a first end of the third memory cell transistor is electrically coupled to the first source line,

a gate of the third memory cell transistor is electrically coupled to the first word line, and

a gate of the fourth memory cell transistor is electrically coupled to the second word line.

15. The memory device according to claim 13, further comprising:

a fifth memory cell transistor and a sixth memory cell transistor coupled in series; and

a second source line electrically coupled to a first end of the fifth memory cell transistor,

wherein

a second end of the fifth memory cell transistor and a first end of the sixth memory cell transistor are electrically coupled to the first bit line;

a second end of the sixth memory cell transistor is electrically coupled to the second bit line,

a gate of the fifth memory cell transistor is electrically coupled to the first word line, and

a gate of the sixth memory cell transistor is electrically coupled to the second word line.

16. The memory device according to claim 13, further comprising:

a seventh memory cell transistor having a first end coupled in series to the second end of the second memory cell transistor;

a fifth bit line electrically coupled to a second end of the seventh memory cell transistor; and

a third word line electrically coupled to a gate of the seventh memory cell transistor,

wherein in a write operation on the second memory cell transistor, the memory device is configured to:

apply a first voltage to the first word line;

apply a second voltage higher than the first voltage to the second word line; and

apply a third voltage lower than the first

voltage to the third word line,

in a write operation on the seventh memory cell transistor, the memory device is configured to:

apply the first voltage to the first word line and the second word line; and

apply the second voltage to the third word line.

17. The memory device according to claim 13, further comprising:

a seventh memory cell transistor having a first end coupled in series to the second end of the second memory cell transistor;

a fifth bit line electrically coupled to a second end of the seventh memory cell transistor; and

a third word line electrically coupled to a gate of the seventh memory cell transistor,

wherein in a read operation on the second memory cell transistor, the memory device is configured to:

apply a fourth voltage to the first word line;

apply a fifth voltage lower than the fourth voltage to the second word line; and

apply a sixth voltage lower than the fifth voltage to the third word line,

in a read operation on the seventh memory cell transistor,

apply the fourth voltage to the first word line and the second word line; and

apply the fifth voltage to the third word line.

18. The memory device according to claim 13 configured to:

in an erase operation on the second memory cell transistor,

apply a seventh voltage to the first source line;

set the first bit line and the second bit line to an open state;

apply the seventh voltage to the first word line or set the first word line to an open state; and

apply an eighth voltage lower than the seventh voltage to the second word line.

19. The memory device according to claim 13 configured to:

in an erase operation on the first memory cell transistor and the second memory cell transistor,

apply a seventh voltage to the first source line;

set the first bit line and the second bit line to an open state; and

apply an eighth voltage lower than the seventh voltage to the first word line and the second word line.