READ CHANNEL IC FOR DUAL PLL SOLUTION

ABSTRACT OF THE INVENTION

The present invention discloses a fully integrated data synchronization circuit for a disk drive read channel system. The data synchronization system comprises dual data synchronizers to provide read reference clocks. Dual PLL circuits (405,408) are coupled to the data synchronizers to provide a stable reference frequency to data synchronizers. One of the two data synchronizers (406,407) is used to obtain leading edge data, while the other is for trailing edge data. Each PLL circuit comprises a phase detector (501,506), a charge pump (502,507), and a VCO (503,508). A loop filter is used in conjunction with a charge pump to control loop characteristics of the PLLs.In an idle mode, one of the PLLsis used as a time base generator to provide a stable reference frequency to data synchronizers. Once data synchronizers achieve lock using the stable reference frequency and switch over to read data, the time base generator PLL is switched over to function as a data synchronizer PLL in a read mode. Thus, one of the PLLs is used as both time base generator and data synchronizer PLL, thereby eliminating the need for extra PLL circuitry and requiring only two PLL circuits to support time base generation and data synchronization.

FIGURE 4