

What is claimed is:

1. A semiconductor structure, comprising: a semiconductor fin disposed above a substrate and having a length in a first direction; a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction, wherein the gate structure has an uppermost surface; and a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure, and wherein the pair of gate edge isolation structures has an uppermost surface co-planar with or above the uppermost surface of the gate structure.
2. The semiconductor structure of claim 1, further comprising: source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.
3. The semiconductor structure of claim 1, further comprising: a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin; a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.
4. The semiconductor structure of claim 3, further comprising: a local interconnect disposed above and electrically coupling the first and second gate structures.
5. The semiconductor structure of claim 4, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

6. The semiconductor structure of claim 3, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.
7. The semiconductor structure of claim 1, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.
8. The semiconductor structure of claim 1, wherein the pair of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.
9. A semiconductor structure, comprising: a semiconductor fin disposed above a substrate and having a length; alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and a gate local interconnect disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.
10. The semiconductor structure of claim 9, further comprising: a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.
11. The semiconductor structure of claim 9, further comprising: a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.
12. The semiconductor structure of claim 11, further comprising: a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.
13. The semiconductor structure of claim 9, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.
14. The semiconductor structure of claim 9, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

15. A semiconductor structure, comprising: a semiconductor fin disposed above a substrate and having a length; alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and a trench contact local interconnect disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

16. The semiconductor structure of claim 15, further comprising: a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

17. The semiconductor structure of claim 15, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

18. The semiconductor structure of claim 15, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

19. A method of fabricating a semiconductor structure, the method comprising: forming first and second parallel semiconductor fins above a substrate; forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin; forming an isolation structure between the dummy spacers of the first and second semiconductor fins; removing the dummy spacers; and forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

20. The method of claim 19, further comprising: forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin, wherein the first and pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

21. The method of claim 19, further comprising: subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

22. The method of claim 19, wherein forming the dummy spacers comprises forming and etching a polycrystalline silicon layer.

23. The method of claim 19, wherein forming the isolation structure comprises depositing and planarizing a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

24. The method of claim 19, wherein forming one or both of the first and second replacement gate structures comprises forming a high-k gate dielectric layer and a metal gate electrode.

25. The method of claim 19, further comprising: forming a local interconnect above and electrically coupling the first and second replacement gate structures.

26. An integrated circuit structure, comprising: a first fin comprising silicon, the first fin having a longest dimension along a first direction; a second fin comprising silicon, the second fin having a longest dimension along the first direction; an isolation material between the first fin and the second fin; a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode; a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode; a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

27. The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.

28. The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.

29. The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

30. The integrated circuit structure of claim 29, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

31. The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

32. The integrated circuit structure of claim 26, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

33. The integrated circuit structure of claim 32, further comprising: a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

34. The integrated circuit structure of claim 33, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

35. The integrated circuit structure of claim 33, further comprising: a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

36. The semiconductor structure of claim 1, wherein the uppermost surface of the pair of gate edge isolation structures is co-planar with the uppermost surface of the gate structure.

37. The semiconductor structure of claim 1, wherein the uppermost surface of the pair of gate edge isolation structures is above the uppermost surface of the gate structure.

38. A semiconductor structure, comprising: a semiconductor fin disposed above a substrate and having a length in a first direction; a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode; and a pair of gate edge isolation structures centered with the semiconductor fin, wherein a

first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

39. The semiconductor structure of claim 38, further comprising: source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

40. The semiconductor structure of claim 38, further comprising: a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin; a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

41. The semiconductor structure of claim 40, further comprising: a local interconnect disposed above and electrically coupling the first and second gate structures.

42. The semiconductor structure of claim 41, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

43. The semiconductor structure of claim 40, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

44. The semiconductor structure of claim 38, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

45. The semiconductor structure of claim 38, wherein the pair of gate edge isolation structures

comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.