Claims

1. Apparatus for processing an audio signal comprising a sequence of blocks ~~(114)~~ of spectral values:

a processor ~~(100)~~ for processing the sequence of blocks using at least one modification value ~~(102)~~ for a first block to obtain aliasing-reduced or aliasing-free first result signal in an overlap range ~~(170)~~ and using at least one second different modification value ~~(106)~~ for a second block of the sequence of blocks to obtain an aliasing-reduced or aliasing-free second result signal ~~(108)~~ in the overlap range ~~(170)~~; and

a combiner ~~(110)~~ for combining the first result signal ~~(104)~~ and the second result signal ~~(108)~~ in the overlap range ~~(170)~~ to obtain a processed signal ~~(112)~~ for the overlap range ~~(170)~~,

wherein the processor ~~(100)~~ comprises:

a modifier ~~(510, 509, 508, 507)~~ for modifying the first block of the sequence using the at least one first modification value ~~(102)~~ to obtain a first modified block ~~(551)~~, for modifying the second block of the sequence using the at least one second modification value ~~(106)~~ to obtain a second modified block ~~(552)~~, for modifying the second block using the second at least one first modification value ~~(102)~~ to obtain a third modified block ~~(553)~~ and for modifying the first block using the at least one second modification value ~~(106)~~ to obtain a fourth modified block ~~(554)~~;

a spectrum-time converter ~~(501, 502, 503, 504)~~ for converting the first to fourth modified blocks into a corresponding time representation ~~(561, 562, 563, 564)~~; and

an overlap-adder ~~(505, 506)~~ for overlap-adding time representations ~~(561, 563)~~ of the first and third modified blocks ~~(551, 553)~~ to obtain the first result signal ~~(104)~~ and for overlap-adding time representations ~~(562, 564)~~ of the second and fourth modified blocks ~~(552, 554)~~ to obtain the second result signal ~~(108)~~.

2. Apparatus in accordance with claim 1, wherein the combiner ~~(110)~~ is configured to combine the first result signal ~~(104)~~ and the second result signal ~~(108)~~ by fading

out ~~(520)~~ the first result signal and by fading in ~~(521)~~ the second result signal and adding both signals ~~(522)~~.

3. Apparatus of one of the preceding claims,

wherein the processor ~~(100)~~ is configured to perform an inverse modified discrete cosine transform operation in performing a spectrum-time conversion.

4. Apparatus of one of the preceding claims,

wherein the processor ~~(100)~~ is configured to perform an overlap-add processing operation ~~(505, 506)~~ in calculating the first and second result signals in the overlap range, and

wherein the combiner ~~(110)~~ is configured to combine the first and second result signals in a combining range, wherein the combining range is identical to the overlap range ~~(170)~~.

5. Apparatus of one of the preceding claims,

wherein the combiner ~~(110)~~ is configured to perform a cross-fade function, wherein the cross-fade function comprises a fade-out part ~~(520)~~ and a fade-in part ~~(521)~~, wherein a sum ~~(522)~~ of a weighting coefficient of the fade-out part ~~(520)~~ and of a weighting coefficient of the fade-in part ~~(521)~~ for a sample in a cross-fade range is constant.

6. Apparatus of one of the preceding claims,

wherein the combiner ~~(110)~~ is configured to perform a cross fade operation, wherein the cross-fade operation comprises a monotonically decreasing fade-out part ~~(520)~~ and a monotonically increasing fade-in part ~~(521)~~.

7. Apparatus of one of the preceding claims,

wherein the processor ~~(100)~~ is configured for applying a bandwidth filling operation ~~(332)~~ having a patching function to patch spectral values from a source range ~~(300)~~ to a target range ~~(334)~~, and

wherein the processor ~~(100)~~ is configured for applying the patching function in calculating the first and second result signals.

8. Apparatus of one of the preceding claims, further comprising:

a patcher ~~(332)~~ for generating the first block in a bandwidth filling range using spectral values from a different frequency range in accordance with a patching function for the first block, and for generating the second block in a bandwidth filling range having spectral values for a different frequency region in accordance with a patching function associated with the second block.

9. Apparatus of one of the preceding claims,

wherein the processor ~~(100)~~ is configured to perform a multiplication operation to the first and second blocks using the gain functions as modification values.

10. Apparatus of one of the preceding claims,

wherein the processor ~~(100)~~ is configured to process the sequence of blocks, wherein the first block is adjacent in time with the second block, and wherein the first and second blocks being adjacent in time having an overlap equaling 55% to 45% of a time portion.

11. Apparatus of one of the preceding claims,

wherein the processor ~~(100)~~ is configured to apply a spectral-time conversion operation having a spectrum-time transform part ~~(212)~~ and a synthesis window part ~~(214)~~ applied to an output of the spectrum-time transform part ~~(212, 213)~~.

12. Apparatus of one of the preceding claims,

wherein the processor (100) is configured to operate using modification values varying over time and frequency.

13. Apparatus of one of the preceding claims, wherein the processor is configured for performing lapped transforms having an overlapping range, and wherein the processor is configured for only performing operations influencing values in the overlapping range and for not performing operations not influencing values in the overlapping range.

14. Method for processing an audio signal comprising a sequence of blocks (114) of spectral values:

processing (100) the sequence of blocks using at least one modification value (102) for a first block to obtain aliasing-reduced or aliasing-free first result signal in an overlap range (170) and using at least one second different modification value (106) for a second block of the sequence of blocks to obtain an aliasing-reduced or aliasing-free second result signal (108) in the overlap range (170); and

combining (110) the first result signal (104) and the second result signal (108) in the overlap range (170) to obtain a processed signal (112) for the overlap range (170),

wherein the processing (100) comprises:

modifying the first block of the sequence using the at least one first modification value (102) to obtain a first modified block (551),

modifying the second block of the sequence using the at least one second modification value (106) to obtain a second modified block (552),

modifying the second block using the second at least one first modification value (102) to obtain a third modified block (553),

modifying the first block using the at least one second modification value (106) to obtain a fourth modified block (554),

converting the first to fourth modified blocks into a corresponding time representation (561, 562, 563, 564);

overlap-adding time representations (561, 563) of the first and third modified blocks (551, 553) to obtain the first result signal (104) and

overlap-adding time representations (562, 564) of the second and fourth modified blocks (552, 554) to obtain the second result signal (108).

15. Computer program for performing, when running on a computer or a processor, the method of claim 14.