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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Information Control System

We, SHARP KABUSHIKI KAISHA formerly Hayakawa Denkikogyo Kabushiki Kaisha, a Japanese Company, of 22—22 Nagaike-cho, Abeno-ku, Osaka-shi, Osaka-fu, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an information control system, and especially to an electronic desk calculator such as a calculator having a dynamic memory in which information is to be stored.

A dynamic memory as herein described means a memory in which memory elements each having such properties that the stored energy attenuates with time and finally disappears are connected in cascade, before said energy or information stored disappears a clock pulse is applied so that the stored information is transferred to the memory element of the next stage, and thus the information is transferred, being synchronized with the clock pulses in order. It is necessary when providing long time duration storage to form a circulating loop between the first stage and the final stage. The synchronization provided by the clock pulse is restricted by the storing capability of the memory element or the time during which the memory element can maintain the information, and the propagation speed of the information is determined by the period of the clock pulse. In contrast to this dynamic memory there is static memory. The static memory comprises memory elements which are capable of maintaining the energy level of the stored information irrespective of time and which are connected in cascade. By the way, the memory herein-described includes such register of a small capacity for storing information constituted of from a several digits to some ten digits.

[*Price 5s. 0d. (25p)*]

In the conventional dynamic memory having a circulating loop such as the one constituted of an ultra-sonic delay line, the delay line itself has its specific propagation speed, and it is considered impossible to vary the propagation speed of the information digitally or discontinuously by means of external signal. Therefore, in such dynamic memory as the above, there has been no way found to perform shift control utilizing the propagation speed of the information.

In practice, accordingly, in such case as the above, an extra buffer register is provided. And, in the case of a register in which the information is shifted rightwardly or to lower place digit upon the introduction of the switching signal and if a leftward shift is desired, the information is transferred from the least significant digit LSD of the register through the buffer register to the most significant digit MSD of the register. In other words, two kinds of circulating loops are provided so that the propagation distance of the information is varied in order to control the shift. By such method as the above, however, an extra buffer register is required, and it is necessary further to properly switch the circulating loops in order to obtain a desired result.

Now, amidst the recent trend of semiconductor integration, the MOS type field effect transistor is receiving a footlight as an element quite suitable for said purpose.

In the MOS type field effect transistor, there is an inherent parasitic capacitance (about 1—2 pF, in fact) between its gate electrode and its substrate because of its structure, and by storing information to be memorized in the form of an electric charge in said gate internal capacitance said transistor can be utilized in an information provisional memory circuit. The stored charge is not discharged promptly because the discharging

path from the gate internal capacitance to the ground exhibits a very high impedance. In this respect, the MOS type field effect transistor has a far higher storing capability compared to the general junction transistor which has some storing operation with respect to minority carriers.

However, as the stored charge is gradually lost due to the leakage current of the gate internal capacitance it is necessary to introduce the clock pulse in order to transfer the stored information to the MOS type field effect transistor of the next stage.

In practice, two MOS type field effect transistors per one bit of the memory are prepared, depending upon the number of desired bits a plurality of the MOS type field effect transistors are further prepared and connected in cascade, then switching means are provided between the stages, and synchronizing clock pulses are introduced thereto thus constituting a dynamic memory. However, in order to prevent the information introduced into the first stage from reaching the last stage instantaneously different kinds of clock pulses having mutually different phase are used for controlling the path between fore stage and rear stage within same bit and the path between the rear stage in a certain bit and the fore stage of the adjacent bit ON and OFF. Needless to say, the duty ratio (duty factor) of the clock pulse is restricted by the memory maintaining capability of the MOS type field effect transistor, and the period of the clock pulse determines the propagation speed of the information.

According to one aspect of the invention there is provided an information control system, comprising a dynamic memory in which a plurality, corresponding to the desired number of bits to be stored of MOS type field effect transistors, each having a gate internal capacitance for temporarily storing an electrical charge which corresponds to a bit of information, are connected in cascade and in which said stored information is shifted in sequence upon introduction of clock pulses each before said electric charges disappear, means for generating periodically and successively said clock pulses which transfer said information and which control the propagation of said information, means for generating instruction signals which designate the kind of effective shift operation to be performed, and control means for varying for a specific period of time and within the time during which said information stored in said MOS type field effect transistor can be sustained the occurrence of said clock pulse to be applied to said dynamic memory corresponding to said kind of instruction and thereby for causing said propagation of said information to be varied and desired effective shift operation performed.

According to a further aspect of the invention there is provided an information control system in an electronic computer, provided with a dynamic register in which a plurality, corresponding to the desired number of bits to be stored, of MOS type field effect transistors, each having a gate internal capacitance for temporarily storing an electric charge which corresponds to a bit of information, are connected in cascade and which upon introduction of successive clock pulses before stored electric charges disappear shifts said information in order in synchronization with said clock pulses, an arithmetic unit for processing the arithmetical operation of said numerical information in said register to provide a result, an operation generator for generating instructions necessary for the arithmetical operation processes, a timing generator for specifying weights of digits of the numerical information, and a control device for discriminating between respective states of the timing signals, control means responsive to operation control instructions and clock pulses to modify at least one clock pulse of said plurality of clock pulses for only a specific period.

The present invention is based upon a dynamic memory which is constituted of the MOS type field effect transistors as mentioned above, and in light of the facts that the storing capability of the MOS type field effect transistor is as long as about several seconds and that the period between the occurrence of the clock pulses can be varied within the range of from less than a microsecond to one second.

More specifically, time T which is required by the contents of the register to circulate one round under normal conditions (propagation time between bits multipled by the number of bits) is used as a reference value of one word time, and if the occurrence of clock pulses is varied during said one word time the contents of the register before and after said variation become different from the contents of the first time of each one word time. This means that leftward shift and rightward shift are performed.

In order that the invention may be clearly understood and readily carried into effect apparatus in accordance therewith will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a block diagram of a complete system embodying this invention;

Figure 2 is a time chart representing the phase relationship of various timing signals;

Figure 3 and Figure 4 are time charts representing a shift control state of a memory;

Figure 5 is a block diagram representing a fundamental structure of a dynamic memory;

Figure 6 is a time chart representing phase relation of switching signals;

Figure 7 and Figure 8 are diagrams repre-

senting operational states of respective parts of the dynamic memory;

Figure 9 is a time chart representing clock pulses after variable frequency control in the case of right-hand shift operation;

Figure 10 is a circuit diagram representing an embodiment of dynamic memory circuit;

Figure 11 is a circuit diagram representing another embodiment of memory circuit;

Figure 12 is a circuit diagram representing a further embodiment of memory circuit;

Figure 13 is a time chart representing the phase relationship of three phase clock pulses.

Referring to Figure 1, X and Y are dynamic registers in each of which memory elements or MOS type field effect transistors having timely restricted memory function are connected in cascade, and information stored therein is transferred upon introduction of synchronizing clock pulses. Their memory capacities are N_x and N_y respectively. Herein, 1 digit is constituted of n bits, and in the case of 8-4-2-1 code, for example, 1 digit of decimal number is represented by 4 bits of binary number. It is defined that $N=N_x$ when $N_x \geq_y$ and $N=N_y$ when $N_y \geq N_x$ and a N digit time is defined as a time of one word-length.

AU is an arithmetic unit executing addition and subtraction with respect to contents transmitted from X and Y, having an output to be returned to the memory X. PG is a pulse generator for preparing a fundamental signal and a generated output thereof is supplied to a timing signal generator TC and to a synchronizing signal control SC. Further, as abovementioned, since there are required plural kinds of clock pulses of mutually different phase for the dynamic register three kinds of clock pulses ϕ_1, ϕ_2 and ϕ_3 which are based upon a fundamental signal are produced here. However, depending upon the type of the memory circuit to be used the clock pulse ϕ_3 may not be required. The term synchronizing signal as used in the subsequent explanation means the group of said plurality of clock pulses as a whole. TC generates a bit time signal and a digit time signal in response to the fundamental signal from the pulse generator PG. OG is an operation generator having as the longest time of its respective information processing (circulation, left-hand shift, right-hand shift and arithmetic operation) the time of one word-length and selecting and generating a desired instruction in response to an operation instruction from input and output devices (not shown), so making said time of the word-length a unit. One instruction is derived over the time of one word-length. SC in response to the instruction Q given from the operation generator OG selects the clock pulse ϕ_1 which especially is to receive a control out of the plurality of the clock pulses ϕ_1, ϕ_2 and ϕ_3, further in response to the contents of the instruction Q performs a control for a specific period of time to produce controlled clock pulses $X\phi_1$ and $Y\phi_1$ to be introduced into the memories X and Y respectively, and supplies said clock pulses $X\phi_1$ and $Y\phi_1$ to the memories X and Y so that the instruction is accomplished. The clock pulses ϕ_2 and ϕ_3 without receiving any control are directly supplied to the memories X and Y from the synchronizing control SC. The reason therefor will be explained later. The control of the clock pulse ϕ_1 as explained above means that the propagation speed of the information is varied. G1, G2, G3 and G4 are logic gates for controlling numerical information and synchronizing signals to be supplied to the respective memories X and Y.

Referring now to Figure 2, t_1, t_2 ... t_n are bit time signals and T_1, T_2, ... T_N are digit time signals. As shown in the drawing, the bit time signals are derived in the order t_1—t_2— ... t_n—t_1 and the digit time signals are derived in the order T_1—T_2— ... T_N—T_1. A period from t_1 to t_n is one digit time. A new digit time begins from the next t_1 and continues to t_n. The subsequent digit time begins from the subsequent t_1. These timing signals are derived from the timing signal generator TC as described above. A fundamental synchronizing signal t_0 may be an output of the pulse generator PG converted by a suitable converter or may be the output of the pulse generator itself. As described above, an instruction Q is derived over a time of one word-length and continues from T_1 to T_N. The drawing is concerned with n=4, wherein the high level of the waveform corresponds to "1" and the low level corresponds to "0".

Now, a shift operation of the memory will be described referring to Figures 3 and 4. The information stored in the Registers X and Y are generally shifted to the right by applying synchronizing signals derived from the generator SC to the registers X and Y. That is, they are shifted by one bit by one synchronizing signal and by n-bits (one digit) by n synchronizing signals. Accordingly, each stored information is shifted to the right by P digits by derivation from nP synchronizing signals. When the memory content is required to be shifted to the right by one digit, it is sufficient to put P=1, and it is sufficient to put P=N when the information is required to be circulated or other information is required to be newly stored. When the memory content is required to be shifted to the left, the least significant (right end) output of the register is used as the input thereof, putting P=N−1.

From the above description, in the synchronous register continuously circulating information in a dynamic fashion at a period of the time of one word-length, if the synchronizing signals are interrupted only for a

period of one digit time within an arbitrary time of one word-length, the content of the register can be shifted to the left. On the other hand, if the synchronizing signals are interrupted for the period other than that said digit time whereby the circulation path is cut off for said period, it is shifted to the right by one digit. Immediately after a desired shift control is over and one word time has elapsed, the numeral values in the register respectively take predetermined digit positions. In other words, each of the numeral values after a rightward shift takes adjacent lower place digit position. The weight of said digit position is of course designated by the digit time signal from the timing signal generator TC.

Considering the condition under which the synchronizing signal (clock pulse ϕ_1, in fact) receives a control corresponding to the contents of the instruction for such as rightward shift, leftward shift or circulation, the clock pulses T_r, T_l and T_a which are the synchronizing signals to be introduced into the register after the receipt of control can be represented by the following equations, putting $N=N_x$.

$$T_r=Q_r.t_0.T_k$$

$$T_l=Q_l.t_0.\overline{T_{k'}}$$

$$T_a=\overline{Q_r}.\overline{Q_l}.t_0$$

where Q_r is a right shift instruction, Q_l is a left shift instruction and T_k and $T_{k'}$ are digit times. When both right and left shift instructions are not generated the fundamental synchronizing signal t_0 is always supplied and the content of the register continues to circulate in dynamic fashion at a period of the time of one word-length synchronizing with said fundamental synchronizing signal t_0. The synchronizing signal t_0 hereinmentioned represents the group of three kinds of clock pulses ϕ_1, ϕ_2 and ϕ_3 as explained before, and these are of the state that frequency control is not yet applied. Thus, the state of circulation is not shown in the time chart. The clock pulse t_0 is periodically and consecutively generated, and in order to vary the way in which information is shifted a logic gate is provided within the transfer path to the dynamic memory, that is within the synchronizing signal control SC, and thereby the supply of the clock pulse to the dynamic memory is temporarily intermitted for a specific period of time. Three inputs to the logic gate are the instructions Q_r and Q_l from the operation generator OG, and digit time signals T_k and $T_{k'}$ from the timing signal generator TC and the clock pulse t_0 from the pulse generator PG (especially, in practice, the clock pulse ϕ_1 out of the group) as explained before.

The time chart of Figure 3 represents a synchronizing signal derived from a right shift instruction Q_r and the states of storage in the register, and a_1, a_2 ... a_n represent digits in the memory.

Since the synchronizing signal is passed to the memory only during a period of the digit time T_k, n signals are derived and the stored content of the register X which has been in the state (A) before the time of one word-length starts changes to the state (B). It should be noted, however, if the digit time signal T_k is present during 2 digit time the information is shifted rightwardly by two digits.

The time chart of Figure 4 represents a synchronizing signal derived by a left shift instruction Q_l and the states of the storage in the register.

Since the synchronizing signal is not passed to memory only during a period of the digit time $T_{k'}$, the stored content is shifted by one digit to the right during periods of the respective digit times but are not shifted during the period of the digit time $T_{k'}$. The shift operation is executed again during a period of the next digit time $T_{k'+}$ and eventually when the time of one word-length ends, the information in the register is shifted to the left as shown in the lowermost part of the drawing.

Next, a digital memory used in such a control system and its operational conditions will be described below:

In Figure 5, M_{n-1}, $M_{(n-1)'}$, M_n, $M_{n'}$, M_{n+1}, $M_{(n+1)'}$ ... are memory elements consisting of the MOS type field effect transistors each having a gate internal capacitance for temporarily storing an electric charge which corresponds to information. S_{n-1}, $S_{(n-1)'}$, S_n, $S_{n'}$, S_{n+1}, $S_{(n+1)'}$ ... are switches which are switched by switching signals. These information storing elements operate in such fashion that information stored in the preceding stage is supplied when the switch located at the input of a stage is closed, and the information stored in that stage is supplied to the element in the next stage when the switch located at the output is closed. Accordingly, information is necessarily supplied to the inputs and derived from the outputs to provide a flow of information. ϕ_1 and ϕ_2 are clock pulses.

Figure 6 is a time chart representing phase relationship of the clock pulses ϕ_1 and ϕ_2. That is the periods of the clock pulses ϕ_1 and ϕ_2 are completely identical but only the positions thereof differ and the clock pulse ϕ_2 is within the interval of the clock pulse ϕ_1. The difference between the phases of the clock pulses ϕ_1 and ϕ_2 is based upon the following reasoning.

If they are in the same phase, all of these switches are driven into "ON" state at the same time, and information stored in the

first stage is instantaneously transmitted to the last stage and no delay occurs. A digital delay device may be constituted by combining two-phase transmission switching operation of different phase with the information storing devices and a dynamic register can be thus provided. In fact the phase of the clock pulse ϕ_2 is completely identical to that of the fundamental signal.

By way of example, in Figure 7, it is assumed that the state (A) is exhibited at first. In the drawing, the high level and the low level of the waveform indicate the levels corresponding to "1" and "0" respectively, stored in the respective memory elements. For example, in the state (A), the memory elements M_n, $M_{n'}$, M_{n+2} and $M_{(n+3)'}$ store information corresponding to "1".

If the clock pulse ϕ_1 reaches the "ON" level and the switches S_{n-1}, S_n and S_{n+1} are driven into the "ON" state, the memory element M_{n-1} stores "1" or "0" information according to the internal conditions of the preceding stages. Similarly, the memory element M_n stores information from the memory element $M_{(n-1)'}$ and the memory element M_{n+1} stores information from the memory element $M_{n'}$. Assuming that the information stored in an element is not changed even if energy is supplied to the next stage, information stored in the memory elements $M_{(n-1)'}$, $M_{(n+1)'}$, ... is not changed and the respective elements having primes (') remain as they are. Those states are shown at (B).

When the clock pulse ϕ_1 reaches the "OFF" level and thereafter the clock pulse ϕ_2 reaches the "ON" level, the information stored in the memory elements M_{n-1}, M_n and M_{n+1} is transmitted to the memory elements $M_{(n-1)'}$, $M_{n'}$ and $M_{(n+1)'}$ respectively but the internal states of storage of the memory elements M_{n-1}, M_n, M_{n+1}, ... are not changed.

When both clock pulses ϕ_1 and ϕ_2 have reached the "ON" level, the contents of the memory elements $M_{(n-1)'}$, $M_{n'}$, and $M_{(n+1)'}$ are transmitted to the memory elements $M_{n'}$, $M_{(n+1)'}$ and $M_{(n+2)'}$ respectively. The same result is obtained also with devices such that the content of one device becomes necessarily the state "1" or "0" when it is transmitted to the next stage.

If the memory element is driven into an energy state corresponding to "0" when transmitted to the element in the next stage, the state (A) of Figure 7 is converted into a state shown in Figure 8. The numerals in the lower part of Figure 8 indicate memory levels of the transmitted informations.

When the switches $S_{(n-1)'}$, $S_{(n-1)'}$, S_n, $S_{n'}$, ... are left in the "OFF" state for a long time, since a static flip-flop can keep its energy level regardless of time but a dynamic flip-flop has a tendency of decreasing its energy with lapse of time its duty cycle of switching is limited. In general, a device which can control a delay time in digital fashion as shown in Figure 5 has a substantial width of switching duty cycle.

Considering a duty cycle in the case of a series dynamic register of N digits (nN bits), in connection with the abovementioned feature, at least four or more synchronizing signals (corresponding to the clock pulses ϕ_1 and ϕ_2 of Figure 5) are provided within a unit of the time of one word-length. Therefore, if elements each having the feature that the information level can be kept in a state that information should be correctly transmitted for at least the time of one word-length are used, the limitation of the duty cycle can be neglected.

Accordingly, putting t_b as one bit time, n as the number of bits in one digit and N as the number of digits of a register, such a state should be maintained for a period, $t_b \times n \times N$.

$$t_b \times n \times N < r$$

$$t_b < \frac{r}{nN}$$

where r is a time in which an information storing element is kept in a state of correctly transmitting its content to the next stage. As the abovementioned, the present invention is based upon the discovery that the MOS type field effect transistor can meet such requirements as the above.

When there is a plurality of storage elements having different characteristics in the digital memory of Figure 5, if the signal period of bit time of the whole control system is determined as t_b by measuring and obtaining the values of their respective times during which the memory can be sustained and applying the least one thereof to the above equation, it becomes possible to control information in dynamic fashion using MOS field effect transistors, switches and capacitors, switches and inductors, etc.

Due to the time limit during which the MOS type field effect transistor can sustain the memory as the abovementioned, a specific minimum period of the clock pulse is provided, and the period of the clock pulse is varied within a range above said limit in order to achieve the shift control of the dynamic registed by means of variable control. However, information control need not be executed for both clock pulses ϕ_1 and ϕ_2. For example, in the case of right shift, the clock pulse ϕ_2 may produce outputs always through a period of the time of one word-length and the clock pulse ϕ_1 may be controlled to produce only four outputs.

Figure 9 is a time chart representing phase relationship between the clock pulses in the case of right shift operation. Synchronizing

signals may be produced only during a period of the digit time T_k by controlling only the clock pulse ϕ_1. The reason will be described below referring to Figure 5. Even if the clock pulse ϕ_2 is produced during a period T_k in which the clock pulse ϕ_1 is not produced due to the intermittence control by the logic gate, the energies stored in the memory elements $M_{(n-1)}$, M_n, $M_{(n+1)}$, are maintained as they are and not lost. The energies stored in the memory elements $M_{(n-1)'}$, $M_{n'}$ and $M_{(n+1)'}$ are transmitted to the memory elements of the next stage by the first clock pulse ϕ_1 which follows. The energies will again be transmitted to the succeeding elements by the next clock pulse ϕ_2.

Figure 10 represents a practical circuit of a dynamic register using MOS field effect transistors suited for semiconductor integration. The respective circuit elements are composed of MOS field effect transistors but some of them have not transistor function. Transistors T_1 and T_2, serving information storing action, operate as amplifying elements having storage times and store energies in their gate internal capacitances. The respective gate electrodes are connected to the output terminals from the preceding stages, the source electrodes are grounded and the drain electrodes are connected through an undermentioned load resistor to a power supply V_{DD}. Transistors T_3 and T_4 switched by the clock pulses operate as switching elements. The clock pulses ϕ_1 and ϕ_2 are supplied to the respective gate electrodes and the source and drain electrodes are inserted in a switching controlled circuit. Transistors T_5 and T_6 connected to the respective drain electrodes of the memory elements T_1 and T_2 operate as load resistors of said memory elements T_1 and T_2. Such flip-flop circuits as memory units are connected in cascade in accordance with the desired number of digits to constitute a dynamic memory.

The above description has been made in connection with a dynamic memory having no feedback loop. Even though a flip-flop circuit utilizing MOS field effect transistors is limited to the dynamic type, it can cyclically store informations at every flip-flop and can effectively store information statically if information feedback loops are formed between the succeeding stages.

Figure 11 is a structural diagram of a feedback type flip-flop circuit of this kind, representing a three-phase driving flip-flop circuit using MOS field effect transistors. It is different from the device of Figure 10 in that an information feedback loop is formed between a storing transistor T_{11} in the first stage and a storing transistor T_{12} in the second stage, and switching transistors T_{13}, T_{14} and T_{15} are inserted in the information transmitting paths to introduce three-phase clock pulses ϕ_1, ϕ_2 and ϕ_3. Transistors T_{16} and T_{17} operate as load resistance elements of the storing elements T_{11} and T_{12}. This circuit successively and dynamically circulates information stored in the gate internal capacitances of the storing elements in the circulation loop by means of the switching elements driven by the clock pulses ϕ_1, ϕ_2 and ϕ_3 to store information of one bit. If the clock pulse ϕ_1 is not applied but only the clock pulses ϕ_2 and ϕ_3 are applied, the memory state is maintained and static information storage becomes possible immediately. A new input is introduced when the clock pulse ϕ_1 is applied. The inside of the circulation loop is changed into a new state by the clock pulse ϕ_2 at this time.

Use of three phase clock pulses is based upon the following reasoning. If the switches inserted in the forward path from the storing transistor T_{11} of the fore stage to the storing transistor T_{12} of the back stage and in the feedback path from the back stage to the fore stage are respectively controlled simultaneously by just one clock pulse ϕ_2 there will arise the following disadvantage. That is, in the actual operation, when the states of the fore stage and the back stage are different (conductive and non-conductive), and an input information is newly stored in the transistor of the fore stage, and if then a clock pulse is introduced, the forward path and the feed-back path will be closed simultaneously resulting in an unstable operation, and a correct storage of the information can not be assured. For example, suppose that the elements are of P channel type, (−) potential is being stored in the gate internal capacitance of the back stage element, the drain end of the back stage is in zero potential state, and that then due to an application of an input information (−) potential is newly stored in the gate internal capacitance of the fore stage.

At this time, the fore stage element is in conductive state and its drain end is in zero potential stage. The drain potential of the fore stage under said condition tends to write the new information in the back stage, the zero potential of the back stage already present therein tends at the same time to cancel the (−) potential of the gate internal capacitance of the fore stage, and thus the new information is eliminated. In order to avoid such occurrence as the above, it is necessary to choose the time constant of the feedback path to a large value. One of the methods for this purpose is to use field effect transistors having mutually different mutual conductance or gate internal capacitance, but since it requires a very high manufacturing technique to integrate within same one wafer the field effect transistors having different mutual conductance or gate internal capacitance and, therefore, it is hard to obtain the field effect transistors of a uniform pre-

determined electrical characteristic stable operation can not be expected.

Figure 12 is a further embodiment in which, in addition to two storing transistors T_{21} and T_{22}, one storing transistor T_{23} is added in the output side. Transistors T_{24}, T_{25} and T_{26} operate as switching elements and transistors T_{27}, T_{28} and T_{29} operate as load resistance elements. These circuits are only different in the kind of switching signal but are perfectly identical in the fundamental operation. In any case, switching control of circulation and read-in is provided according to existence of the clock pulse ϕ_1.

Figure 13 represents phase relationship of the above clock pulses ϕ_1, ϕ_2 and ϕ_3.

In one application of the invention the switching signals ϕ_2 and ϕ_3 are maintained as they are and are not controlled at all by the synchronizing signal control device SC. A way of information control (circulation, left shift, right shift) in this feedback type dynamic memory is similar to pulse number control in dynamic memories as described above, but differs at a point that the switching signal ϕ_1 need not be applied when the contents of the registers X and Y are put in a quiescent state because when the clock pulses ϕ_2 and ϕ_3 are being applied information is sustained circulatingly through the feedback path by two MOS type field effect transistors.

WHAT WE CLAIM IS:—

1. An information control system, comprising a dynamic memory in which a plurality, corresponding to the desired number of bits to be stored, of MOS type field effect transistors, each having a gate internal capacitance for temporarily storing an electrical charge which corresponds to a bit of information, are connected in cascade and in which said stored information is shifted in sequence upon introduction of clock pulses each before said electric charges disappear, means for generating periodically and successively said clock pulses which transfer said information and which control the propagation of said information, means for generating instruction signals which designate the kind of effective shift operation to be performed, and control means for varying for a specific period of time and within the time during which said information stored in said MOS type field effect transistor can be sustained the occurrence of said clock pulse to be applied to said dynamic memory corresponding to said kind of instruction and thereby for causing said propagation of said information to be varied and desired effective shift operation performed.

2. An information control system, in accordance with Claim 1, in which said control means interrupts at least one clock pulse of said plurality of clock pulses for only a specific period according to a desired shift to be performed, to control propagation of the information in the memory.

3. An information control system, in accordance with Claim 1, in which said dynamic memory is synchronized with a plurality of clock pulses having the same period but different phases.

4. An information control system, in accordance with Claim 1, in which said dynamic memory includes at least two MOS type field effect transistors at least one for a first-stage and at least one other for a second-stage to constitute a memory unit for storing a binary digit, a path between said memory stages is switched by a plurality of clock pulses, and a plurality of such memory units are connected in cascade according to a required number of binary digits to be stored.

5. An information control system, in accordance with Claim 4, in which a bit interval t_b of the synchronizing signal is selected according with a formula:

$$t_b < \frac{t}{nN}$$

where t is a time period for which the memory element will correctly transfer information to the next transistor and nN is the total number of the memory units in the memory.

6. An information control system, in accordance with Claim 4, in which a feedback loop is formed between the input and the output of the each memory unit of said dynamic memory.

7. An information control system, in accordance with Claims 4 and 6, in which said feedback loop is switched by another clock pulse for returning information in the second-stage to the first-stage.

8. An information control system, in accordance with Claim 4, in which each memory unit includes one MOS type field effect transistor executing memory operation in the output side of the second-stage.

9. An information control system, in accordance with Claim 4, in which switches are inserted in the paths between the memory units in said dynamic memory and at least one clock pulse applied thereto is modified only for a specific period.

10. An information control system, in accordance with Claim 9, in which a switch is inserted between the first-stage and second-stage in a memory unit of the dynamic memory, and said switches inserted between the memory units being driven by a plurality of clock pulses of different phases and only the clock pulses applied to the latter switch being modified.

11. An information control system, in accordance with Claim 2, in which said dynamic memory is formed so as to transfer

determined electrical characteristic stable operation can not be expected.

Figure 12 is a further embodiment in which, in addition to two storing transistors T_{21} and T_{22}, one storing transistor T_{23} is added in the output side. Transistors T_{24}, T_{25} and T_{26} operate as switching elements and transistors T_{27}, T_{28} and T_{29} operate as load resistance elements. These circuits are only different in the kind of switching signal but are perfectly identical in the fundamental operation. In any case, switching control of circulation and read-in is provided according to existence of the clock pulse ϕ_1.

Figure 13 represents phase relationship of the above clock pulses ϕ_1, ϕ_2 and ϕ_3.

In one application of the invention the switching signals ϕ_2 and ϕ_3 are maintained as they are and are not controlled at all by the synchronizing signal control device SC. A way of information control (circulation, left shift, right shift) in this feedback type dynamic memory is similar to pulse number control in dynamic memories as described above, but differs at a point that the switching signal ϕ_1 need not be applied when the contents of the registers X and Y are put in a quiescent state because when the clock pulses ϕ_2 and ϕ_3 are being applied information is sustained circulatingly through the feedback path by two MOS type field effect transistors.

WHAT WE CLAIM IS:—

1. An information control system, comprising a dynamic memory in which a plurality, corresponding to the desired number of bits to be stored, of MOS type field effect transistors, each having a gate internal capacitance for temporarily storing an electrical charge which corresponds to a bit of information, are connected in cascade and in which said stored information is shifted in sequence upon introduction of clock pulses each before said electric charges disappear, means for generating periodically and successively said clock pulses which transfer said information and which control the propagation of said information, means for generating instruction signals which designate the kind of effective shift operation to be performed, and control means for varying for a specific period of time and within the time during which said information stored in said MOS type field effect transistor can be sustained the occurrence of said clock pulse to be applied to said dynamic memory corresponding to said kind of instruction and thereby for causing said propagation of said information to be varied and desired effective shift operation performed.

2. An information control system, in accordance with Claim 1, in which said control means interrupts at least one clock pulse of said plurality of clock pulses for only a specific period according to a desired shift to be performed, to control propagation of the information in the memory.

3. An information control system, in accordance with Claim 1, in which said dynamic memory is synchronized with a plurality of clock pulses having the same period but different phases.

4. An information control system, in accordance with Claim 1, in which said dynamic memory includes at least two MOS type field effect transistors at least one for a first-stage and at least one other for a second-stage to constitute a memory unit for storing a binary digit, a path between said memory stages is switched by a plurality of clock pulses, and a plurality of such memory units are connected in cascade according to a required number of binary digits to be stored.

5. An information control system, in accordance with Claim 4, in which a bit interval t_b of the synchronizing signal is selected according with a formula:

$$t_b < \frac{t}{nN}$$

where t is a time period for which the memory element will correctly transfer information to the next transistor and nN is the total number of the memory units in the memory.

6. An information control system, in accordance with Claim 4, in which a feedback loop is formed between the input and the output of the each memory unit of said dynamic memory.

7. An information control system, in accordance with Claims 4 and 6, in which said feedback loop is switched by another clock pulse for returning information in the second-stage to the first-stage.

8. An information control system, in accordance with Claim 4, in which each memory unit includes one MOS type field effect transistor executing memory operation in the output side of the second-stage.

9. An information control system, in accordance with Claim 4, in which switches are inserted in the paths between the memory units in said dynamic memory and at least one clock pulse applied thereto is modified only for a specific period.

10. An information control system, in accordance with Claim 9, in which a switch is inserted between the first-stage and second-stage in a memory unit of the dynamic memory, and said switches inserted between the memory units being driven by a plurality of clock pulses of different phases and only the clock pulses applied to the latter switch being modified.

11. An information control system, in accordance with Claim 2, in which said dynamic memory is formed so as to transfer

its stored information to the right every time the clock pulses are applied, said clock pulses being applied to said memory for only a period corresponding to the required number of digit shift positions when the memory content is transferred to the right, and the synchronizing signals being interrupted for only a period corresponding to the required number of digit shift positions when the memory content is transferred to the left.

12. An information control system in an electronic computer, provided with a dynamic register in which a plurality, corresponding to the desired number of bits to be stored, of MOS type field effect transistors, each having a gate internal capacitance of temporarily storing an electric charge which corresponds to a bit of information, are connected in cascade and which upon introduction of successive clock pulses before stored electric charges disappear shifts said information in order in synchronization with said clock pulses, an arithmetic unit for processing the arimetical operation of said numerical information in said register to provide a result, an operation generator for generating instructions necessary for the arithmetical operation processes, a timing generator for specifying weights of digits of the numerical information, and a control device for discriminating between respective states of the timing signals, control means responsive to operation control instructions and clock pulses to modify at least one clock pulse of said plurality of clock pulses for only a specific period.

13. An information control system, in accordance with Claim 12, in which gates are provided in the paths through which the clock pulses are to be led into the dynamic register and said gates are controlled by the result of discrimination of the timing signals, operation control instructions and clock pulses in the control device.

14. An information control system, in accordance with Claim 7, in which said feedback loop in the memory unit is switched with a time delay, the switch between the memory units being switched in a phase different therefrom, and the memory being synchronized by use of three clock pulses having different phases and only the occurrence of clock pulses for driving the switch between the memory units being modified.

15. An information control system, in accordance with Claims 4 and 11, in which the MOS type field effect transistors providing storage and the switches for switching the information transmission paths are constituted by MOS field effect transistors and are integrated in a semiconductor integrated circuit.

16. An information control system substantially as described with reference to the accompanying drawings.

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