CLAIMS

WHAT IS CLAIMED IS:

1. A vertical-type nonvolatile memory device, the vertical-type nonvolatile memory device comprising:

a substrate including a cell array area and an extension area, the extension area extending in a first direction from the cell array area and comprising vertical contacts;

a vertical channel structure extending in a vertical direction from a top surface of the substrate;

a first stack structure comprising gate electrode layers and first interlayer insulating layers that are alternately stacked along sidewalls of the vertical channel structure;

a plurality of division areas extending in the first direction and dividing the cell array area and the extension area into units in a second direction perpendicular to the first direction;

in the extension area, two insulating layer dams are arranged between two of the division areas adjacent to each other in the second direction, wherein the two insulating layer dams extend in the first direction;

a second stack structure comprising sacrificial layers and second interlayer insulating layers that are alternately stacked on the substrate between the two insulating layer dams; and

an electrode pad connected to a first gate electrode layer of the gate electrode layers in the extension area,

wherein the first stack structure extends from the cell array area to an area between one of the division areas and one of the insulating layer dams in the extension area,

the electrode pad comprises a first pad area on the first stack structure and a second pad area on the second stack structure,

a first vertical contact penetrates the second pad area and is inserted into the second stack structure,

the first pad area and the second pad area are connected to each other on a top surface of the one insulating layer dam, and

the first pad area is connected to corresponding gate electrode layers.

2. The vertical-type nonvolatile memory device of claim 1, wherein, in the

vertical direction, the first pad area is thicker than the gate electrode layer in the cell array area.

3. The vertical-type nonvolatile memory device of claim 1 or claim 2, wherein the electrode pad is divided into a first electrode pad and a second electrode pad by a pad gap extending in the first direction between the two insulating layer dams, and

the first vertical contact is connected to the first electrode pad and a second vertical contact is connected to the second electrode pad.

4. The vertical-type nonvolatile memory device of claim 3, wherein an end portion of each of the first electrode pad and the second electrode pad in the first direction have different heights from each other in the vertical direction.

5. The vertical-type nonvolatile memory device of claim 3 or claim 4, wherein the gate electrode layers have a stepped structure in the first direction in the extension area,

the gate electrode layers corresponding to the first electrode pad have a stepped structure each two layers, while a single odd-numbered gate electrode layer constitutes an upper layer,

the gate electrode layers corresponding to the second electrode pad have a stepped structure each two layers, while a single even-numbered gate electrode layer constitutes an upper layer,

the first electrode pad is connected to the odd-numbered gate electrode layer, and

the second electrode pad is connected to the even-numbered gate electrode layer.

6. The vertical-type nonvolatile memory device of any one of claims 1 to 5, wherein, in the cell array area, another division area extending in the first direction is arranged between the two division areas adjacent to each other in the second direction.

7. The vertical-type nonvolatile memory device of any one of claims 1 to 6, wherein the vertical channel structure has a first vertical channel structure in the cell array area and a second vertical channel structure in the extension area, and

the second vertical channel structure is arranged in a portion where the first stack

structure is formed in the extension area.

8. A vertical-type nonvolatile memory device, the vertical-type nonvolatile memory device comprising:

a substrate including a cell array area and an extension area extending in a first direction from the cell array area;

a vertical channel structure extending in a vertical direction from a top surface of the substrate;

a first stack structure comprising gate electrode layers and first interlayer insulating layers that are alternately stacked along sidewalls of the vertical channel structure;

a division area extending in the first direction and dividing the cell array area and the extension area into units in a second direction perpendicular to the first direction;

in the extension area, two insulating layer dams are arranged between two division areas adjacent to each other in the second direction, wherein the two insulating layer dams extend in the first direction;

a second stack structure comprising sacrificial layers and second interlayer insulating layers that are alternately stacked on the substrate between the two insulating layer dams;

an electrode pad connected to a first gate electrode layer of the gate electrode layers and arranged in the extension area, the electrode pad comprising a first pad area on the first stack structure and a second pad area on the second stack structure; and

a first vertical contact arranged in the extension area and inserted into the second stack structure via the second pad area of the electrode pad,

wherein the electrode pad overlaps at least one of the insulating dams in the vertical direction.

9. The vertical-type nonvolatile memory device of claim 8, wherein the electrode pad has a raised pad structure thicker than each of the gate electrode layers of the cell array area in the vertical direction,

a lower portion of the first pad area is in contact with a side surface of one of the insulating layer dams, and

the first pad area is connected to the second pad area on a top surface of the one

insulating layer dam.

10. The vertical-type nonvolatile memory device of claim 8 or claim 9, wherein the electrode pad is divided into a first electrode pad and a second electrode pad by a pad gap extending in the first direction between the two insulating layer dams,

the first electrode pad and the second electrode pad have side end portions at substantially identical positions in the first direction and have different heights from each other in the vertical direction, and

the first vertical contact is connected to the first electrode pad and a second vertical contact is connected to the second electrode pad.

11. The vertical-type nonvolatile memory device of claim 10, wherein the gate electrode layers have a stepped structure in the first direction in the extension area,

the gate electrode layers corresponding to the first electrode pad have a stepped structure each two layers, while a single odd-numbered gate electrode layer constitutes an upper layer,

the gate electrode layers corresponding to the second electrode pad have a stepped structure each two layers, while a single even-numbered gate electrode layer constitutes an upper layer,

the first electrode pad is connected to the odd-numbered gate electrode layer, and

the second electrode pad is connected to the even-numbered gate electrode layer.

12. The vertical-type nonvolatile memory device of any one of claims 8 to 11, wherein, in the cell array area, another division area extending in the first direction is arranged between the two division areas adjacent to each other in the second direction,

the vertical channel structure comprises a first vertical channel structure in the cell array area and a second vertical channel structure in the extension area, and

the second vertical channel structure is arranged in a portion where the first stack structure is formed in the extension area.

13. A method of manufacturing a vertical-type nonvolatile memory device, the

method comprising:

forming a mold structure by alternately stacking second interlayer insulating layers and sacrificial layers on a substrate including a cell array area and an extension area;

forming, in the extension area, insulating layer dams extending in a first direction on the substrate and being apart from each other in a second direction perpendicular to the first direction;

forming a stepped structure exposing the sacrificial layers in the first direction in the extension area by etching the mold structure;

forming an additional sacrificial layer on the exposed sacrificial layers in the extension area;

forming, on the substrate, a vertical channel structure to penetrate the mold structure and extending in a direction perpendicular to a top surface of the substrate;

forming, on the substrate, a first division trench extending in the first direction and dividing the cell array area and the extension area;

forming a first stack structure comprising gate electrode layers and first interlayer insulating layers that are alternately stacked along sidewalls of the vertical channel structure, by replacing the sacrificial layer and the additional sacrificial layer with a first conductive layer by using the first division trench;

forming a division area by forming an insulating layer in the first division trench; and

forming, in the extension area, a first vertical contact connected to an electrode pad,

wherein two insulating layer dams are arranged in the second direction from the division area, and

in the forming of the first stack structure, the first stack structure is formed in the cell array area, a second stack structure that is substantially identical to the mold structure between the two insulating layer dams is maintained, and the electrode pad, which is connected to the gate electrode layers in the extension area, is formed,

wherein, in the forming of the first stack structure, the first stack structure is formed between the first division trench and one of the insulating layer dams in the extension area,

the electrode pad comprises a first pad area on the first stack structure and a second pad area on the second stack structure,

in the forming of the first vertical contact, the first vertical contact is, while being

connected to the second pad area, configured to penetrate the second pad area and inserted into the second stack structure,

the first pad area and the second pad area are connected to each other on a top surface of the one insulating layer dam, and

the first pad area is connected to corresponding gate electrode layers.

14. The method of claim 13, wherein, in the forming of the stepped structure, in the extension area, top surfaces of the sacrificial layers and the insulating layer dams are coplanar and exposed in the stepped structure, and

in the forming of the additional sacrificial layer,

the additional sacrificial layer covers top surfaces of the sacrificial layers and the insulating layer dams that are exposed in the stepped structure, and

in the forming of the first stack structure,

in the extension area, the additional sacrificial layer and one of the sacrificial layers are replaced with the electrode pad.

15. The method of claim 13 or claim 14, wherein the electrode pad is divided into a first electrode pad and a second electrode pad by a pad gap extending in the first direction between the two insulating layer dams,

the first vertical contact is connected to the first electrode pad and a second vertical contact is connected to the second electrode pad, and

the first electrode pad and the second electrode pad comprises side end portions at substantially identical positions in the first direction and have different heights from each other in a vertical direction.

16. The method of claim 15, wherein the gate electrode layers have a stepped structure in the first direction in the extension area,

the gate electrode layers corresponding to the first electrode pad have a stepped structure each two layers, while a single odd-numbered gate electrode layer constitutes an upper layer,

the gate electrode layers corresponding to the second electrode pad have a stepped

structure each two layers, while a single even-numbered gate electrode layer constitutes an upper layer,

the first electrode pad is connected to the odd-numbered gate electrode layer, and

the second electrode pad is connected to the even -numbered gate electrode layer.

17. The method of any one of claims 13 to 16, wherein the forming of the first division trench comprises forming a second division trench adjacent to the first division trench in the second direction and forming, in the cell array area, a third division trench extending in the first direction between the first and second division trenches, and

the forming of the division area comprises forming the divided area and another division area by forming an insulating layer in the first division trench and third division trench.