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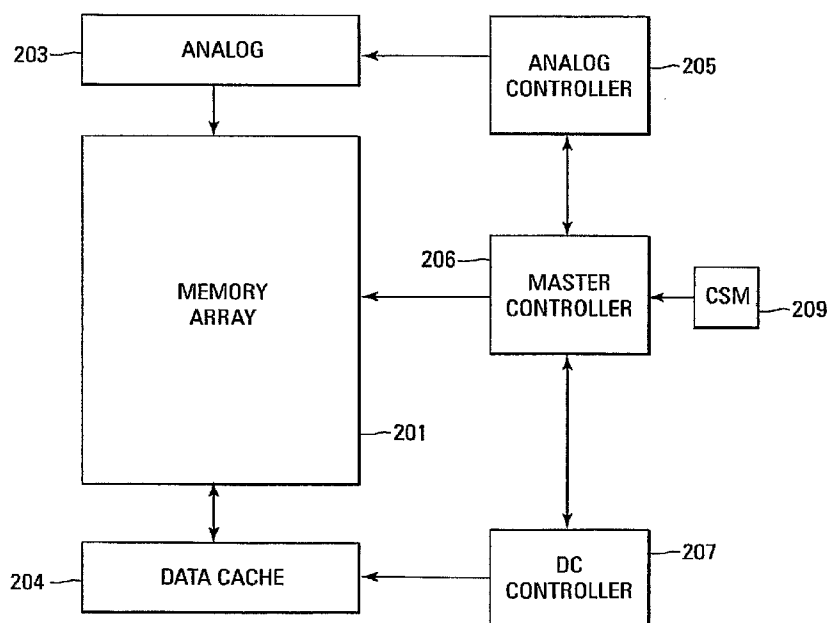
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(54) Title: MEMORY DEVICE DISTRIBUTED CONTROLLER SYSTEM



(57) Abstract: A memory device distributed controller circuit distributes memory control functions amongst a plurality of memory controllers. A master controller receives an interpreted command and activates the appropriate slave controllers depending on the command. The slave controllers can include a data cache controller that is coupled to and controls the data cache and an analog controller that is coupled to and controls the analog voltage generation circuit. The respective controllers have appropriate software/firmware instructions that determine the response the respective controllers take in response to the received command.

WO 2007/106481 A1



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