

**SYSTEMS AND METHODS TO IMPROVE WAFER BOW COMPENSATION
EFFICIENCY AND FLATTEN WAFERS TO NEUTRAL BOW**

CROSS-REFERENCES

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] Semiconductor manufacturing typically involves one or more processes to deposit and pattern a structure on a wafer. As the complexity and/or non-uniformity of the structure and/or materials on or across the wafer increase, stress applied to the wafer can cause wafer deformation (e.g., bowing, twisting, etc.) impacting various aspects from structure formation to product yield. For example, in three-dimensional NOT-AND logic gate (3D-NAND) structure fabrication, multi-stacked films with thick, high stress carbon-based hard masks, metallization patterns, and substrate trenches can cause significant wafer warpage, leading to issues such as frontside lithographic overlay mismatches, wafer bow beyond chucking limits of an electrostatic chuck, etc.

[0003] The background provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent that it is described in this background, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the disclosure.

SUMMARY

[0004] Disclosed herein are methods and systems of analyzing wafer shapes and backside films. In one aspect of the embodiments herein, a computer program product is disclosed, the computer program product including a non-transitory computer readable medium having computer-executable instructions for: identifying a wafer shape having a frontside and a backside, wherein the wafer shape has a first bow along a first axis of the wafer shape and a second bow along a second axis of the wafer shape; identifying a plurality of complementary profile film stacks, wherein each complementary profile film stack includes a first non-uniform thickness profile film and a second non-uniform thickness profile film; determining a compensated first bow and a compensated second bow of the wafer shape corresponding to each stack of complementary profile films when applied to the backside of the wafer shape; and identifying a first complementary profile film stack of the plurality of complementary profile film stacks based on the compensated first bow and the compensated second bow.

[0005] In some embodiments, including additional computer-executable instructions for identifying a semiconductor fabrication process recipe to deposit the first complementary profile film stack. In some embodiments, a first subset of the plurality of complementary profile film stacks include complementary profile film stacks having multiple pairs of complementary profile films. In some embodiments, each pair of complementary profile films in a complementary profile film stack of the first subset has a different stress ratio than other pairs of complementary profile films in the complementary profile film stack. In some embodiments, the first axis and the second axis are perpendicular to each other. In some embodiments, the wafer shape has a delta bow based on a difference between the first bow and the second bow and a compensated delta bow based on a difference between the compensated first bow and the compensated second bow, and wherein identifying the first complementary profile film stack is based on the percentile difference between the delta bow and the compensated delta bow. In some embodiments, the first non-uniform thickness profile film has an internal tensile stress and the second non-uniform thickness profile film has an internal compressive stress. In some embodiments, the plurality of complementary profile film stacks include films having different ratios of internal compressive stress to internal tensile stress. In some embodiments, including additional computer-executable instructions for determining a compensation efficiency for each complementary profile film stack, wherein the first complementary profile film stack has a maximum compensation efficiency of the plurality of complementary profile film stacks. In some embodiments, including additional computer-executable instructions for: identifying a plurality of total thicknesses for each complementary profile film stack; determining a plurality of compensated first bows and compensated second bows for each complementary profile film stack, the plurality of compensated first bows and compensated second bows corresponding to the plurality of total thicknesses; and determining an optimal total thickness for each complementary profile film stack based on the plurality of compensated first bows and compensated second bows. In some embodiments, including additional computer-executable instructions for determining a compensated delta bow for each total thickness of the plurality of total thicknesses for each complementary profile film stack of the plurality of complementary profile film stack, wherein determining the optimal total thickness is based on a percentile difference between the compensated delta bow and a delta bow based on the first bow and the second bow. In some embodiments, the first non-uniform thickness profile film is a curved-bar profile film and the second non-uniform thickness profile film is a curved-channel profile film. In some embodiments, the plurality of complementary profile film stack include curved-bar profile films having different profiles based on polynomial functions defining the profile in an x-direction of the wafer shape. In some embodiments, including additional computer-executable instructions for: identifying a plurality of cap layers, each cap layer having

- a uniform thickness profile and either a tensile internal stress or compressive internal stress; determining a plurality of secondary compensated first bow and secondary compensated second bow of the wafer shape corresponding to combinations of each complementary profile film stack and each cap layer; and identifying a first cap layer and a second complementary profile film stack
- 5 based on the plurality of secondary compensated first bow and secondary compensated second bow. In some embodiments, determining the compensated first bow and the compensated second bow includes simulating the wafer shape and each corresponding complementary profile film stack. In some embodiments, the simulation models the wafer shape as a shell and each complementary profile film stack as a membrane without bending stiffness.
- 10 [0006] These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

- [0007] Figures 1A and 1B show examples of unbowed and bowed semiconductor wafers on an electrostatic chuck.
- 15 [0008] Figures 2A-B show example isometric views of anisotropic wafer bow.
- [0009] Figure 3A illustrates exemplary zones for depositing films having a curved bar profile and a curved channel profile on a backside of a wafer according to various embodiments herein.
- [0010] Figures 3B and 3C illustrate a side view and exploded side view of a wafer having backside layers having a curved bar profile and a curved channel profile according to various
- 20 embodiments herein.
- [0011] Figures 3D-3J illustrate side views of a wafer having alternating stack of backside layers having more than one pair of a curved bar profile film and a curved channel profile film according to various embodiments herein.
- [0012] Figure 4A-B are graphs showing internal stress of individual tensile and compressive
- 25 films and a stacked film according to various embodiments herein.
- [0013] Figure 5A-C present simulations of wafer bow compensation based on different complementary profile films.
- [0014] Figures 6A-C present simulations of wafer bow for different thicknesses of complementary profile films.
- 30 [0015] Figure 7 is a process flow diagram illustrating use of a model to select a process recipe.
- [0016] Figure 8 is a process flow diagram illustrating training of a model.

[0017] Figure 9 is an example interface for a finite element method software.

[0018] Figures 10A and 10B show a block diagram of an example substrate processing system.

[0019] Figure 11A shows an example cross section of an edge of a shower-pedestal.

[0020] Figure 11B shows a top view of an example carrier ring.

5 [0021] Figure 12 shows a schematic of an example process system that may be used to perform the methods described herein.

[0022] Figure 13 presents a schematic diagram of a processing system for performing various embodiments herein.

DETAILED DESCRIPTION

10 *Terminology*

[0023] The following terms are used throughout the instant specification:

[0024] The terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate” and “partially fabricated integrated circuit” may be used interchangeably. Those of ordinary skill in the art understand that the term “partially fabricated integrated circuit” can refer to a semiconductor wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm. Examples of wafer materials include silicon (Si), gallium arsenide (GaAs), and silicon germanium (SiGe). Besides semiconductor wafers, other workpieces that may take advantage of the disclosed embodiments include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, display devices or components such as backplanes for pixelated display devices, flat panel displays, micro-mechanical devices and the like. The workpiece may be of various shapes, sizes, and materials.

[0025] A “semiconductor device fabrication operation” as used herein is an operation performed during fabrication of semiconductor devices. Typically, the overall fabrication process includes multiple semiconductor device fabrication operations, each performed in its own semiconductor fabrication tool such as a plasma reactor, an electroplating cell, a chemical mechanical planarization tool, a wet etch tool, and the like. Categories of semiconductor device fabrication operations include subtractive processes, such as etch processes and planarization processes, and material additive processes, such as deposition processes (e.g., physical vapor deposition, chemical vapor deposition, atomic layer deposition, electrochemical deposition, electroless deposition). In the context of etch processes, a substrate etch process includes processes that etch a mask layer or, more generally, processes that etch any layer of material previously deposited on

and/or otherwise residing on a substrate surface. Such an etch process may etch a stack of layers in the substrate.

[0026] “Manufacturing equipment” refers to equipment in which a manufacturing process takes place. Manufacturing equipment often has a process chamber in which the workpiece resides during processing. Typically, when in use, manufacturing equipment performs one or more semiconductor device fabrication operations. Examples of manufacturing equipment for semiconductor device fabrication include deposition reactors such as electroplating cells, physical vapor deposition reactors, chemical vapor deposition reactors, and atomic layer deposition reactors, and subtractive process reactors such as dry etch reactors (e.g., chemical and/or physical etch reactors), wet etch reactors, and ashers.

[0027] “Wafer bow” as used herein may refer to a deformation of a wafer. The deformation may have radial and/or azimuthal components. Wafer bows may be symmetric or asymmetric in radial and/or azimuthal directions. Examples of types of wafer bow include dome shapes, bowl shapes, and saddle shapes. Wafer bow may occur during fabrication, for example, as a result of stress to the wafer during deposition of materials on an active surface of a wafer. Wafer bow may occur during various types of fabrication, such as when large stacks of materials are deposited at a high temperature and then the process chamber is cooled down to a room temperature. Wafer bow may cause complications in subsequent processing steps. For example, the wafer may fail to chuck correctly if an amount of bowing is too large, which may subject the wafer to nonuniform heating and/or other process conditions. Moreover, some processing steps (e.g., photolithography) may produce poor results if performed on a wafer that is excessively bowed.

[0028] In some embodiments, wafer bow may be measured as a deviation of the mean or median distance of the surface of the wafer to a reference plane. In some embodiments, the point of the median surface of the wafer may be the center point (e.g., in the case of concave or domed bowing), or an edge point of the wafer and/or an average edge point of the wafer (e.g., in the case of warping or convex bowing). In some embodiments wafer bow may be measured from a reference plane such that when an edge point of the wafer is below the reference plane the edge point is considered to have a negative bow, and when the edge point of the wafer is above the reference plane the edge point is considered to have a positive bow. In some embodiments, positive or negative bow may be measured along a z axis perpendicular to the reference plane.

[0029] In some embodiments, wafer bow may vary between the two principal planar directions of a substrate, which are referred to as the x and y directions. For example, wafer bow along the x direction may be in a positive z direction while wafer bow along the y direction may be in a

negative z direction (the z axis being perpendicular to a plane formed by the planar x and y directions). Figure 2B illustrates 8 shapes that may be formed based on bowing in x and y directions. When bowing is positive along the x and y directions, a bowl shape is formed, while when bowing is negative in the x and y directions, an umbrella or dome shape is formed. Other shapes include a “half pipe” or “taco” shape when there is substantially no wafer bow in one direction while a positive or negative bow in the planar perpendicular direction. When wafer bow is positive in one direction and negative in another direction, a “saddle” or “potato chip” shape is formed.

[0030] Wafer bowing may be characterized by x-bow and y-bow values. A positive x-bow corresponds to bowing of the wafer in a positive z-direction at a coordinate of the wafer having a large x-value and a small or zero y-value, e.g., an x-value greater than about 100 mm or of about 150 mm (for a 300 mm wafer) and a y-value of about 0 mm (where the reference point is at a center of the wafer). A negative x-bow similarly corresponds to bowing of the wafer in a negative z-direction at a coordinate of the wafer having a large x-value and a small or zero y-value. Conversely, a positive y-bow and negative y-bow correspond to bowing of the wafer in positive or negative z-directions, respectively, at a coordinate of the wafer having a large y-value and a small or zero x-value.

[0031] In some embodiments, wafer bow may be characterized by a single value. In some embodiments, wafer bow may be described as a “delta bow.” When referring to wafer bow of saddle-shaped wafers, the wafer delta bow may be expressed in terms of a difference between the negative-bow in one direction (such as along the x-axis) and positive-bow in another direction (such as along the y-axis). For example, a wafer bow of 200 μm may result from an x-bow of -25 μm and a y-bow of +175 μm . For wafers having a taco, bowl, or dome-shaped wafer bow, wafer bow may refer to a difference between the maximum bow and a reference plane as described above. In some embodiments, delta bow describes a maximum difference between the bows in perpendicular directions, e.g., a difference between a maximum x-bow and a maximum y-bow.

[0032] In some embodiments, delta bow may be a difference between a maximum bow in the positive z-direction and a maximum bow in the negative z-direction. In some embodiments, the maximum bow in the positive z-direction is either an x-bow or y-bow value, and the maximum bow in the negative z-direction is the corresponding y-bow or x-bow value, respectively. However, in some embodiments, the maximum bow in the positive z-direction and the maximum bow in the negative z-direction may both be from x-bow or both from y-bow. As shown in compensated wafer 604 in Figure 6A, the delta bow is 155 μm , which is measured as a difference between a positive x-bow value at about 100 mm radius (i.e., about 65 μm) and a negative x-bow value at 150 mm

(i.e., about $-90\text{ }\mu\text{m}$). The y-bow values are not used to determine the delta bow in compensated wafer 604 as the x-bow's change as a function of radius results in the maximum bow in the positive z-direction and the maximum bow in the negative z-direction to both be measured along the x-axis.

- 5 **[0033]** A “curved bar profile” is characterized by a two-dimensional shape that has a varying thickness along one of the two principal planar dimensions of a substrate, which are referred to as the x and y directions. While the thickness varies in one of these two directions, it does not substantially vary in the other direction. Further, the curved bar profile means that the thickness of the layer is generally thicker toward the center of the substrate than the edges of the substrate.
- 10 Hence the structure appears like a bar or “speed bump” on the backside of the substrate. In some cases, the curved bar profile varies in the direction away from the plane of the substrate (the z-direction) as a function of x-axis position, but without significantly varying in the y-axis position. In other cases, the curved bar profile varies in the z direction as a function of y-axis position, but without significantly varying in the x-axis position. In certain embodiments, a curved bar is
- 15 disposed along a principal axis of the substrate such that a centerline of the bar passes through the origin (center point) of the substrate. Thus, the curved bar profile may be characterized by a film having greater thickness in the center of the substrate than the edge of the substrate. The curved shape may be generally rounded such a circular, parabolic, gaussian, etc. In some embodiments the shape may be characterized by a parabolic or polynomial function.
- 20 **[0034]** A “curved channel profile” is characterized by a two-dimensional shape that has a varying thickness along one of the x and y directions of the substrate, which are referred to as the x and y directions. While the thickness varies in one of these two directions, it does not substantially vary in the other direction. Further, the curved channel profile means that the thickness of the layer is generally thicker toward the edges of the substrate than the center of the
- 25 substrate. Hence the structure appears like a channel or indentation on the backside of the substrate. In some cases, the curved channel profile varies in the direction away from the plane of the substrate (the z-direction) as a function of x-axis position, but without significantly varying in the y-axis position. In other cases, the curved channel profile varies in the z direction as a function of y-axis position, but without significantly varying in the x-axis position. In certain embodiments,
- 30 a curved channel is disposed along a principal axis of the substrate such that a centerline of the channel passes through the origin (center point) of the substrate. Thus, the curved channel profile may be characterized by a film having greater thickness at the edges of the substrate than the center of the substrate. The curved shape may be generally rounded such as a circular, parabolic, gaussian, etc. In some embodiments the shape may be characterized by a parabolic or polynomial

function.

[0035] Generally, the curved bar and curved channel profiles refer to geometries of the films' varying properties. Frequently, the film property is film thickness, but other properties can similarly assume the profiles. Such properties may include film density, film composition, film internal stress, etc. Examples of a curved bar profile and a curved channel profile are illustrated in Figures 3B and 3C. Film 308 is an example of a curved bar profile, while film 307 is an example of a curved channel profile. A curved bar profile film and a curved channel profile film may also be referred to as non-uniform thickness profile films. A non-uniform thickness profile film may refer to either of a curved bar profile film or a curved channel profile film.

[0036] A "uniform thickness profile" is characterized by a two-dimension shape that has a substantially non-varying thickness along any planar directions of a substrate, e.g., an x and y direction. In some embodiments, the combination of a curved channel profile film and a curved bar profile film may be a uniform thickness film. In some embodiments, a curved channel profile film and a curved bar profile film have complementary shapes that together may form a substantially uniform thickness profile bilayer film. In some embodiments, the combination of a curved bar profile film and a curved channel profile film may be referred to as a complementary profile film stack. In some embodiments, a non-uniform thickness profile may refer to either or both of a curved channel profile and a curved bar profile. In some embodiments, a stacked film formed from combination of layers having a curved channel profile and layers of having a curved bar profile may be substantially flat, e.g., having a flatness similar to a single uniform thickness profile film deposited to a similar thickness as the combined non-uniform thickness profile films. In some embodiments, as discussed further below in relation to Figures 3D-J, a complementary profile film stack may comprise multiple pairs of complementary profile films. In some embodiments a complementary profile film stack may comprise one or more curved bar profile films and one or more curved channel profile films.

Bowed Wafers

[0037] Semiconductor device fabrication often involves deposition of a stack of layers or films on a wafer. Typically, most deposition and other processing to form the devices occurs on one side of the wafer, often referred to as the front face or frontside of a wafer. As the deposited layers build up, they can introduce stress in the wafer. A large net tensile or compressive stress can cause the wafer to bow (and potentially crack in case of excessive tensile stress), which is undesirable.

[0038] Bowing is especially likely to occur where large stacks of materials are deposited, for example, in the context of 3D-NAND devices, or where a thick frontside layer is deposited. Where

bowing is significant, it can deleteriously affect subsequent processing steps. For instance, the wafer may fail to chuck correctly if the bowing is too great. Figures 1A and 1B show a wafer on an electrostatic chuck, which typically have a flat surface. Figure 1A shows a wafer 102 on an electrostatic chuck 110. When the wafer 102 is substantially flat for purposes of a particular process operation, e.g., having a bow of about 100 μm or less, the wafer may be properly clamped, securing the wafer for subsequent processing steps. Figure 1B shows a bowed wafer 104 on the electrostatic chuck 110. Wafer 104 is illustrated as having a negative wafer bow (i.e., a dome shape where the center point of the wafer is above the edge of the wafer). This may result from frontside layers having a compressive internal stress. Frontside layers having a tensile internal stress may cause a wafer to bow in the opposite manner, having a bowl shape.

[0039] When the bow is significant, various manufacturing problems may arise. In some instances, the wafer may fail to secure properly on the electrostatic chuck. This may cause various nonuniformity issues—for example, the wafer may not be heated uniformly, the process gases may not be applied to the wafer uniformly across the wafer, and/or the distance between the wafer and the showerhead and/or showerhead pedestal may not be maintained evenly in parallel (i.e., parallelism may be disrupted). Wafer bow may cause other problems. For example, certain processing steps (e.g., photolithography) are very precise and produce poor results if the wafer is not substantially flat. The problem may be manifest as lithography defocus. Cracking may also occur, which can introduce additional defects, reducing yield.

[0040] One example stack that may cause these problems is a stack having alternating layers of oxide and nitride (e.g., silicon oxide/silicon nitride/silicon oxide/silicon nitride, etc.). Another example of a type of stack likely to cause bowing includes alternating layers of oxide and polysilicon (e.g., silicon oxide/polysilicon/silicon oxide/polysilicon, etc.). Other examples of stack materials that may be problematic include, but are not limited to, tungsten and titanium nitride.

[0041] The materials in the stacks may be deposited through chemical vapor deposition (CVD) techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), or plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Certain disclosed embodiments may be useful whenever wafer stress and/or bowing are induced due to material present on the frontside of the wafer.

[0042] The frontside stacks may be deposited to any number of layers and thicknesses. In an

example, the stack may include about 20 or more layers, and have a total thickness of about 2 μm to about 4 μm . In some cases, multiple-layer stacks may include about one hundred or more layers. In some embodiments, multiple-layer stacks may have about five hundred or more layers. In some embodiments, the multiple-layer stacks may have about one thousand or more layers. Such stacks
5 may have a thickness of about 4 μm to 12 μm , for example.

[0043] The stress induced in the wafer by the stack or other frontside deposition may be about -500 MPa to about $+500\text{ MPa}$. In some embodiments, the resulting in a bow is about 150 μm or greater, e.g., about 300 μm and above, about 400 μm and above, or about 200 μm to about 400 μm (for a 300 mm wafer).

10 **[0044]** Another cause of wafer bow may be frontside processing which uses thick hardmasks with limited etch selectivity. In these embodiments, at least one of the one or more frontside layers is a hardmask. The thick hardmasks may have an internal stress similar to those described above, e.g., have a magnitude of 0 MPa to about 500 MPa. The stress caused by the hardmask may be tensile stress or compressive stress. The thick hardmasks may cause wafers to have a significant
15 wafer bow, e.g., about 150 μm or more.

[0045] Various techniques have been devised for combatting bowing. When bowing is severe, deposition processes may be tuned to reduce or counteract internal stresses in deposited layers. However, any such tuning should not interfere with process requirements for fabricating devices. One commonly used technique to counteract bowing deposits layers on the backside of the wafer.

20 **[0046]** Backside deposition may form a high-stress film on the backside of the wafer intentionally to control overall stress and bowing of the wafer. If the backside layer has the same type of internal stress (tensile or compressive) and of comparable magnitude to the internal stress created on the frontside of the wafer, the backside film effectively counteracts and reduces the bow of the wafer.

25 **[0047]** Examples of backside films used to counteract bow include the following: amorphous silicon, silicon oxide, silicon nitride, and silicon oxynitride. Variations of these films may be used, such as doped amorphous silicon, doped silicon oxide, doped silicon nitride, and doped silicon oxynitride; and these films may be formed under different deposition conditions to tune and optimize their material properties. Also, other types of films that may be introduced during the
30 semiconductor process may be used in conjunction with, and/or instead of, these exemplary films. Current backside films have high internal stress and can mitigate the stresses imparted on the wafer from the frontside layers to reduce or eliminate the wafer bow. Although not required, generally, backside layers are made of films with high stress when deposited on the silicon wafer. High-

stress films may be preferred because a high-stress films may compensate the wafer bow more efficiently.

5 [0048] In some embodiments, backside film thicknesses are relatively uniform because the bow caused by depositing material on the frontside is relatively symmetrical, forming a bowl or dome shape based on an isotropic internal stress. Thus, depositing a uniform thickness profile film, either with tensile or compressive internal stress, could mitigate the stress imparted on a wafer from the frontside layers as the backside film would impart an opposite wafer bow that is similarly symmetrical. However, certain frontside deposition techniques may cause anisotropic stress, such that the internal stress on the frontside of the wafer, and hence the resultant bowing, varies in one principal planar direction compared to another principal planar direction, e.g., x and y directions. 10 In such embodiments a wafer may have x-bow and y-bow that are different in magnitude as well as direction (or sign). A uniform backside layer may insufficiently address such saddle-shaped wafer bow.

[0049] Figure 2A presents a perspective view of a bowed wafer exhibiting one type of asymmetrical bowing. Substrate 201 is shown relative to a three-dimensional coordinate system 15 having reference plane 203 parallel to a plane defined by the x-axis direction and the y-axis direction. In this manner, an extent of deformation (e.g., warpage) of substrate 201 from reference plane 203 is indicated along the u-axis direction. Accordingly, substrate 201 is shown as being asymmetrically bowed. In other words, a sign or direction of the bowing of substrate 201 along the x-axis direction is different than a sign or direction of the bowing of substrate 201 along the y-axis direction. For instance, bow in the x-axis direction has a positive value and bow in the y-axis direction has a negative value. Such deformation of substrate 201 may be referred to as “saddle-shaped” bowing of substrate 201. As used herein, warpage refers to any deviation of a median surface of substrate 201 from a reference plane 203, and, thereby, from planarity. 20

25 [0050] One technique to address saddle-shaped wafer bow is to deposit films on the backside of the wafer that cause anisotropic stress across the wafer from the backside such that the overall wafer bow may be controlled. Such films, when viewed along an x-direction, may have an internal compressive stress near the center of the wafer while having an internal tensile stress near the edge of the wafer, or vice versa. Such films, when viewed along a y-direction, may have an internal compressive stress from center-to-edge or an internal tensile stress from center-to-edge. When 30 deposited on the backside of a wafer such films may reduce wafer bow that is inequal along x and y directions. While such techniques are obviously applicable to wafers having a positive y-bow and negative x-bow, or vice versa, techniques disclosed herein may be applied to various wafer bow shapes that have a different magnitude or sign of bowing in one principal direction than the

other principal direction, or wafers having no bow. For example, the techniques disclosed herein may be applied to the wafer having a certain shape of bow caused by the frontside deposition. For another example, the backside of the bare wafer having no frontside deposited layers or the wafer having no or minimal bow may be processed with the techniques disclosed herein preemptively
5 before bow is generated due to the frontside deposition.

[0051] Anisotropic internal stress may be accomplished by depositing curved bar profile and curved channel profile films on a wafer. A curved bar profile film and a curved channel profile film may have different internal stresses, resulting in a stacked film that has an anisotropic internal stress, i.e., the internal stress changes based upon the direction. As an example, Figures 3A-C
10 illustrate curved bar and curved channel profile films. Figure 3A is a bottom-side view of a wafer 306 having a center zone 304 and edge zones 302. Figure 3B and 3C present a side view and exploded side view, respectively, along the x direction of the wafer 306 having a curved bar profile film 308 and a curved channel profile film 307. A frontside layer 305 may be deposited on the frontside (or top) of wafer 306, causing a wafer bow that is compensated by films 307 and 308
15 deposited on a backside (or bottom) of the wafer 306. A film may be deposited on the backside of the wafer such that the film is substantially deposited in either center zone 304 or edge zones 302. This may be accomplished by a showerhead that is configured to substantially deposit in center zone 304 or edge zones 302. In some embodiments, a showerhead pedestal (or shopped) may be used for such deposition. In some embodiments, a shopped may be configured to deposit in such
20 zones by, e.g., control of reactant gas flow in zones of the shopped that correspond to the zones of Figure 3A. Such zones are schematically illustrated in Figure 3A for illustration purposes only; a shopped or wafer may be considered having any different numbers, shapes, and configurations of zones.

[0052] Referring back to Figures 3B and 3C, a film deposited substantially in center zone 304
25 may have curved bar profile 308, while a film deposited substantially in edge zones 302 may have curved channel profile 307. That is, for example, a compressive stress film (307) may be deposited more in edge zones 302 (e.g., is thicker) compared to in center zone 304, while a tensile stress film (308) may be deposited more in the center zone 304 (e.g., is thicker) compared to in edge zones 302. While films may be deposited substantially in either center zone 304 or edge zones 302, it
30 should be understood that some deposition may occur across the wafer and in the other zone. Furthermore, the shapes of the curved bar profile and curved channel profile are mere examples and variations in profile shape may occur. In some embodiments, center zone 304 may also be referred to as a curved bar profile deposition zone. In some embodiments, edge zones 302 may also be referred to as a curved channel profile deposition zone. In some other embodiments, center

zone 304 may be referred to as a curved bar profile deposition zone, and edge zones 302 may be referred to as a curved channel profile deposition zone.

[0053] The curved bar profile film 308 has a decreasing thickness along an x direction from center to edge of wafer 306 and a uniform, or substantially uniform, thickness along a y direction of the wafer. Conversely, the curved channel profile film 307 has an increasing thickness along the x direction from center to edge of wafer 306 and a uniform, or substantially uniform, thickness along a y direction of the wafer. Together, curved bar profile film 308 and curved channel profile film 307 may form a uniform thickness profile film or a complementary profile film stack. The complementary profile film stack has a thickness 309 based on the combined thickness of the curved channel profile film 307 and the curved bar profile film 308.

[0054] As film 307 and film 308 are deposited independently, each film may be deposited under conditions to have a different internal stress. For example, curved bar profile film 308 may have a compressive internal stress, while curved channel profile film 307 may have a tensile internal stress, or vice versa. As film stresses may be superimposed, the stacked film may have a compressive internal stress in areas of the film having a small x/large y coordinate, i.e., corresponding to center zone 304, while the stacked film also has a tensile internal stress in areas of the film having a large x/small y coordinate, i.e., coordinating to edge zones 302, or vice versa. As noted above, the center of the wafer may be considered the origin, e.g., $x=0$ and $y=0$.

[0055] While Figures 3B and 3C show a complementary profile film stack comprising one pair of curved channel profile film 307 and a curved profile film 308, a complementary profile film stack may comprise more than one pair of a curved channel profile film and a curved profile film. The curved channel profile film of a certain pair (e.g., a first pair) may have different properties such as a thickness, stress, stress ratio, materials, compositions, etc. from those of the curved channel profile film of the other pair (e.g., a second pair). Similarly, the curved bar profile film of a certain pair (e.g., the first pair) may have different properties such as a thickness, stress, stress ratio, materials, compositions, etc. from those of the curved bar profile film of the other pair (e.g., the second pair).

[0056] While films 307 and 308 are discussed herein as having opposite types of internal stress, e.g., one film has a compressive internal stress and the other film has a tensile internal stress, in some embodiments both films may have a tensile or compressive internal stress, but different magnitudes of internal stress. This may address wafers that have different magnitudes of x-bow and y-bow even if the both bows are positive or negative. In some embodiments depositing same type stress films may increase throughput.

[0057] In some embodiments, as the wafer bow to be compensated by the backside layers increases, the film thickness may also increase, as a thicker film may generally compensate greater wafer bow. However, greater thicknesses also increase the risk of cracking. Backside films having an internal tensile stress are more prone to cracking as backside films are typically brittle. Thus, in some embodiments a tensile film is deposited prior to a compressive film, as the compressive film deposited on the tensile film will partially counteract the internal tensile stress and reduce the risk of cracking. However, at greater thicknesses of the backside films, the internal stress may still cause the film to crack. For example, a single stack of complementary profile films may exhibit cracking at a total film thickness of 1.25 μm . Cracking is undesirable as it may reduce the wafer bow compensation of the layer as well as cause defects and potential etching during later fabrication operations and even contaminate and/or damage the processing chamber.

[0058] To address this concern, a complementary profile film stack including alternating non-uniform profile films may be used that has a higher film cracking margin compared to an equivalent thickness single pair film. In some implementations, a complementary profile film stack including alternating non-uniform profile films may be deposited, where each other film has a curved channel profile or a curved bar profile. Figures 3D-3G present various implementations for a complementary profile film stack including alternating non-uniform profile films on a substrate 306 having one or more frontside layers 305. In Figure 3D, films 307 and 308 are alternated to form an alternating stack film 340 having films 308-1, 308-2, 308-3, and 308-N and films 307-1, 307-2, 307-3, and 307-M. In some embodiments, $N=M$, i.e., an alternating stack has an equal number of curved bar profile films and curved channel profile films. In other embodiments, $N \neq M$, such that there are more or fewer curved bar profile films than curved channel profile films.

[0059] The alternating stack film 340 may compensate greater amounts of wafer bow from frontside layers than a single stack of a curved channel profile film and a curved bar profile film of equivalent thickness may compensate alone. For example, a single pair of complementary profile films may crack at thicknesses of about 1.25 μm , which would compensate for about 250 μm of wafer bow. An alternating stack film (i.e., more than one pair of complementary profile films) having a total thickness of 1.25 μm may similarly compensate about 250 μm of wafer bow, but with a reduced risk of cracking. An alternating stack film may reduce throughput due to depositing multiple complementary profile films rather than a single pair complementary profile films, and thus typically would be undesirable. However, the improved material properties of an alternating film stack provide the numerous benefits discussed herein, including a higher cracking margin and improved thermal stability. In some embodiments, an alternating stack film 340 may

comprise two or more sets of complementary profile films, e.g., two or more sets of a curved bar profile film 308 and a curved channel profile film 307.

[0060] In some embodiments, each of the curved bar profile films 308-1-N and curved channel profile films 307-1-M have the same profile, respectively. In other embodiments, the profiles of one or more non-uniform thickness profile film may be different from the other non-uniform thickness profile films. In some embodiments, a pair of complementary profile films may be defined by a thickness 350, which refers to the thickness of the pair of complementary profile films (e.g., a combination of a curved bar profile film and a curved channel profile film). A thickness 350 of the pair of complementary profile films may be less than about 1 μm or between about 0.5 μm and about 1 μm . In some embodiments, each pair of complementary profile films in an alternating film stack may have the same thickness, which for a four-bilayer stack shown in Figure 3D may have a total thickness between about 2 μm and about 4 μm . In some embodiments, each pair of complementary profile films in an alternating stack may have different thickness.

[0061] Figure 3D presents an illustration where a curved bar profile film 308 is deposited after a curved channel profile film 307 is deposited, which is then repeated four times to provide an alternating stack of 4 pairs of complementary profile films. Figure 3E presents a similar stack except that a curved bar profile film 308-1 is deposited before a curved channel profile film 307-1 is deposited, instead of after. As described above, the number of layers and the thickness profiles illustrated in these figures are exemplary only. More or less than four pairs of the complementary profile films are deposited to optimize the overall bow of the wafer. An additional tensile or compressive internal stress layer may also be added, in between the pair of the complementary films, or as the last layer, as illustrated in Figures 3F and 3G.

[0062] Figures 3F and 3G present illustrations of cap or filler layers that may be deposited. In Figure 3F, a cap layer 342 that has a uniform, or substantially uniform, thickness is deposited. As will be discussed further below, cap layer 342 may be a uniform thickness profile film having a tensile internal stress, a compressive internal stress, or zero or negligible internal stress. A uniform thickness profile film may be deposited after depositing one or more pairs of complementary profile films. In some embodiments, a uniform thickness profile film may be deposited between pairs of the alternating stack of complementary profile films. For example, complementary profile films as described herein may be used to compensate for saddle-shaped wafer bow, e.g., a positive x-bow and negative y-bow. While complementary profile films may reduce the difference in wafer bow between the x-direction and y-direction, the wafer bow from a reference plane (e.g., an xy plane intersecting the wafer) may still be relatively large, e.g., 200 μm or more. For example, a saddle-shaped wafer may have backside layers deposited thereon that change the shape to a bowl

or dome shaped wafer. The difference between x-bow and y-bow is reduced, but the wafer is still bowed. A uniform thickness profile cap layer may compensate for such a wafer bow by having a uniform tensile internal stress or compressive internal stress. As the x-bow and y-bow have been substantially equalized by the complementary profile films, the uniform thickness profile film may thus compensate the remaining wafer bow.

[0063] Figure 3G presents an illustration of a filler layer 344. During deposition of a curved bar profile film 308, a curved bar profile film may have a “center drop,” where the thickness of the film has two maxima offset from a center position of the film at or near radius zero (i.e., at or near the wafer center), and at radius zero the thickness of the film is less than the maxima. This difference in thickness may be insubstantial for small thicknesses of complementary profile films, e.g., less than about 1 μm . However, for larger thicknesses of a complementary profile film stack or an alternating stack of complementary profile films having a large overall thickness, e.g., greater than about 2 μm or greater than about 2.5 μm , the center drop may become noticeable and affect the flatness of the film. Thus, a filler layer 344 may be deposited to fill the gap formed in the curved bar profile film. In some embodiment, a filter layer 344 may be deposited to fill the gap formed in the curved channel profile film, for example, where the alternating stack film 340 is formed similarly to that of Figure 3D. Filler layer 344 may be deposited using similar techniques as curved bar profile 344 with a sharper taper in thickness as a function of radius.

[0064] In some embodiments, an alternating stack of complementary profile films may have pairs of complementary profile films having different properties such as thickness, stress, stress ratio, materials, compositions, etc., Figure 3H illustrates an alternating stack of complementary profile films where the order of deposition for pairs of complementary profile films changes. Curved channel profile film 327-1 is deposited first, followed by curved bar profile films 328-1 and 328-2. In some embodiments, curved bar profile film 328-1 and curved bar profile film 328-2 may have different properties as described herein or the same properties. Then, a curved channel profile film 327-2 may be deposited last and may, in some embodiments, have different properties as described herein or the same properties as curved channel profile film 327-1.

[0065] Figure 3I illustrates another alternating stack of complementary profile films where the order of deposition for pairs of complementary profile films changes. In Figure 3I, curved bar profile film 338-1 is deposited first, followed by curved channel profile films 337-1 and 337-2. In some embodiments, curved channel profile film 337-1 and curved channel profile film 337-2 may have different properties as described herein or the same properties. Then, a curved bar profile film 338-2 may be deposited last and may, in some embodiments, have different properties as described herein or the same properties as curved bar profile film 338-1.

[0066] Figure 3J illustrates an alternating stack of complementary profile films where each pair of complementary profile films has a different thickness. Curved channel profile film 347-1 and curved bar profile film 348-1 may have a first thickness 342. Curved channel profile film 347-2 and curved bar profile film 348-2 may have a second thickness 344. First thickness 342 is larger than second thickness 344. In some embodiments, curved channel profile film 347-1 and curved bar profile film 348-1 may have different properties than curved channel profile film 347-2 and curved bar profile film 348-2, respectively, in addition to the different thickness. For example, as discussed further below, pairs of complementary profile films may be defined by a stress ratio between the internal compressive stress and the internal tensile stress of each complementary profile film in a pair of complementary profile films. In some embodiments, a complementary profile film stack including an alternating stack of complementary profile films having different stress ratios, e.g., where each pair of complementary profile films have different properties, may reduce wafer bow more than a complementary profile film stack having a single stress ratio.

[0067] A complementary profile film stack including an alternating stack of complementary profile films may have various advantages over a single pair of complementary profile films. As noted above, an alternating stack of films may have a higher cracking margin. This may result from the compressive stress film applying a compressive stress on the tensile stress films, reducing the internal tensile stress at the exterior edge of the tensile stress film and thus reducing the risk of cracking.

[0068] Figures 4A-B provide graphs of internal stress times thickness for two films along a x-axis measured from center-to-edge of a wafer. In Figure 4A, the tensile film is deposited with a curved channel profile, while the compressive film is deposited with a curved bar profile. The stacked film has an internal stress based on the combination of the two films, and thus has a compressive stress (negative values in Figure 4A) for small x-values (e.g., about up to 100 mm along the x-axis from the center) and a tensile stress (positive values) for large x-values (e.g., from about 100 mm to the edge of the wafer along the x-axis).

[0069] Figure 4B shows a different combination of films, where the tensile film is deposited with a curved bar profile, while the compressive film is deposited with a curved channel profile. The stacked film has an internal stress based on the combination of the two films, and thus has a tensile stress (positive values in Figure 4B) for small x-values (e.g., about up to 100 mm along the x-axis from the center) and a compressive stress (negative values) for large x-values (e.g., from about 100 mm to the edge of the wafer along the x-axis). The result of the stacked film is an anisotropic internal stress that changes across the x- and y-directions of the film, as shown for the x-axis in Figures 4A and 4B.

[0070] In various embodiments, two films may be deposited according to the graphs of either Figure 4A or 4B. In some embodiments, additional backside layers may be deposited. The graphs of Figures 4A and 4B are examples, and films as-deposited may have stress profiles that vary from those shown. For example, as discussed further herein, the internal stresses of both films may be controlled based upon the identified amount of bowing/internal stress of a wafer.

[0071] It is generally desirable to model the wafer bow compensation that may be achieved by complementary profile film stacks as described herein. In some embodiments, to model this wafer bow compensation, a complementary profile film stack may be deposited on a bare wafer that has zero or negligible bow, i.e., is flat or substantially flat. The wafer bow from complementary profile film stacks, which may also be called backside films, may be determined experimentally by depositing the films on a bare wafer that does not have any other films deposited thereon, including frontside films. The wafer bow caused by the complementary profile film stack may be measured and used to determine how the complementary profile film stack may reduce wafer bow on a production wafer having pre-existing wafer bow from one or more frontside layers. However, when the complementary profile film stacks are later deposited on wafers having frontside films, the performance of the complementary profile film stacks on wafers having frontside films is typically different than the performance of the complementary profile film stacks on bare wafers without frontside films. Understanding this relationship and selecting a backside film that performs optimally given a pre-existing wafer bow is desirable.

[0072] Disclosed herein are methods for modelling how backside films will affect wafer bow given various frontside films. For example, a given backside film, such as a complementary profile film stack, may reduce the delta bow of an incoming wafer shape differently depending on the ratio of x-bow and y-bow of the incoming shape and the ratio of compressive internal stress and tensile internal stress of the complementary profile film stack. A model may be constructed to help determine which complementary profile film stack may most efficiently reduce the wafer bow for a particular incoming wafer shape. Greater efficiency in mitigating wafer bow is preferable as a thinner, more efficient film can mitigate the same amount of delta bow as a thicker, less efficient film. The thinner, more efficient film can thus be deposited in less time, resulting in increased throughput and reduced material manufacturing, and/or operational cost.

[0073] Additionally, the minimal wafer bow achievable by a particular complementary profile film stack may be modelled. As noted below, a complementary profile film stack may mitigate x-bow and y-bow differently depending on a stress ratio of the films and the shape of the incoming wafer. Typically, the wafer bow caused by a complementary profile film stack is not a perfect complement to the incoming wafer shape, thus the wafer may not be completely flattened by a

complementary profile film stack regardless of the thickness of the complementary profile film stack. For example, an incoming wafer shape may have an x-bow of 150 μm and a y-bow of -100 μm , having a delta bow of 250 μm . A complementary profile film stack may be deposited that compensates 150 μm of x-bow, but only compensates -75 μm of the y-bow, resulting in a compensated delta bow of 25 μm . While the thickness of the complementary profile film stack could be increase to compensate -100 μm of y-bow, the x-bow may then be compensated by 200 μm , resulting in a compensated delta bow of 50 μm . Thus, no matter the thickness of the complementary profile film stack (e.g., film thickness 309), the residual wafer bow will always be at least 25 μm or 10% (residual bow may be measured as a fraction of compensated delta bow / incoming delta bow). In some embodiments, there is an optimal thickness of the complementary profile film stack that may result in a minimum overall wafer bow. A thinner or thicker film than the optimal thickness would have a greater residual delta bow after depositing the film stack as the film stack cannot completely mitigate the delta bow, as illustrated by the example above and discussed further below in relation to Figures 6A-C.

[0074] Each of these effects may be simulated for various incoming wafer shapes and backside film stacks. In some embodiments, the simulations may test imaginary incoming wafer shapes to model the relationship between the complementary profile film stacks and the incoming wafer shapes to optimize the delta bow. In some embodiments, at least about 10, at least about 100, or between about 10 and about 100 different incoming wafer shapes may be simulated. In some embodiments, at least about 10, at least about 100, or between about 10 and about 100 different backside film stacks may also be simulated. The incoming wafer shapes and backside film stacks may then be combined to determine a resulting wafer shape. The resulting wafer shapes, or compensated wafer shapes, may then be analyzed to determine various properties, such as x-bow, y-bow, and delta bow. Thus, in some embodiments, more than about 1000 or more than about 10,000 different combinations of incoming wafer shapes and complementary profile film stacks may be simulated. In some embodiments, 10 or more or 100 or more different incoming wafer shapes are modelled against 10 or more or 100 or more complementary profile film stacks, resulting in 100 or more, 1000 or more, or 10,000 or more combinations. This data may then be analyzed and used to determine optimal process recipes to perform for a particular incoming wafer shape, which may be used to design or modify recipes as various wafer shapes are encountered during production.

[0075] In some embodiments, wafer bow from frontside films may be modelled based on an x-direction stress and y-direction stress, or an x-bow and y-bow. The shape of a wafer will change based on the x-bow and y-bow. For example, multiple wafers may have a particular delta bow,

which is the difference between the x-bow and y-bow, that is the same for each wafer. However, the stresses causing that delta bow may differ, resulting in various wafer shapes where, e.g., the y-bow may be exceptionally large and the x-bow relatively small, but the delta bow is the same as another wafer having equal x-bow and y-bow.

5 [0076] Figures 5A and 5B illustrate two exemplary backside stack films, stack film A and stack film B, simulated as applied to the backside of various exemplary incoming wafer shapes. Both of stack films A and B are complementary profile film stacks as described herein, having a curved bar profile film having a tensile internal stress and a curved channel profile film having a compressive internal stress, where the curved bar profile film is deposited with a decreasing
10 thickness as a function of the x-axis (similar to the profiles shown in Figures 3A-C). In Figures 5A and 5B, the lines marked with squares indicate y-bow, while the non-marked lines indicate x-bow. In Figure 5A, the left chart indicates the x-bow and y-bow of a complementary profile film stack film A. Also shown in Figure 5A are incoming shapes 502a-c having the same delta bow, but the x-bow and y-bow are different for each shape. Shape 502a has equal x-bow and y-bow,
15 while shape 502b has a greater x-bow than y-bow and shape 502c has a greater y-bow than x-bow.

[0077] When stack film A is applied to a bare wafer, the delta bow of the resulting wafer is 190 μm . However, when stack film A is applied to any of incoming shapes 502a-c, the change in the delta bow is less than 190 μm for each of compensated shapes 503a-c. This difference in change of delta bow between a flat wafer and a wafer having pre-existing bow may be described as the
20 efficiency of the backside film stack to address the incoming wafer bow. Efficiency is an important metric to evaluate backside films, as the efficiency of a backside film in addressing wafer bow directly correlates with the thickness of the film. The greater the efficiency, the thinner the backside film required to address the same wafer bow, which improves throughput and reduces cost by reducing time and resources spent in depositing backside films. Generally, greater
25 efficiency is preferable.

[0078] As shown in Figure 5A, the change in delta bow for each shape after applying stack film A is between about 104 μm and about 109 μm . The efficiency of stack film A for each incoming wafer shape may be determined as the percentile ratio of the change in delta bow for each shape vs the delta bow of the stack film when applied to bare wafers. Thus, for incoming wafer shape
30 502a, the change in delta bow was 108 μm , and $108/190 = 57\%$ efficiency. Notably, the efficiency may be different for different compensated shapes 503a-c, indicating that the incoming wafer shape may affect the efficiency of the backside films.

[0079] Figure 5B presents a backside stack film B having a different wafer shape when

deposited on a flat silicon wafer. When stack film B is applied to a bare wafer, the delta bow of the resulting wafer is 196 μm . Stack film B was similarly applied to incoming wafer shapes 502a-c, resulting in compensated shapes 507a-c. As with respect to a stack film A, the efficiency may be different for different compensated shaped shapes 507a-c. Notably, the change in delta bow and efficiency of stack film B is significantly higher than the comparable delta bow and efficiency of stack film A, having an efficiency of between about 67% and about 69%. Thus, stack Film B is generally preferable over stack Film A to compensate the wafer bow of shapes 502a-c, as the efficiency of stack Film B is higher, allowing for a thinner, and thus less time-consuming and expensive, stacked film to be deposited. As illustrated by Figure 5A and 5B, different film stacks may address the delta bow differently for the same incoming wafer shape, and the same film stack may address the delta bow differently for different incoming wafer shapes, and both.

[0080] In some embodiments, the efficiency of various complementary profile film stacks may be modeled based on a stress ratio of the compressive non-uniform profile film to the tensile non-uniform profile film. The stress ratio may represent the relationship between the compressive stress and the tensile stress of the complementary profile films (which may result in a stress distribution as shown in Figures 4A-B). As internal stress also correlates with wafer bow, the stress ratio may also represent the x-bow and y-bow of the complementary profile film stack; a higher magnitude ratio indicates a greater internal compressive stress compared to the internal tensile stress of the complementary profile films. For stack film A and stack film B, stack film A has a stress ratio of -9, while stack film B has a stress ratio of -3 (the ratio is negative because compressive and tensile stress have opposite signs to indicate the type of internal stress). While stack films A and B include a curved bar profile film having a tensile internal stress and a curved channel profile film having a compressive internal stress, suitable modifications may be made to use a complementary profile film stack having a curved bar profile film having a compressive internal stress and a curved channel profile film having a tensile internal stress.

[0081] Figure 5C presents three charts 571a-c illustrating curves of efficiency vs stress ratio for an incoming wafer shape having different amounts of incoming delta bow, e.g., wafer shape 502a but at a total delta bow of 200 μm , 344 μm , and 600 μm . As shown in Figure 5C, the optimal stress ratio may change as the incoming delta bow of the incoming wafer shape changes between 200 μm , 344 μm , and 600 μm . For chart 571a, the optimal stress ratio (shown as HCN/HTN) is about -4, having an efficiency of about 78%. Higher or lower stress ratios would result in a complementary profile film stack having a decreased efficiency in mitigating wafer

bow. For chart 571b, which has an incoming wafer shape as shown in Figures 5A-B, the optimal stress ratio is about -5 with an efficiency of about 69%. For chart 571c the optimal stress ratio is about -6 with an efficiency of about 56%. Each efficiency curve may be generated by simulating the effect of various complementary profile stack films on wafer bow for an incoming wafer shape, determining the compensated wafer delta bow, and determining an efficiency of each complementary profile stack film. While film A and film B are shown in Figure 5C, the curves may be determined from multiple complementary profile film stacks having varying stress ratios. Each complementary profile film stack may be simulated on an incoming wafer shape, and a curve of efficiency vs stress ratio may be constructed.

- 10 **[0082]** In some embodiments, each complementary profile film stack may be modelled using a normalized thickness of the complementary profile film stack (e.g., thickness 309, above). Normalizing for thickness may improve the utility of the efficiency metric as the wafer bow compensated by a complementary profile film stack will vary with thickness; thicker films generally compensate more wafer bow. Furthermore, as the thickness of the films is a significant factor in the time and cost of depositing the films, normalizing the thickness of the complementary profile film stacks enables a better comparison across films to determine an optimal film for compensating an incoming wafer shape.

- [0083]** In some embodiments, a complementary profile film stack to be modelled may be an alternating stack of pairs of complementary profile films, as discussed above in relation to Figures 3D-J. In such embodiments, each pair of complementary profile films included in the alternating stack may have different properties, for example different stress ratios. In some embodiments, a first pair of complementary profile films may have a first stress ratio, and then a second pair of complementary profile films may have a second stress ratio. As stresses may be superimposed, the net effect on compensated wafer bow of each pair of complementary profile films in the complementary profile film stack may be modelled. For example, the 2-dimensional chart 571b could be presented as a 3-dimensional chart, where the x-axis represents a stress ratio of a first pair of complementary profile films, the y-axis represents a stress ratio of a second pair of complementary profile films, and the z-axis represents efficiency. In such embodiments, thickness may still be normalized for the total thickness of the complementary profile film stack that includes each pair of complementary profile films. In some embodiments, each pair of complementary profile films may be modelled as having an equal fraction of the normalized thickness, while in other embodiments the relative normalized thicknesses of each pair of complementary profile films may be varied, adding another dimension to the model for determining an optimal efficiency.

[0084] In addition to efficiency, each complementary profile film stack may also be analyzed to determine its flattening percentage. The effect of a complementary profile film stack on the shape of an incoming wafer is typically not a perfect inverse of the wafer bow. Thus, even if the x-bow is perfectly compensated by the complementary profile film stack, a nonzero y-bow may still exist. In such a circumstance, the y-bow may not be reduced without increasing the x-bow, resulting in no net change in delta bow or even an increase in delta bow.

[0085] Figure 6A presents a chart of delta bow as a function of the total thickness of a complementary profile film stack to illustrate this phenomenon. The complementary profile film stack used for wafer bow mitigation shown in Figure 6A may have the same stress ratio but various thicknesses. The incoming wafer shape for Figure 6A is the same as incoming shape 502a, having a delta bow of 344 μm and equal x-bow and y-bow. Stack film B of Figure 5B was simulated as deposited on the backside at thicknesses between 0.5 μm and 3 μm in 0.5 μm increments. The line indicates a curve fit and the blue area indicates a potential error of the curve fit.

[0086] Depositing a backside complementary profile film stack such as stack B will change the bow of the incoming wafer shape. Depositing a backside complementary profile film stack having a thickness of about 0.5 μm may reduce the delta bow, as shown in compensated wafer 602 that has a delta bow of 225 μm . Increasing the thickness of the complementary profile film stack may further reduce the delta bow to a minimum of 155 μm at about a 2 μm thick film as shown in compensated wafer 604. Above that thickness, however, the delta bow will increase, as shown in compensated wafer 606 having a delta bow of 268 μm .

[0087] In some embodiments, the delta bow vs thickness curve has a minimum delta bow because, as the thickness of a complementary profile film stack increases beyond the thickness that results in a minimum delta bow, the x-bow and y-bow may be overcompensated and increase in magnitude in the opposite sign as the original x-bow and y-bow. This trend is illustrated by compensated wafers 602-606. For the incoming wafer shape and compensated wafer 602, the x-bow is negative while the y-bow is positive. Compensated wafer 604 has a large positive and large negative x-bow, and negative y-bow. Compensated wafer 606 has a larger negative y-bow and a larger positive x-bow than compensated wafer 604. As the thickness of the backside film increases from 0 μm to about 2 μm , the magnitude of the x-bow and y-bow decrease, as shown by compensated wafer 602. At compensated wafer 606, however, the magnitude of the x-bow and y-bow have increased with opposite signs from the compensated wafer 602. In some embodiments, this may result from the backside film compensating x-bow and y-bow unequally: the incoming wafer shape has equal x-bow and y-bow, but the change in

x-bow and y-bow across each of compensated wafers 602-606 is unequal. As the backside film can reduce the wafer bow from 344 μm to a minimum of 155 μm , the flattened percentage of the wafer is about 55%, leaving a residual wafer bow of 45% (i.e., 155/344).

[0088] In some embodiments, each different complementary profile film stack may be modeled on an incoming wafer shape to determine compensated delta bow vs total film thickness curves for each complementary profile film stack. Figure 6B shows such curves for complementary profile film stacks having stress ratios of -3, -4, -5, and -6. Each complementary profile film stack, represented by a stress ratio, was simulated as applied to an incoming wafer having a bow of 655 μm at various thicknesses in 0.5 μm steps. A stress ratio of -5 has the lowest minimum at around 5.5 μm total film thickness (i.e., optimal thickness), while stress ratios of -3, -4 or -6 have higher minimums at different total film thicknesses. The table below illustrates the properties of each stack film, including residual bow (which is the percentage of the original wafer bow remaining after depositing the stack film).

Stack film used w/ stress ratio	Wafer delta bow (μm) when most flattened	Optimal thickness (μm)	Residual bow as % of the incoming wafer bow of 655 μm
-6	254	4.5	39%
-5	212	5.5	32%
-4	247	6.5	38%
-3	367	8.5	56%

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[0089] In some embodiments, a cap layer may also be modelled to determine minimum flattening. A cap layer is a uniform internal stress layer, having a uniform profile of tensile or compressive internal stress. A cap layer may be used alone without a complementary profile film stack, or in conjunction with a complementary profile film stack. In some embodiments, this can achieve a similar or better flattening than a complementary profile film stack alone.

[0090] Figure 6C illustrates the combination of complementary profile film stacks and cap layers for three different stress ratios of complementary profile film stacks. Similar to Figure 6B, a complementary profile film stack having a stress ratio of -5 has a minimum delta bow without

any cap layers. For a complementary profile film stack having a stress ratio of -5, a cap layer actually increases the delta bow, regardless of the internal stress of the cap layer. For a complementary profile film stack having a stress ratio of -6, however, a cap layer may decrease the delta bow as shown at 612a (the dotted lines indicate the effect of a cap layer). Similarly, for a complementary profile film stack having a stress ratio of -4, a cap layer may decrease the delta bow as shown at 612b. A major difference between 612a and 612b, however, is the internal stress of the cap layer. For a stress ratio of -6, the cap layer only reduces the delta bow if it has an internal tensile stress. A cap layer having an internal compressive stress would increase delta bow. Inversely, for a stress ratio of -4, the cap layer only reduces the delta bow if it has an internal compressive stress. A cap layer having an internal tensile stress would increase delta bow.

[0091] Figures 6A-C illustrate a complementary profile film stack having a single pair of complementary profile films, but in some embodiments, a complementary profile film stack may include multiple pairs of complementary profile films having the same or different properties, such as stress ratio. In such embodiments, the compensated delta bow may vary based on the thickness of each pair of complementary profile films. Similar to the cap layers graphs shown in Figure 6C, a complementary profile film stack having multiple pairs of complementary profile films having, e.g., different stress ratios, may achieve a smaller compensated delta bow than a complementary profile film stack having a single stress ratio. In some embodiments, charts similar to those shown in Figure 6A-C may be generated based on varying the thickness for each pair of complementary profile films in a complementary profile film stack. For example, a complementary profile film stack having two pairs of complementary profile films having different stress ratios may be used to plot a 3-dimensional chart of compensated delta bow as a function of the thicknesses of each pair of complementary profile films. Other plots may be generated as a function of backside film properties described herein to model and visualize compensated delta bow.

[0092] Figure 7 presents a flowchart for a process of simulating wafer shape according to various embodiments herein. The shape of an incoming wafer may be determined (702). As an example, a measurement module and/or one or more sensors may be used to measure and determine the shape of an incoming wafer. Such module and/or sensors may be integrated to the process chamber or provided separately from the process chamber. The incoming wafer may be a bare wafer having no films deposited on both the frontside and backside of the wafer. The shape of such incoming wafer may be measured or determined to be flat or substantially flat. The incoming wafer may have one or more layers formed on at least one of the frontside and

backside of the wafer. Such one or more layers may be patterned. In some embodiments, shape may be defined by an x-bow and y-bow. In other embodiments, wafer shape may also be determined by internal stresses of the incoming wafer, particularly along perpendicular directions of the wafer, e.g., an x-direction and y-direction. In some embodiments, a wafer shape is selected from a pre-determined group of wafer shapes to best match a wafer being analyzed. For example, wafer bow of production wafers may be influenced by multiple different frontside layers that are computationally intensive to simulate, but can be sufficiently modelled by a single internal stress value for perpendicular directions and a corresponding polynomial function to define a stress distribution in the perpendicular directions. In some embodiments, an incoming wafer may be modelled by selecting a pre-determined wafer shape that best approximates the incoming wafer shape or by modelling the incoming wafer shape using simplified models of internal stress to approximate the incoming wafer shape.

[0093] One or more complementary profile film stack recipes may be selected (704). The recipes selected may be based upon the shape of the incoming wafer. For example, as noted above in relation to Figure 5C, the optimal stress ratio of a complementary profile film stack may depend on the incoming wafer shape. As the incoming wafer shape is known, certain complementary profile film stacks may be filtered and not simulated as they are already known to have poor performance. For example, if an incoming wafer shape was similar to incoming shape 502b, a complementary profile film stack similar to stack film A may not be selected, while stack film B is selected.

[0094] The wafer shape and selected complementary profile film stack recipes are simulated (706). The simulations may involve determine a compensated shape similar to those shown in Figures 5A and 5B. The simulations may also involve determining a flattening possible by each complementary profile film stack, similar to that shown in Figures 6A and 6B. Various data may be derived from the simulations, such as the efficiency of each complementary profile film stack and the minimum delta bow as a function of thickness for each complementary profile film stack.

[0095] In some embodiments, a cap layer may also be optionally simulated (708). The cap layer may be simulated for determining efficiency, thickness, and/or minimum delta bow. For efficiency, the cap layer may be combined with the complementary profile film stack to determine an average efficiency of the total backside film stack. For delta bow, that cap layer may be combined with the complementary profile film stack to determine a minimum thickness achievable when using a both a complementary profile film stack and the cap layer, similar to the charts shown in Figure 5C.

- [0096] A recipe may then be determined based on the simulations (710). In some embodiments, the determined recipe is a pre-selected recipe that has already been validated. In other embodiments, the simulation data may be used to help a process engineer design or modify a recipe to address a particular incoming wafer shape. For example, the simulations may indicate to a process engineer that a particular range of thicknesses and stress ratios may best address wafer bow for a particular incoming wafer shape, and a process engineer may then refine a recipe based on those ranges. As such, as described herein, determining a recipe includes selecting a recipe from the library of recipes, modifying or updating existing recipes, and creating or developing an entirely new recipe.
- [0097] Optionally, in some embodiments the determined recipe is performed (712). The determined recipe may be deposited to mitigate wafer bow of a production wafer having a shape similar to the incoming wafer noted in 702, above. In some embodiments, operation 712 is not performed. In some embodiments, the determined recipe may be used for further development or research of a recipe and is not performed.
- [0098] Figure 8 presents a process flow for developing a model as described herein. Complementary profile film stacks are identified (802). In some embodiments, the complementary profile film stacks may be identified from a library or database of recipes for complementary profile film stacks. In some embodiments, the complementary profile film stacks are identified based on various parameters that may be used to model the effect of the complementary profile film stacks. Such parameters may include stress, stress ratio, stress distribution, thickness, other parameters discussed herein, and any combinations thereof. Figure 9, further described below, indicates parameters that may be used for modelling complementary profile film stacks.
- [0099] In some embodiments, complementary profile film stacks may comprise one or more pairs of complementary profile films, e.g., a compressive layer and a tensile layer. In some embodiments, each pair of the compressive and tensile layers may be defined by a stress ratio (e.g., the ratio of a compressive internal stress to a tensile internal stress), which may be identical or varied through the pairs when more than one pair of complementary profile films of compressive and tensile layers form the complementary profile film stack. In some embodiments, the stress ratio is determined by depositing each complementary profile film stack on a bare wafer and measuring the wafer bow. The wafer bow may then be used to determine the internal stress of the complementary profile film stack. In some embodiments, at least about 10 or at least about 20 different stress ratios are identified. In some embodiments, complementary profile film stacks may be identified based on pre-developed recipes. In some embodiments,

recipes to deposit complementary profile film stacks having a desired stress ratio may be developed and tested to develop data across a range of stress ratios. In some embodiments, stress ratios of the identified complementary profile film stacks may vary from about -1 to about -10.

5 [0100] In some embodiments, each complementary profile film stack may also be defined by a thickness. As noted above, thicker films may mitigate more wafer bow, but there may be a maximum flattening achievable by a complementary profile film stack having a particular stress ratio. Thus, each complementary profile film stack stress ratio may also be modelled with various thicknesses. Thicknesses may range from about 0.5 μm to about 3 μm . In some
10 embodiments, a complementary profile film stack having a particular stress ratio may be modelled in increments of 0.5 μm , but other increments may also be used.

[0101] The combination of stress ratio and thicknesses may result in at least a hundred different complementary profile film stacks. For example, assuming 20 different stress ratios and 6 different thicknesses, about 120 different complementary profile film stacks may be identified. More or fewer stress ratios and thicknesses may also be modelled in various embodiments.

15 [0102] Next, various incoming wafer shapes may be modelled (804). In some embodiments, an incoming wafer shape may be defined by frontside stress having an x-component and a y-component. In some embodiments, stress in a z-component may be ignored to simplify computations. By varying the magnitude and ratios of the stress tensor for each incoming wafer shape, various wafer shapes may be determined. These wafer shapes may approximate wafer
20 shapes that may occur during production from the deposition of multiple frontside layers. In some embodiments, at least 10 or at least 100 different incoming wafer shapes are determined. Each incoming wafer shape may be defined by the frontside stress, which may be used to determine the x-bow, y-bow, and delta bow of the incoming wafer shape.

[0103] Next, each complementary profile film stack and each incoming wafer shape may be
25 combined to simulate the effects of the complementary profile film stack on the wafer bow of the incoming wafer shape (806). This may be done using a finite element method (FEM) model to simulate wafer bow based on frontside and backside layers. As shown in Figures 4A-C and 5A-C, the backside films and wafer shapes may be combined and the resulting wafer bow determined.

30 [0104] In some embodiments, cap layers may also be additionally simulated (808). As noted above, a cap layer may be used in addition to a complementary profile film stack to address wafer bow. In some embodiments, cap layers having a uniform internal tensile stress or a uniform internal compressive stress may be simulated. In some embodiments at least about 10

different cap layers may be simulated, including various magnitudes of internal stress and various thicknesses.

[0105] The properties of the simulated compensated wafers may then be determined (810). In some embodiments, properties may include the final wafer bow, including the delta bow as well as the x-bow and y-bow. In some embodiments properties may include an efficiency of each complementary profile film stack when applied to each incoming wafer shape. In some embodiments, properties may include a flattening percentage of each complementary profile film stack when applied to each incoming wafer shape (e.g., a percent reduction in delta bow) or a residual bow of the wafer after applying the complementary profile film stack (e.g., a percent of the original delta bow remaining). In some embodiments, properties may also include an optimal thickness or optimal stress ratio for each incoming wafer shape. The complementary profile film stack having the greatest efficiency or the greatest flattening percentage for a particular incoming wafer shape may be determined.

[0106] The relationships between complementary profile film stacks and incoming wafer shapes may be modelled (810). In some embodiments, modelling may include generating charts of efficiency vs stress ratio as shown in Figure 4C or charts of residual bow vs film thickness as shown in Figure 5C. In some embodiments, modelling may involve determining one or more relationships between incoming wafer shapes and backside film stacks, including complementary profile film stacks and cap layers. In some embodiments, relationships modelled may include stress ratios of complementary profile film stacks to stress ratios of frontside films for incoming wafer shapes. These models and relationships may then be used as shown in Figure 6 to identify which process recipe to use to compensate an incoming wafer bow.

[0107] In some embodiments, the simulated combinations of incoming wafer shapes and complementary profile film stacks may be calibrated against empirical data. A depth of experiment (DOE) may be performed on coupon wafers to determine the deposition profiles of non-uniform profile films as well as on coupon wafers having frontside films deposited thereon to simulate incoming wafer shapes. The deposition profile of the experimental films and the deposition profile of the simulated films may be compared and the model calibrated to minimize differences between the simulated deposition profile and the experimental deposition profile. In some embodiments, the model may be refined to minimize a cost function between the simulated deposition profile and the experimental deposition profile.

[0108] In some embodiments, simulations described herein may be performed using a FEM modelling software. Figure 9 illustrates a graphical user interface for a FEM model that can

simulate frontside and backside films to determine wafer bow. Inputs to the model may include the compressive internal stress and tensile internal stress of a complementary profile film stack (e.g., HCN_stress for high compressive silicon nitride and HTN_stress for high tensile silicon nitride). In some embodiments, inputs may include a parabolic or polynomial function to model the stress distribution. For example, a stress distribution as shown in Figures 4A-B, above, may be used, or other stress distributions may be used. In some embodiments, the stress distributions may be determined empirically by fitting a polynomial function to metrology data of wafer bow for films having one or more frontside and one or more backside films deposited thereon as described herein. Additional inputs may also be included, such as second, third, fourth, etc. HCN_stress and HTN_stress, for modelling complementary profile film stacks having multiple pairs of complementary profile films. Additional inputs may also include compressive and tensile layers of materials other than silicon nitride. Inputs may also include a cap layer stress and thickness (e.g., HTN_cap_stress and HTN_cap_thk). Additional inputs may also be included, such as second, third, fourth, etc. cap layer stress and thicknesses. Inputs may also include frontside stress in an x-direction and y-direction (FS_stress_x and FS_Stress_y). Inputs may also include a stack thickness and frontside film thickness. The outputs of the FEM model may include an x-bow and y-bow, as well as various parameters for visualizing the wafer bow.

[0109] In some embodiments, the FEM model may simulate wafer bow using a FEM method with various simplifications. For example, the wafer may be treated as shell while the films are treated as membranes on the shell. Treating the wafer as a shell may simplify calculations as the wafer is treated as a two-dimensional plane rather than a three-dimensional object. This simplification dramatically reduces computation time with a negligible reduction in accuracy of the output. In some embodiments, this simplification has a negligible reduction in accuracy because of the large difference in thickness between the wafer (~800 μm) and the films (e.g., about 1 to about 3 μm), as well as the large difference between the thickness of the films and the diameter of the wafer (300 mm). In some embodiments, the films deposited on the wafer may be treated as membranes without any bending stiffness.

[0110] In some embodiments, the model may be configured to apply the frontside stresses and/or backside stresses according to particular stress distributions. For example, in some embodiments, a complementary profile film stack may be modelled as having a parabolic stress distribution along an x-direction and a uniform stress distribution along a y-direction. In some embodiments, the stress distribution may be modified based on DOE experiments as noted above to better approximate experimental results.

[0111] In some embodiments, the FEM model may be used to simulate the combination of

incoming wafer shapes and backside film stacks to generate data as described in Figures 7 and 8. In some embodiments, the FEM model may be able to simulate a single combination in less than about 30 seconds using an average commercial laptop, allowing for the simulation of large numbers of combinations much faster than a FEM model that treats the wafer and films as a 3D object. The reduced complexity of the FEM model causes an increased computational speed that allows for faster and more efficient simulation of wafer bow.

[0112] Example materials used to make backside layers having tensile internal stress include silicon nitrides (SiN), silicon oxynitrides, and polymer layers. As examples, tensile films can be deposited using CVD or PECVD techniques. To combat wafer bow caused by a frontside layer with a compressive internal force, a compressive film may be used for the bulk backside layers. Compressive films may be formed using specific materials and/or processing conditions. Example materials used to make compressive films include silicon oxides (SiO_x), silicon nitrides, aluminum oxides, aluminum nitrides, and polysilicon. Compressive films can be deposited using CVD or PECVD techniques. The above-recited materials and deposition techniques may apply to any one or more backside layers in a multilayer backside stack. Any two backside layers may be formed by the same or different techniques.

[0113] Deposition by PECVD may proceed by flowing a reactant into a process chamber, and optionally with a co-reactant, while exposing the bowed semiconductor substrate to plasma. The plasma may drive a gas phase reaction that results in deposition of film. The PECVD reactions may generally involve delivering reactant(s) to the semiconductor substrate continuously while the semiconductor substrate is exposed to plasma. In some embodiments, depositing a nitride film on the backside of the substrate includes exposing the backside of the flat and/or bowed semiconductor substrate to a silicon-containing precursor and a nitrogen-containing reactant, and exposing the backside of the semiconductor substrate to plasma to drive a reaction between the silicon-containing precursor and the nitrogen-containing reactant to deposit the nitride film. To protect the frontside of the semiconductor substrate on which circuits, transistors, and other device components are patterned during the backside processes, the frontside is protected from being exposed to plasma and/or reactant or process gases, for example, by keeping the gap between the frontside of the semiconductor substrate and the showerhead to less than plasma sheath and/or by flowing inert gas(es) onto the frontside of the semiconductor substrate. By depositing on the backside of the semiconductor substrate, the nitride film avoids being deposited on circuits, transistors, and other device components on the frontside of the bowed semiconductor substrate.

[0114] In some embodiments, the curved bar profile and curved channel profiles described herein may be achieved by controlling precursor concentration adjacent to the bowed

semiconductor substrate during deposition. In the present disclosure, precursor concentration adjacent to the bowed semiconductor substrate may be controlled by design features in a showerhead pedestal. Such design features may influence flow dynamics of the precursor from the showerhead pedestal. In some implementations, the showerhead pedestal may be divided into multiple zones as shown in Figure 3A. For example, precursor gas may be delivered in a first zone and inert gas may be delivered in a second zone, and/or different flow rates or concentrations of precursor and inert gas may be delivered to different zones to control the thickness and/or properties of the films deposited in different zones. This modulates the concentration of precursor gas adjacent to the bowed semiconductor substrate. In some implementations, the precursor gas may be delivered via a first supply tube and the inert gas may be delivered via a second supply tube.

Apparatus

[0115] In some embodiments, Figure 10A is a block diagram that illustrates a substrate processing system 1032 used to perform processing on a wafer 1002, according to some embodiments. As shown, the substrate processing system may include a processing chamber (or a chamber) 1034. A center column may be configured to support a pedestal for when a top surface (or a frontside) of the wafer 1002 is being processed, e.g., a film is being formed on the top surface of the wafer 1002, or on the backside of the wafer 1002. The pedestal, in accordance with some embodiments disclosed herein, may be referred to as a showerhead pedestal (“ShoPed”) 1006. A showerhead 1036 may be disposed over the ShoPed 1006.

[0116] In some embodiments, the showerhead 1036 may be electrically coupled to power supply 1038 via a match network 1040. The power supply 1038 may be controlled by a control module 1042, e.g., a controller. In some embodiments, power may be provided to the ShoPed 1006 instead of the showerhead 1036, or power may be provided to both the ShoPed 1006 and the showerhead 1036. The control module 1042 may be configured to operate the substrate processing system 1032 by executing process input and control for specific process recipes. Depending on whether the top surface of the wafer 1002 is receiving a deposited layer or layer stack or the bottom surface of the wafer 1002 is receiving a deposited layer or layer stack, the controller module 1042 may set various operational inputs for a process recipe, such as power levels, timing parameters, process gasses, mechanical movement of a wafer 1002, and/or the height of the wafer 1002 relative to the ShoPed 1006 (and the distance between the wafer 1002 and the showerhead 1036).

[0117] In some embodiments, the center column may also include lift pins, which are controlled by a lift pin control. Such lift pins may be used to raise the wafer 1002 from the ShoPed 1006 to

allow an end effector (not shown) to pick the wafer and to lower the wafer 1002 after being placed by the end effector. The end effector may also place the wafer 1002 over spacers 1044. As will be described below, the spacers 1044 may be sized to provide a controlled separation of the wafer 1002 between a bottom surface of the showerhead 1036 (facing the wafer) and a top surface of the ShoPed 1006 (facing the wafer).

[0118] In some embodiments, the substrate processing system 1032 may further include a first gas manifold 1046 that is connected to first gas sources 1048, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the purposes and processing being performed over a top surface of the wafer 1002, the control module 1042 may controls the delivery of first gas sources 1048 via the first gas manifold 1046. The chosen gases may then be flown into the showerhead 1036 and distributed in a space volume defined between a face of the showerhead 1036 that faces that wafer 1002 when the wafer is resting over the pedestal or ShoPed.

[0119] In some embodiments, the substrate processing system 1032 may further include a second gas manifold 1050 that is connected to second gas sources 1052, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a bottom surface of the wafer 1002, the control module 1042 may control the delivery of second gas sources 1052 via the second gas manifold 1050. The chosen gases may then be flown into the showerhead 1036 and distributed in a space volume defined between a face of the ShoPed 1006 that faces an under surface or under side (e.g., backside) of the wafer 1002 when the wafer is resting over the ShoPed 1006 and/or spacers 1044. The spacers 1044 may provide for a separation that optimizes deposition to the under surface of the wafer 1002, while reducing deposition over the top surface of the wafer 1002. In some embodiments, while deposition is targeted for the under surface of the wafer 1002, an inert gas may be flown over the top surface of the wafer 1002 via the showerhead 1036, which may push reactant gases away from the top surface and enable reactant gases provided from the ShoPed 1006 to be directed to the under surface of the wafer 1002. Spacers 1044 and/or other similar substrate support features may be used to provide controlled separation between the wafer and the ShoPed and the showerhead. Spacers 1044 and/or other similar substrate support features may be connected or supported by the ShoPed such that the wafer (or its reference plane, when the wafer is bowed) may maintain an even and/or parallel distance from the top surface of the ShoPed, even when there is an unwanted movement or oscillation at the system or chamber level.

[0120] In some embodiments, either showerhead 1036 or ShoPed 1006, or both, may have a zonal deposition design similar to that shown in Figure 3A. For example, gas manifold 1050 may be fluidically linked to control the delivery of gases to either zones 302 or zone 304. By controlling

the flow of gases to either zones 302 or zone 304 films may be deposited as shown in Figures 3B and 3C. In some embodiments, either showerhead 1036 or ShoPed, or both, may have a zonal deposition design different from that shown in Figure 3A. For example, with reference to Figure 7, when the bowing of wafer is measured or identified (702), a showerhead and/or ShoPed that
5 has corresponding zonal deposition design to that specific wafer may be used to deposit films to the backside of the wafer, or gas flows through a showerhead and/or ShoPed may be tuned to correspond to the profile of the wafer bow.

[0121] Further, the gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct gases are delivered during the deposition
10 and plasma treatment phases of the process. Process gases may exit the chamber 1034 via one or more exhausts or outlets. A vacuum pump (e.g., a one or two stage mechanical dry pump and/or a turbomolecular pump) may draw process gases out and maintains a suitably low pressure within the reactor by a close loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0122] In some embodiments, a carrier ring 1054 may encircle an outer region of the ShoPed
15 1006. When the top surface of the wafer 1002 is being processed, e.g., a material is being deposited thereon, the carrier ring 1054 may be configured to sit over a carrier ring support region that is a step down from a wafer support region in the center of the ShoPed 1006. The top surface of the carrier ring 1054 is generally coplanar with the top surface of the wafer 1002. The carrier
20 ring 1054 may include an outer edge side of its disk structure, e.g., outer radius, and a wafer edge side of its disk structure, e.g., inner radius, that is closest to where the wafer 1002 sits. The carrier ring 1054 may be associated with an inner diameter (ID). The inner diameter may extend to an inner perimeter of the carrier ring and generally surround a substrate (e.g., wafer 1002) in a processing chamber. The wafer edge side of the carrier ring 1054 may also include a plurality of
25 contact support structures or “tabs” which may be configured to lift the wafer 1002 when the carrier ring 1054 is held by the spacers 1044. The carrier ring 1054 may include a plurality of tabs with a quantity selected from a range to support the wafer 1002 during processing. Additional details regarding embodiments of the tabs will follow. In some embodiments, a wafer may be placed directly upon, or supported directly by, spacers or other similar substrate support features
30 without a carrier ring.

[0123] Figure 10B is a block diagram that illustrates another version of substrate processing system 1032 used to perform processing on the wafer 1002, according to some embodiments. In some embodiments, spider forks 1056 may be used to lift and maintain the carrier ring 1054 in its process height, e.g., to allow depositing in the under surface (backside) of the wafer 1002. The

carrier ring 1054 may therefore be lifted along with the wafer 1002. In some implementations, the carrier ring 1054 may be rotated to another station, e.g., in a multi-station system. In some embodiments, a spider forks or any other transfer mechanism may be used to lift or move the wafer directly without a carrier ring.

5 **[0124]** Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead 936) and a ShoPed 906. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination of
10 showerhead and pedestal, which enables deposition on a backside of the wafer. The electrode geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal or ShoPed may include an embedded controlled heater (or distributed heater or heater elements), wafer lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer
15 of wafers and the processing of gasses with or without RF power from the pedestal.

[0125] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the ShoPed, showerhead, and/or electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may
20 be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0126] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may
25 further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0127] In some embodiments, the gap between the side of the wafer that does not need plasma/deposition may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the
30 system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 mm (limited by the wafer bow), and such gap can be controlled. The gap maybe controlled depending on process conditions.

[0128] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b)
35 selective design of hole patterns on the ShoPed to selectively deposition film in different areas of

the backside of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0129] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 954 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0130] Figure 11A shows a cross-sectional view of an edge region of the ShoPed 1006. This view provides a cross-sectional representation of the carrier ring 1054, which has a carrier ring inner radius 1054a and a carrier ring outer radius 1054b. In some embodiments, the carrier ring 1054 includes support extensions 1054c, which extend below the substantial flat surface of the carrier ring 1054.

[0131] The support extensions 1054c are configured to mate and sit within support surfaces defined into a top surface of the spacers 1044. The support surfaces provide a complementary mating surface for the support extensions 1054c, such that the carrier ring 1054 is prevented from sliding or moving when supported by the spacers 1044. Although three spacers are shown as spacers 1044 are shown in Figure 7B, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 1006, and spacing is defined for supporting wafer 1002 at a spaced apart relationship from a top surface of the ShoPed 1006.

[0132] Further shown is that a top surface of the ShoPed 1006 will include a hole pattern 1006a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 1006a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 1006 and extend to an outer periphery of the ShoPed 1006. At least one hole pattern 1006a is provided at an edge hole region 1007 of

the hole pattern, and orifices defined in the edge hole region 1007 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 1006.

[0133] In one example, the angle or tilt at which the orifices in the edge hole region 1007 is defined to tilt or angle away from the center of the ShoPed 1006. In one embodiment, the angle is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 1007, additional distribution of process gases can be provided during backside deposition of the wafer 1002. In one embodiment, the remainder orifices 1006d of the hole pattern 1006a are oriented substantially perpendicular to the surface of the ShoPed 1006 and directed toward the underside of the wafer 1002.

[0134] Figure 11B illustrates that when the wafer 1002 is held by the carrier ring 1054, the wafer 1002 edge will sit on an edge region closer to the carrier ring inner radius 1054a of the carrier ring 1054. The surface of the showerhead 1036 facing the top surface of the wafer 1002, when positioned using spacers 1044, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the wafer 1002.

[0135] By way of example, the distance between the top of the wafer 1002 and the surface of the showerhead 1036 is preferably between about 2 mm to about 0.5 mm, and in some embodiments about 1 mm to about 0.5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about 0.5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about 0.5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 1036 is configured to supply an inert gas flow over the top side of the wafer 1002 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 1006.

[0136] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., VECTOR® DT product lines and ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0137] Figure 12 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 1200 includes a transfer module 1203. The transfer module 1203 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 1203 is a multi-station reactor 1209 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-

station reactor 1209 may include multiple stations 1211, 1213, 1215, and 1217 that may sequentially perform operations in accordance with disclosed embodiments. Stations may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0138] Mounted on the transfer module 1203 may be one or more single or multi-station modules 1207 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 1200 also includes one or more wafer source modules 1201, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 1219 may first remove wafers from the wafer source modules 1201 to loadlocks 1221. A wafer transfer device (generally a robot arm unit) in the transfer module 1203 moves the wafers from loadlocks 1221 to and among the modules mounted on the transfer module 1203.

[0139] In various embodiments, a system controller 1242 is employed to control process conditions during deposition. The system controller 1242 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0140] The system controller 1242 may control all the activities of the deposition apparatus. The system controller 1242 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 1242 may be employed in some embodiments.

[0141] The depicted embodiment includes a user interface associated with the system controller 1242. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0142] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by “programming.” Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language.

[0143] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may
5 be hard coded.

[0144] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

10 [0145] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 1242. The signals for controlling the process are output on the analog and digital output connections of the system 1200.

[0146] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of
15 the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0147] In some implementations, a system controller 1242 is part of a system, which may be
20 part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as
25 the “controller,” which may control various components or subparts of the system or systems. The system controller 1242, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching
30 circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

System Controllers

- [0148] Broadly speaking, a controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. Such controller may be used in or with any of the apparatus described herein. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.
- [0149] A system controller may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, a system controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0150] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module,
5 an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0151] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool
10 components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0152] A system controller may include various programs. A substrate positioning program
15 may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control program may include code for controlling gas composition, flow rates, pulse times, and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control
20 program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck.

[0153] Examples of chamber sensors that may be monitored during deposition include mass
25 flow controllers, pressure sensors such as manometers, and thermocouples located in the pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0154] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used
30 in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of the following steps, each step provided with a number of possible tools: (1) application of
35 photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of

photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and
5 (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

[0155] Certain embodiments disclosed herein relate to computational systems for generating and/or using models. Certain embodiments disclosed herein relate to methods for generating and/or using a model implemented on such systems. A system for generating a model may be configured to analyze data for calibrating or optimizing the expressions or relationships used to
10 represent the classification of, source of, or remedies for a defect on a substrate. A system for generating a model may also be configured to receive data and instructions such as program code representing physical processes occurring during the semiconductor device fabrication operation. In this manner, a model is generated or programmed on such system. A programmed system for using a model may be configured to (i) receive input such as an incoming wafer having wafer bow,
15 and (ii) execute instructions that determine a recipe to best mitigate the wafer bow.

[0156] Many types of computing systems having any of various computer architectures may be employed as the disclosed systems for implementing machine learning models and algorithms for generating and/or optimizing such models. For example, the systems may include software components executing on one or more general purpose processors or specially designed processors
20 such as Application Specific Integrated Circuits (ASICs) or programmable logic devices (e.g., Field Programmable Gate Arrays (FPGAs)). Further, the systems may be implemented on a single device or distributed across multiple devices. The functions of the computational elements may be merged into one another or further split into multiple sub-modules.

[0157] In some embodiments, code executed during generation or execution of a machine
25 learning model on an appropriately programmed system can be embodied in the form of software elements which can be stored in a nonvolatile storage medium (such as optical disk, flash storage device, mobile hard disk, etc.), including a number of instructions for making a computer device (such as personal computers, servers, network equipment, etc.).

[0158] At one level a software element is implemented as a set of commands prepared by the
30 programmer/developer. However, the module software that can be executed by the computer hardware is executable code committed to memory using “machine codes” selected from the specific machine language instruction set, or “native instructions,” designed into the hardware processor. The machine language instruction set, or native instruction set, is known to, and

essentially built into, the hardware processor(s). This is the “language” by which the system and application software communicates with the hardware processors. Each native instruction is a discrete code that is recognized by the processing architecture and that can specify particular registers for arithmetic, addressing, or control functions; particular memory locations or offsets; and particular addressing modes used to interpret operands. More complex operations are built up by combining these simple native instructions, which are executed sequentially, or as otherwise directed by control flow instructions.

[0159] The inter-relationship between the executable software instructions and the hardware processor is structural. In other words, the instructions per se are a series of symbols or numeric values. They do not intrinsically convey any information. It is the processor, which by design was preconfigured to interpret the symbols/numeric values, which imparts meaning to the instructions.

[0160] The models used herein may be configured to execute on a single machine at a single location, on multiple machines at a single location, or on multiple machines at multiple locations. When multiple machines are employed, the individual machines may be tailored for their particular tasks. For example, operations requiring large blocks of code and/or significant processing capacity may be implemented on large and/or stationary machines.

[0161] In addition, certain embodiments relate to tangible and/or non-transitory computer readable media or computer program products that include program instructions and/or data (including data structures) for performing various computer-implemented operations. Examples of computer-readable media include, but are not limited to, semiconductor memory devices, phase-change devices, magnetic media such as disk drives, magnetic tape, optical media such as CDs, magneto-optical media, and hardware devices that are specially configured to store and perform program instructions, such as read-only memory devices (ROM) and random access memory (RAM). The computer readable media may be directly controlled by an end user or the media may be indirectly controlled by the end user. Examples of directly controlled media include the media located at a user facility and/or media that are not shared with other entities. Examples of indirectly controlled media include media that is indirectly accessible to the user via an external network and/or via a service providing shared resources such as the “cloud.” Examples of program instructions include both machine code, such as produced by a compiler, and files containing higher level code that may be executed by the computer using an interpreter.

[0162] In various embodiments, the data or information employed in the disclosed methods and apparatus is provided in an electronic format. Such data or information may include design layouts, fixed parameter values, floated parameter values, feature profiles, metrology results, and

the like. As used herein, data or other information provided in electronic format is available for storage on a machine and transmission between machines. Conventionally, data in electronic format is provided digitally and may be stored as bits and/or bytes in various data structures, lists, databases, etc. The data may be embodied electronically, optically, etc.

5 **[0163]** In certain embodiments, a machine learning model can each be viewed as a form of application software that interfaces with a user and with system software. System software typically interfaces with computer hardware and associated memory. In certain embodiments, the system software includes operating system software and/or firmware, as well as any middleware and drivers installed in the system. The system software provides basic non-task-specific
10 functions of the computer. In contrast, the modules and other application software are used to accomplish specific tasks. Each native instruction for a module is stored in a memory device and is represented by a numeric value.

[0164] An example computer system 1300 is depicted in Figure 13. As shown, computer system 1300 includes an input/output subsystem 1302, which may implement an interface for interacting
15 with human users and/or other computer systems depending upon the application. Embodiments of the invention may be implemented in program code on system 1300 with I/O subsystem 1302 used to receive input program statements and/or data from a human user (e.g., via a GUI or keyboard) and to display them back to the user. The I/O subsystem 1302 may include, e.g., a keyboard, mouse, graphical user interface, touchscreen, or other interfaces for input, and, e.g., an
20 LED or other flat screen display, or other interfaces for output. Other elements of embodiments of the disclosure, such as the order placement engine 208, may be implemented with a computer system like that of computer system 1300, perhaps, however, without I/O.

[0165] Program code may be stored in non-transitory media such as persistent storage 1310 or memory 1308 or both. One or more processors 1304 reads program code from one or more non-
25 transitory media and executes the code to enable the computer system to accomplish the methods performed by the embodiments herein, such as those involved with generating or using a process simulation model as described herein. Those skilled in the art will understand that the processor may accept source code, such as statements for executing training and/or modelling operations, and interpret or compile the source code into machine code that is understandable at the hardware
30 gate level of the processor. A bus couples the I/O subsystem 1302, the processor 1304, peripheral devices 1306, memory 1308, and persistent storage 1310.

[0166] In various embodiments, the computer system 1300 may be part of or connected to a controller that is employed to control process conditions during various etch and deposition

operations. The controller will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

CONCLUSION

5 **[0167]** Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Embodiments disclosed herein may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed
10 embodiments. Further, while the disclosed embodiments will be described in conjunction with specific embodiments, it will be understood that the specific embodiments are not intended to limit the disclosed embodiments. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments
15 are not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. A computer program product, comprising a non-transitory computer readable medium
5 having computer-executable instructions for:
 - identifying a wafer shape having a frontside and a backside, wherein the wafer shape has a first bow along a first axis of the wafer shape and a second bow along a second axis of the wafer shape;
 - identifying a plurality of complementary profile film stacks, wherein each
10 complementary profile film stack comprises a first non-uniform thickness profile film and a second non-uniform thickness profile film;
 - determining a compensated first bow and a compensated second bow of the wafer shape corresponding to each stack of complementary profile films when applied to the backside of the wafer shape; and
 - 15 identifying a first complementary profile film stack of the plurality of complementary profile film stacks based on the compensated first bow and the compensated second bow.
2. The computer program product of claim 1, comprising additional computer-executable instructions for identifying a semiconductor fabrication process recipe to deposit the first
20 complementary profile film stack.
3. The computer program product of claim 1, wherein a first subset of the plurality of complementary profile film stacks comprise complementary profile film stacks having multiple pairs of complementary profile films.
25
4. The computer program product of claim 1, wherein each pair of complementary profile films in a complementary profile film stack of the first subset has a different stress ratio than other pairs of complementary profile films in the complementary profile film stack.
- 30 5. The computer program product of claim 1, wherein the first axis and the second axis are perpendicular to each other.
6. The computer program product of claim 1, wherein the wafer shape has a delta bow based on a difference between the first bow and the second bow and a compensated delta bow

based on a difference between the compensated first bow and the compensated second bow, and wherein identifying the first complementary profile film stack is based on the percentile difference between the delta bow and the compensated delta bow.

5 7. The computer program product of claim 1, wherein the first non-uniform thickness profile film has an internal tensile stress and the second non-uniform thickness profile film has an internal compressive stress.

8. The computer program product of claim 7, wherein the plurality of complementary
10 profile film stacks comprise films having different ratios of internal compressive stress to internal tensile stress.

9. The computer program product of claim 8, comprising additional computer-executable instructions for determining a compensation efficiency for each complementary profile film
15 stack, wherein the first complementary profile film stack has a maximum compensation efficiency of the plurality of complementary profile film stacks.

10. The computer program product of claim 1, comprising additional computer-executable instructions for:
20 identifying a plurality of total thicknesses for each complementary profile film stack;
 determining a plurality of compensated first bows and compensated second bows for each complementary profile film stack, the plurality of compensated first bows and compensated second bows corresponding to the plurality of total thicknesses; and
 determining an optimal total thickness for each complementary profile film stack based
25 on the plurality of compensated first bows and compensated second bows.

11. The computer program product of claim 10, comprising additional computer-executable instructions for determining a compensated delta bow for each total thickness of the plurality of total thicknesses for each complementary profile film stack of the plurality of complementary
30 profile film stack, wherein determining the optimal total thickness is based on a percentile difference between the compensated delta bow and a delta bow based on the first bow and the second bow.

12. The computer program product of claim 1, wherein the first non-uniform thickness profile film is a curved-bar profile film and the second non-uniform thickness profile film is a curved-channel profile film.
- 5 13. The computer program product of claim 12, wherein the plurality of complementary profile film stack comprise curved-bar profile films having different profiles based on polynomial functions defining the profile in an x-direction of the wafer shape.
14. The computer program product of claim 1, comprising additional computer-executable
10 instructions for:
 identifying a plurality of cap layers, each cap layer having a uniform thickness profile and either a tensile internal stress or compressive internal stress;
 determining a plurality of secondary compensated first bow and secondary compensated second bow of the wafer shape corresponding to combinations of each complementary profile
15 film stack and each cap layer; and
 identifying a first cap layer and a second complementary profile film stack based on the plurality of secondary compensated first bow and secondary compensated second bow.
15. The computer program product of claim 1, wherein determining the compensated first
20 bow and the compensated second bow comprises simulating the wafer shape and each corresponding complementary profile film stack.
16. The computer program product of claim 15, wherein the simulation models the wafer shape as a shell and each complementary profile film stack as a membrane without bending
25 stiffness.