

METHOD FOR MANUFACTURING A STRUCTURE FOR FORMING A TRIDIMENSIONAL MONOLITHIC INTEGRATED CIRCUIT

Field of the invention

5 The present invention relates to a method for manufacturing a structure for forming a monolithic integrated circuit, as well as a structure and a substrate intended to be used for implementing said method.

Background of the invention

10 Tridimensional (3D) monolithic integrated circuits are particularly promising in view of increasing the density and decreasing the size of electronic components, because they especially avoid misalignment problems of said components.

 The manufacture of such circuits involves transferring a semi-conductor layer onto a substrate already comprising at least one electric component, for example a
15 transistor.

 However, such a transfer is at issue when said component is likely to be damaged when subjected to a temperature higher than 400 °C.

 Indeed, to date there is no method enabling a semi-conductor layer with a good crystal quality to be transferred and involving only steps that can be implemented at a
20 temperature lower than 400 °C.

 Thus, a first option will be to form the semi-conductor layer by directly depositing it onto the substrate comprising at least one electronic component. However, such a deposition made at a temperature lower than 400 °C results in obtaining a polycrystalline or amorphous layer, not having the required crystal quality for the subsequent formation
25 of other electronic components.

 Another option will be to use the Smart Cut™ method which is well known to transfer a semi-conductor layer from a donor substrate to an acceptor substrate. This method involves forming a weakened zone in the donor substrate by implanting atomic species, such as hydrogen and/or helium. However, this implantation generates defects
30 in the transferred layer, which can only be cured to date by an annealing at a temperature higher than 500 °C.

 The so-called BSOI (Bonded Silicon-On-Insulator) and BESOI (Bonded and Etched-Back Silicon-On-Insulator) techniques could be contemplated to transfer a silicon layer from a bulk substrate bonded to a substrate comprising at least one electronic
35 component. However, these techniques enable neither very thin layers to be formed nor a satisfactory bonding energy to be achieved if the temperatures used do not exceed 400 °C.

Brief description of the invention

Embodiments of the invention seek to provide a method for manufacturing a structure comprising a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, which enables a semi-conductor layer having the required properties for the intended application and which provides a good adhesion between the semi-conductor layer and the first substrate to be obtained, without using a temperature higher than 400 °C.

In an aspect of the invention, it is provided a method for manufacturing a structure comprising a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, characterised in that it comprises the following steps of:

(a) providing a first bonding metal layer on the first substrate, called an acceptor substrate,

(b) providing a second substrate, called a donor substrate, comprising successively:

- a semi-conductor base substrate,

- a stack of a plurality of semi-conductor epitaxial layers, a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$ being located at the surface of said stack opposite to the base substrate,

- a second bonding metal layer,

(c) bonding the first substrate and the second substrate through the first and second bonding metal layers, said bonding step being carried out at a temperature lower than or equal to 400 °C,

(d) removing a part of the second substrate so as to transfer the layer of $\text{Si}_x\text{Ge}_{1-x}$ on the first substrate, said removing comprising at least selectively chemically etching a layer of the second substrate relative to the $\text{Si}_x\text{Ge}_{1-x}$ layer.

Thus, the layer of $\text{Si}_x\text{Ge}_{1-x}$ has both an excellent crystal quality and a mobility of charge carriers which is higher than that of a relaxed single crystal silicon layer. Consequently, the structure formed is optimum for manufacturing tridimensional monolithic integrated circuits for high performance and/or low power applications.

On the other hand, metal-metal bonding provides strong bonding energy even at a temperature not exceeding 400 °C, this energy being substantially higher than that provided by a dielectric-dielectric bonding made at such a temperature. Further, the metal-metal interface has the advantage, unlike a dielectric-dielectric interface, not to be attacked by a hydrofluoric acid solution possibly employed for selectively etching at least one layer of the second substrate.

In the present text, a “layer A on the layer B” type or “layer B underlying the layer A” type phrase does not necessarily imply that layers A and B have a common interface; they indeed can be separated by one or more intermediate layers. On the other hand, the “layer A directly on layer B” phrase means that layers A and B are contacting with each other.

According to one embodiment, the second substrate comprises a dielectric layer between the layer of $\text{Si}_x\text{Ge}_{1-x}$ and the second bonding metal layer.

The thickness of said dielectric layer is advantageously between 10 and 20 nm.

According to one embodiment, the base substrate is a silicon substrate.

According to a preferred embodiment, the stack successively comprises, from the base substrate:

- a layer of silicon-germanium having a composition gradually varying over its thickness,

- a layer of silicon-germanium having a constant composition over its thickness,

- a layer of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x , said layer of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer (212) of silicon-germanium having a constant composition over its thickness so as to make up an etching barrier layer towards the layer of $\text{Si}_x\text{Ge}_{1-x}$,

- the layer of $\text{Si}_x\text{Ge}_{1-x}$.

Particularly advantageously:

- the composition of the layer of silicon-germanium having a composition gradually varying over its thickness is $\text{Si}_{0.8}\text{Ge}_{0.2}$ at the surface of said layer opposite to the base substrate,

- the composition of the layer of silicon-germanium having a constant composition over its thickness is $\text{Si}_{0.8}\text{Ge}_{0.2}$, the thickness of said layer being between 0.5 μm and 2 μm ,

- the composition of the etching barrier layer is chosen from Si and $\text{Si}_{0.6}\text{Ge}_{0.4}$, the thickness of said layer being between 10 nm and 50 nm,

- the composition of the layer of $\text{Si}_x\text{Ge}_{1-x}$ is chosen from $\text{Si}_{0.8}\text{Ge}_{0.2}$, Si and Ge, the thickness of said layer being between 5 and 50 nm.

The first and second bonding metal layers can comprise titanium, nickel, copper and/or tungsten.

According to one embodiment, step (b) comprises the following successive steps of:

- epitaxially growing a layer of silicon-germanium with a gradual composition over its thickness,

- epitaxially growing a layer of silicon-germanium with a constant composition over its thickness,

- polishing the layer of silicon-germanium with a constant composition,

- epitaxially growing a layer of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x on the polished layer of silicon-germanium, said layer of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer of silicon-germanium having a constant composition over its thickness,

- epitaxially growing the layer of $\text{Si}_x\text{Ge}_{1-x}$ on the layer of $\text{Si}_y\text{Ge}_{1-y}$,

- depositing the second bonding metal layer.

According to one embodiment, step (b) comprises, between the step of epitaxially growing the layer of $\text{Si}_x\text{Ge}_{1-x}$ and the step of depositing the second bonding metal layer, a step of depositing a dielectric layer.

Step (b) can comprise, after the step of depositing the dielectric layer, a densification annealing of said layer.

Particularly advantageously, step (b) further comprises forming, between the dielectric layer and the second bonding metal layer, a layer of a binary or ternary metal alloy.

According to one embodiment, step (d) comprises withdrawing a part of the thickness of the base substrate by polishing, followed by selectively etching the rest of said base substrate.

Particularly advantageously, etching the base substrate is made with a TMAH, KOH, and/or $\text{HF}:\text{HNO}_3$ solution.

On the other hand, removing the base substrate can be followed by selectively etching the layers of silicon-germanium with a constant composition and a gradual composition by means of a SC1 solution and/or a $\text{HF}:\text{H}_2\text{O}_2:\text{CH}_3\text{COOH}$ solution.

Another aspect relates to a method for manufacturing a tridimensional monolithic integrated circuit, comprising implementing the method described above.

More precisely, this method for manufacturing a tridimensional monolithic integrated circuit, comprises:

- manufacturing a structure comprising a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400°C and a layer of $\text{Si}_x\text{Ge}_{1-x}$ extending on said first substrate by means of the method described above,

- manufacturing at least one other electronic component in or on the layer of $\text{Si}_x\text{Ge}_{1-x}$.

Said method is remarkable in that all the steps implemented on said structure are made at a temperature lower than or equal to 400°C .

Another aspect relates to a structure likely to be obtained by the method described above.

Said structure comprises a first substrate comprising at least one electronic component likely to be damaged by a temperature higher than 400 °C and a semiconductor layer extending on said first substrate, and is characterised in that said semiconductor layer is a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$ and in that said structure comprises, between said first substrate and said semi-conductor layer, a metal layer.

According to one embodiment, said structure further comprises a dielectric layer between the metal layer and the semi-conductor layer.

Advantageously, the structure comprises, between the metal layer and the dielectric layer, a layer of a binary or ternary metal alloy.

Said at least one electronic component can comprise a transistor, a memory, a photodetector, a diode, a laser, a switch, an amplifier and/or a filter.

Another aspect relates to a donor substrate intended to be used in the method described above.

This donor substrate successively comprises:

- a semi-conductor base substrate,
- a stack of a plurality of semi-conductor epitaxial layers, a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$, being located at the surface of said stack opposite to the base substrate,
- a bonding metal layer.

According to one embodiment, the donor substrate further comprises a dielectric layer between the layer of $\text{Si}_x\text{Ge}_{1-x}$ and the metal layer.

Said dielectric layer can have a thickness between 10 and 20 nm.

According to one embodiment, the base substrate is a silicon substrate.

According to one preferred embodiment, the stack successively comprises, from the base substrate:

- a layer of silicon-germanium having a composition gradually varying over its thickness,
- a layer of silicon-germanium having a constant composition over its thickness,
- a layer of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x , said layer of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer of silicon-germanium having a constant composition over its thickness so as to make up an etching barrier layer towards the layer of $\text{Si}_x\text{Ge}_{1-x}$,
- the layer of $\text{Si}_x\text{Ge}_{1-x}$.

Brief description of the drawings

Further characteristics and advantages of the invention will appear from the detailed description that follows, in reference to the appended drawings in which:

- Fig. 1A to 1C are cross-section views of a donor substrate according to various embodiments of the invention,

5 - Fig. 2 is a cross-section view of an acceptor substrate comprising at least one electronic component,

- Fig. 3 and 4 illustrate successive steps of the method for manufacturing the structure according to one embodiment of the invention.

10 It is set out that for the sake of legibility of the figures, the different elements illustrated are not necessarily represented to scale. Identical reference signs from one figure to the other designate identical elements or elements providing the same function.

Detailed description of embodiments of the invention

Fig. 1A to 1C illustrate various alternatives of the donor substrate.

15 Generally, the donor substrate comprises successively:

- a base substrate 20,

20 - a stack 21 of a plurality of semi-conductor epitaxial layers, among which a layer 210 of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$, which is located at the surface of said stack which is opposite to the base substrate 20, said layer being intended to be transferred to another substrate to form the final structure,

- a bonding metal layer 22.

The base substrate 20 is of a semi-conductor material, or a stack of different semi-conductor materials. According to one particular embodiment, the base substrate is of bulk single crystal silicon.

25 In Fig. 1A to 1C, the stack 21 is represented as four layers 213, 212, 211 and 210. However, those skilled in the art could vary the number of layers and their compositions without departing from the scope of the invention, as long as a layer underlying the layer 210 makes up an etching barrier layer. In other words, it is possible to implement selective etching of at least one of the layers of the stack relative to the layer 210.

30 Advantageously, the layers of the stack are silicon, germanium and/or silicon-germanium layers. GaP can possibly be used because this material has a lattice parameter close to that of silicon. Those skilled in the art are able to choose the composition of each layer (which can be, depending on the cases, constant or gradual over the thickness) depending on the desired properties for the layer 210.

35 According to a preferred embodiment, the layer 213 which is formed by epitaxy on the base substrate 20 is a layer of SiGe having a composition gradually varying over

its thickness, such that the final composition of said layer (i.e. at the surface opposite to the base substrate 20) is for example $\text{Si}_{0.8}\text{Ge}_{0.2}$.

5 A layer 212 of silicon-germanium with an identical composition to the final composition of the layer 213 (that is, in this example, $\text{Si}_{0.8}\text{Ge}_{0.2}$) is formed by epitaxy on said layer 213. The composition of the layer 212 is constant over its thickness. The layer 212 is thick, that is having typically a thickness between $0.5\text{ }\mu\text{m}$ and $2\text{ }\mu\text{m}$. Particularly advantageously, a polishing of the surface of the layer 212 is performed before continuing the epitaxy.

10 A layer 211 of a different material from that of the layer 212 (for example of silicon or of $\text{Si}_{0.6}\text{Ge}_{0.4}$ if the layer 212 is of $\text{Si}_{0.8}\text{Ge}_{0.2}$) is formed by epitaxy on the layer 212. The thickness of the layer 211 is in the order of 10 to 50 nm. The layer 211 is an etching barrier layer towards the underlying layers 212, 213. Those skilled in the art are capable of choosing the composition of the layer 211 to provide a sufficient etching selectivity such that etching the base substrate and/or the layers 212, 213 does not attack the
15 overlying layer 210.

The layer 210 is formed by epitaxy on the layer 211. The layer 210 is intended to be transferred onto another substrate to form the final structure, as will be explained below. The layer 210 is of a different material from that making up the etching barrier layer 211. For example, the layer 210 has the composition $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$, the
20 material of said layer being possibly restrained depending on the lattice parameter difference towards the underlying layer 211. For example, the layer 210 can be of $\text{Si}_{0.8}\text{Ge}_{0.2}$, of silicon or of germanium. The thickness of the layer 210 is typically between 5 and 50 nm.

The metal layer 22 can be formed by one of the following materials: nickel,
25 copper, tungsten, titanium. Said layer is generally deposited by one of the following techniques: physical vapour deposition (PVD), electro-deposition, chemical vapour deposition (CVD). The thickness of the metal layer 22 is typically between 10 and 1000 nm.

30 In the embodiment of Fig. 1A, the metal layer 22 is directly deposited onto the layer 210.

In the embodiment of Fig. 1B, a dielectric layer 23 is deposited onto the layer 210 before depositing the metal layer 22. Such a dielectric layer is particularly interesting for a back-gate type application for which a buried oxide is needed. Said dielectric layer advantageously has a very low thickness (typically between 10 and 20 nm). Such a thin
35 layer is thereby not altered by a possible HF etching because the edge attack surface is low for this thickness range. The dielectric layer 23 is generally deposited by one of the following techniques: plasma enhanced chemical vapour deposition (PECVD), atomic

layer deposition (ALD), low pressure chemical vapour deposition (LPCVD), PVD. Depositing said dielectric layer can be followed by a densification annealing.

In the embodiment of Fig. 1C, a layer 24 of a binary or ternary metal alloy is deposited onto the dielectric layer 23 before depositing the metal layer 22. The layer 24
5 has the advantage of promoting adhesion of the metal layer 22 onto the dielectric layer 23.

The donor substrate thus formed can be bonded to another substrate, called an acceptor substrate which comprises at least one electronic component likely to be damaged by a temperature higher than 400 °C.

10 Such an electronic component can for example be a transistor, a memory, a photodetector, a diode, a laser, a switch, an amplifier, a filter or a combination of these components.

Fig. 2 illustrates one embodiment of an acceptor substrate 1.

Said substrate 1 comprises a base substrate 20, for example of bulk silicon,
15 which supports a dielectric layer 13 containing a plurality of transistors 10. Said transistors are of the FinFET (Fin Field Effect Transistor) type, which have a non planar structure.

To bond the acceptor substrate to the donor substrate, a bonding metal layer 11 is advantageously formed on the surface of the acceptor substrate 1 intended to form the
20 bonding interface. Said bonding metal layer 11 can be made of one of the following materials: nickel, titanium, tungsten, copper.

Then, as illustrated in Fig. 3, the donor substrate and acceptor substrate are bonded through bonding layers 22 and 11. In this illustration, the donor substrate is that of Fig. 1A but it could naturally be that of Fig. 1B or that of Fig. 1C.

25 Such metal-metal bonding can be made at a low temperature, that is at a temperature lower than 400 °C, while providing a high bonding energy. Thus, the bonding step does not damage the electronic components 10.

On the other hand, if a back gate function is necessary in the final structure, the metal layer 11, 22 can fulfil this function.

30 In reference to Fig. 4, the layer 210 is transferred from the donor substrate to the acceptor substrate by implementing at least one etching step so as to detach the layer 210 from the underlying layers of the substrate 2. Said etching must be selective towards the layer 210 in order not to damage it.

First of all, a mechanical polishing (also called "grinding") of the base substrate 20
35 can be implemented. This polishing can include a first coarse polishing step followed by a fine polishing step. Most of the base substrate 20 can thereby be withdrawn until a thickness of a few micrometres remains.

Secondly, the rest of the base substrate 20 can be removed by dry polishing or chemical etching. In the case of a silicon substrate, the etching composition is advantageously TMAH, KOH, or HF:HNO₃.

5 Thirdly, the layers 213 and 212 can be withdrawn by dry etching or chemical etching. In the case of layers of silicon-germanium, the etching composition can be a composition SC1 (NH₄OH:H₂O₂:H₂O) or HF:H₂O₂:CH₃COOH.

Possibly, if the etching selectivity permits it, the layer 211 can also be withdrawn by etching. Otherwise, said layer 211 can be withdrawn by dry polishing.

10 Optionally, the different abovementioned etching steps can be implemented by combining different etching compositions. Those skilled in the art are able to define the suitable composition depending on the material to be etched.

From the structure represented in Fig. 4, at least one other electronic component (not illustrated) can be manufactured in or on the layer 210 of Si_xGe_{1-x}.

15 Finally, the examples just described are of course only particular and in no way limiting illustrations as regards the application fields of the invention.

CLAIMS

1. A method for manufacturing a structure comprising a first substrate (1) comprising at least one electronic component (10) likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, characterised in that it comprises the following steps of:

(a) providing a first bonding metal layer (11) on the first substrate (1),

(b) providing a second substrate (2) comprising successively:

- a semi-conductor base substrate (20),

- a stack (21) of a plurality of semi-conductor epitaxial layers, a layer (210) of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$ being located at the surface of said stack (21) opposite to the base substrate (20),

- a second bonding metal layer (22),

(c) bonding the first substrate and the second substrate through the first and second bonding metal layers (11, 22), said bonding step being carried out at a temperature lower than or equal to 400 °C,

(d) removing a part of the second substrate so as to transfer the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$ on the first substrate (1), said removing comprising at least selectively chemically etching a layer of the second substrate (2) relative to the $\text{Si}_x\text{Ge}_{1-x}$ layer (210).

2. The method according to claim 1, wherein the second substrate (2) comprises a dielectric layer (23) between the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$ and the second bonding metal layer (22).

3. The method according to claim 2, wherein the thickness of the dielectric layer (23) is between 10 and 20 nm.

4. The method according to claim 1, wherein the base substrate (20) is a silicon substrate.

5. The method according to one of claims 1 and 2, wherein the stack (21) successively comprises, from the base substrate (20):

- a layer (213) of silicon-germanium having a composition gradually varying over its thickness,

- a layer (212) of silicon-germanium having a constant composition over its thickness,

- a layer (211) of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x , said layer of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer (212) of silicon-germanium having a constant composition over its thickness so as to make up an etching barrier layer towards the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$,

5 - the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$.

6. The method according to claim 5, wherein:

10 - the composition of the layer (213) of silicon-germanium having a composition gradually varying over its thickness is $\text{Si}_{0.8}\text{Ge}_{0.2}$ at the surface of said layer (213) opposite to the base substrate (20),

- the composition of the layer (212) of silicon-germanium having a constant composition over its thickness is $\text{Si}_{0.8}\text{Ge}_{0.2}$, the thickness of said layer (212) being between $0.5 \mu\text{m}$ and $2 \mu\text{m}$,

15 - the composition of the etching barrier layer (211) is chosen from Si and $\text{Si}_{0.6}\text{Ge}_{0.4}$, the thickness of said layer (211) being between 10 nm and 50 nm,

- the composition of the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$ is chosen from $\text{Si}_{0.8}\text{Ge}_{0.2}$, Si and Ge, the thickness of said layer (210) being between 5 and 50 nm.

20 7. The method according to one of claims 1 to 6, wherein the first and second bonding metal layers comprise titanium, nickel, copper and/or tungsten.

8. The method according to one of claims 1 to 7, wherein step (b) comprises the following successive steps of:

25 - epitaxially growing a layer (213) of silicon-germanium with a gradual composition,

- epitaxially growing a layer (212) of silicon-germanium with a constant composition,

- polishing the layer (212) of silicon-germanium with a constant composition,

30 - epitaxially growing a layer (211) of $\text{Si}_y\text{Ge}_{1-y}$, with $0 \leq y \leq 1$ and y different from x on the polished layer (212) of silicon-germanium, said layer (211) of $\text{Si}_y\text{Ge}_{1-y}$ having a different composition from that of the layer (212) of silicon-germanium having a constant composition over its thickness,

- epitaxially growing the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$ on the layer (211) of $\text{Si}_y\text{Ge}_{1-y}$,

- depositing the second bonding metal layer (22).

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9. The method according to claim 8, wherein step (b) comprises, between the step of epitaxially growing the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$ and the step of depositing the second bonding metal layer (22), a step of depositing a dielectric layer (23).

5 10. The method according to claim 9, wherein step (b) comprises, after the step of depositing the dielectric layer (23), a densification annealing of said layer.

10 11. The method according to one of claims 9 and 10, wherein step (b) further comprises forming, between the dielectric layer (23) and the second bonding metal layer (22), a layer (24) of a binary or ternary metal alloy.

15 12. The method according to one of claims 1 to 11, wherein step (d) comprises withdrawing a part of the thickness of the base substrate (20) by polishing, followed by selectively etching the rest of said base substrate (20).

13. The method according to claim 12, wherein etching the base substrate (20) is made with a TMAH, KOH, and/or HF:HNO_3 solution.

20 14. The method according to one of claims 12 and 13, wherein removing the base substrate (20) is followed by selectively etching the layers (213, 212) of silicon-germanium with a constant composition and a gradual composition by means of a SC1 solution and/or a $\text{HF:H}_2\text{O}_2:\text{CH}_3\text{COOH}$ solution.

25 15. A method for manufacturing a tridimensional monolithic integrated circuit, characterised in that it comprises:

- manufacturing a structure comprising a first substrate (1) comprising at least one electronic component (10) likely to be damaged by a temperature higher than 400 °C and a layer (210) of $\text{Si}_x\text{Ge}_{1-x}$ extending on said first substrate by means of a method according to one of claims 1 to 14,

30 - manufacturing at least one other electronic component in or on the layer (210) of $\text{Si}_x\text{Ge}_{1-x}$,

said method being further characterised in that all the steps implemented on said structure are made at a temperature lower than or equal to 400 °C.

35 16. A structure comprising a first substrate (1) comprising at least one electronic component (10) likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer (210) extending on said first substrate, characterised in that said

semi-conductor layer (210) is a layer of $\text{Si}_x\text{Ge}_{1-x}$, with $0 \leq x \leq 1$ and in that said structure comprises successively, from said first substrate (1) to said semi-conductor layer (210):

- a metal layer (11, 22);
- a layer (24) of a binary or ternary metal alloy;
- a dielectric layer (23).

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17. The structure according to claim 16, wherein said at least one electronic component (10) comprises a transistor, a memory, a photodetector, a diode, a laser, a switch, an amplifier and/or a filter.

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