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3 **METHOD TO REMOVE SPACER AFTER SALICIDATION TO ENHANCE**
4 **CONTACT ETCH STOP LINER STRESS ON MOS**
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8 **Background of Invention**

9 **1) Field of the Invention**

10 This invention relates generally to structures and method for
11 fabricating semiconductor devices and more particularly structures and method
12 for inducing stresses of different areas of a substrate.
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14 **2) Description of the Prior Art**
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16 As semiconductor device switching speeds continue to increase
17 and operating voltage levels continue to decrease, the performance of MOS and
18 other types of transistors needs to be correspondingly improved. The carrier
19 mobility in a MOS transistor has a significant impact on power consumption and
20 switching performance, where improvement in carrier mobility allows faster
21 switching speeds. The carrier mobility is a measure of the average speed of a
22 carrier (e.g., holes or electrons) in a given semiconductor, given by the average
23 drift velocity of the carrier per unit electric field. Improving carrier mobility can
24 improve the switching speed of a MOS transistor, as well as allow operation at
25 lower voltages.
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27 One way of improving carrier mobility involves reducing the
28 channel length and gate dielectric thickness in order to improve current drive and

1 switching performance. However, this approach may increase gate tunneling
2 current, which in turn degrades the performance of the device by increasing off
3 state leakage. In addition, decreasing gate length generally calls for more
4 complicated and costly lithography processing methods and systems.

5 The importance of overcoming the various deficiencies is
6 evidenced by the extensive technological development directed to the subject, as
7 documented by the relevant patent and technical literature. The closest and
8 apparently more relevant technical developments in the patent literature can be
9 gleaned by considering the following.

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11 US 20040262784 High performance cmos device structures and
12 method of manufacture - A semiconductor device structure includes at least two
13 field effect transistors formed on same substrate, the first field effect transistor
14 includes a spacer having a first width, the second field effect transistor includes a
15 compressive spacer having a second width, the first width being different than said
16 second width. Preferably, the first width is narrower than the second width. A
17 tensile stress dielectric film forms a barrier etch stop layer over the transistors.
18 Inventors: Bruce B. Doris, et al.

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20 US 6825529: and US 20040113217A1: Stress inducing spacers
21 - Spacer structure for semiconductor devices formed in substrate, has two spacer
22 structures, each comprising stress inducing material adjacent to both sidewall of
23 one of device's gate terminal and its channel which applies mechanical stress -
24 Inventor: Chidambarao

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26 US20040104405A1: Novel CMOS device - Improving mobility
27 of holes and electrons within semiconductor device structure, involves forming first

1 and second stress layers over p- and n-type metal oxide semiconductor device
2 respectively - Inventor: Huang

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4 US 6573172: Methods for improving carrier mobility of PMOS and
5 NMOS devices - Fabrication of semiconductor device by forming P-channel and
6 N-channel metal oxide semiconductor transistors in wafer, forming tensile film on
7 P-channel transistor and forming compressive film on N-channel transistor -
8 Inventor: En, et al.

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10 US20030040158A1: Semiconductor device and method of
11 fabricating the same - Semiconductor device includes first nitride layer containing
12 tensile stress and second nitride layer containing compressive stress - Inventor:
13 Saitoh, Takehiro

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16 Thus, there remains a need for methods by which the carrier
17 mobility of both NMOS and PMOS transistors may be improved so as to facilitate
18 improved switching speed and low-power, low-voltage operation of CMOS
19 devices, without significantly adding to the cost or complexity of the manufacturing
20 process.

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Summary of the Invention

The embodiments of the present invention provides a structure and a method of manufacturing a FET device without spacer and with an overlying stress layer improves device performance which is characterized as follows.

An example embodiment of the invention is a method of fabrication semiconductor device; comprising the steps of:

- providing a substrate having a first region and a second region;
- providing a first gate, first source/drain regions in said first region; a first channel region in said first region under said first gate;
- providing a second gate, second spacers on the second gate sidewalls; second source/drain regions in said second region adjacent to said second spacers;
- forming a stress dielectric layer over: the first gate, the first source/drain regions, the second gate, the second spacers and the second source/drain regions; whereby said stress dielectric layer serves to puts stress on the first channel region on the substrate close to the first gate.

Another example embodiment of the invention is a method of fabrication semiconductor device; comprising the steps of:

- providing a substrate having a first region and a second region;
- providing a first gate, first spacers on the first gate sidewalls; first source/drain regions in the first region adjacent to the first spacers; providing first S/D silicide regions over the first source/drain regions;

1 providing a second gate, second spacers on the second gate sidewalls;
2 second source/drain regions in the second region adjacent
3 to the second spacers; providing second S/D silicide
4 regions over the second source/drain regions;
5 forming a conformal dielectric layer over the substrate at least the first
6 region and the second region;
7 forming a non-conformal dielectric layer over the conformal dielectric layer;
8 the non-conformal dielectric layer is thicker over the
9 second cap and first cap and the substrate than over the
10 second and first spacer sidewalls;
11 removing a first thickness of the non-conformal dielectric layer in the first
12 region; using an etch, to expose the conformal dielectric
13 layer over the first spacers;
14 removing the first spacers using an etch;
15 removing the non-conformal dielectric layer;
16 forming a stress dielectric layer which serves to put stress on the stress
17 on the substrate close to the first gate where the first
18 spacers were removed in the first region thereby enhance
19 the first device performance.

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22 An aspect of this embodiment is wherein the first region is a
23 NFET region and the second region is a PFET region; and the stress dielectric
24 layer produces a compressive stress on the NFET channel in a uni-axial
25 direction; and the channel has a 110 crystal orientation.

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1 An example embodiment of the invention is a semiconductor
2 device comprises:
3 a substrate having a first region and a second region;
4 a first gate, first source/drain regions in the first region adjacent to the first
5 spacers; providing first S/D silicide regions over the first
6 source/drain regions;
7 a second gate over the second region, second spacers on the second
8 gate sidewalls; second source/drain regions in the
9 second region adjacent to the second spacers; second
10 S/D silicide regions over the second source/drain regions;
11 a conformal dielectric layer over the second gate and the second spacers,
12 the second S/D silicide regions, and the first S/D silicide
13 regions;
14 a stress dielectric layer over the sidewalls of the first gate and over the
15 substrate adjacent to the first gate; the stress dielectric
16 layer which serves to puts stress on the stress on the
17 substrate close to the first gate which does not have first
18 spacers thereby enhance the first device performance;
19 the stress dielectric layer over the sidewalls of the second spacers and
20 the second gate.

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22 An aspect of this embodiment is wherein the first region is a
23 NFET region and the second region is a PFET region; the stress dielectric layer is
24 a tensile stress layer; and the stress dielectric layer produces a compressive
25 stress on the NFET channel in a uni-axial direction; and the NFET channel has a
26 110 crystal orientation.

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1 The above and below advantages and features are of
2 representative embodiments only, and are not exhaustive and/or exclusive. They
3 are presented only to assist in understanding the invention. It should be
4 understood that they are not representative of all the inventions defined by the
5 claims, to be considered limitations on the invention as defined by the claims, or
6 limitations on equivalents to the claims. For instance, some of these advantages
7 may be mutually contradictory, in that they cannot be simultaneously present in a
8 single embodiment. Similarly, some advantages are applicable to one aspect of
9 the invention, and inapplicable to others. Furthermore, certain aspects of the
10 claimed invention have not been discussed herein. However, no inference should
11 be drawn regarding those discussed herein relative to those not discussed herein
12 other than for purposes of space and reducing repetition. Thus, this summary of
13 features and advantages should not be considered dispositive in determining
14 equivalence. Additional features and advantages of the invention will become
15 apparent in the following description, from the drawings, and from the claims.
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Brief Description of the Drawings

The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figures 1 through 6 are cross sectional views for illustrating a method for manufacturing a transistor according to a first example embodiment of the present invention.

Figure 7 is cross sectional view for illustrating a method for manufacturing a transistor according to a second example embodiment of the present invention.

Detailed Description of the Example Embodiments

First example embodiment

The example embodiments of the present invention will be described in detail with reference to the accompanying drawings. The example embodiments provide methods of applying a stress on a channel of an MOS transistor using a stress layer in silicide process. Preferably, the source drain regions have a silicide contact layer thereover. An embodiment removes spaces from a gate and forms a stress layer on or adjacent to the gate. The spacers can be removed from either the PMOS or the NMOS transistor.

A. Substrate has a NFET region and a PFET region

As shown in figure 1, we provide a substrate having a NFET region 12, a PFET region 14 and an optional peripheral region 16. The substrate can have isolation region(s) 24 at least between the NFET region 12, the PFET region 14 and the peripheral region 16.

In the NFET region, we provide a NFET transistor that can be comprised of NFET gate dielectric 29, a NFET gate 30, NFET cap 32, a NFET spacers on the NFET gate 30 sidewalls; NFET source/drain regions 25 in the NFET region adjacent to the NFET spacers 26. We provide NFET S/D silicide regions 26 over the NFET source/drain regions 25 and the NFET cap 32 preferably comprised of silicide. The NFET transistor has a NFET channel under the NFET gate. A NFET channel is in the NFET region under the NFET gate.

In the PFET region 14, we provide a PFET transistor that can be comprised of a PFET gate dielectric layer 27, a PFET gate 38, PFET cap 40,

1 PFET spacers 36 on the PFET gate 38 sidewalls. We provide PFET source/drain
2 regions 33 in the PFET region 14 adjacent to the PFET spacers 36. PFET S/D
3 silicide regions 34 are formed over the PFET source/drain regions 33. The PFET
4 cap 40 is preferably comprised of a silicide. A PFET channel is in the PFET region
5 under the PFET gate.

6 In the peripheral region, we provide peripheral gate structure 49
7 over the peripheral region 16. The peripheral gate structures are comprised of a
8 peripheral gate 40, peripheral spacer 44 and peripheral cap 48.

9 The substrate has an (peripheral) isolation region 24 over at least
10 a portion of the peripheral region 16; and the peripheral gate structure 49 can be
11 over the isolation region.

12 The structures can be made using a salicide process.

13 **B. conformal dielectric layer**

14 Referring to figure 2, we form a conformal dielectric layer 52
15 (about or substantially uniform thickness) over the substrate at least the NFET
16 region 12, the PFET region 14 and the peripheral region 16. The conformal
17 dielectric layer preferably has about uniform thickness.

18 The conformal dielectric layer 52 can be comprised of oxide or
19 silicon oxynitride (SiON) and can have a thickness between 50 and 100
20 angstroms.

21 **C. non-conformal dielectric layer**

22 We then form a non-conformal dielectric layer 54 over the
23 conformal dielectric layer 52. The non-conformal dielectric layer can be comprised
24 of nitride or SiC. A nitride non-conformal dielectric layer can be formed using a
25 PECVD process.

26 The non-conformal dielectric layer 54 is thicker over about
27 horizontal surfaces than over sloped or vertical surfaces. The non-conformal

1 dielectric layer 54 can be between 150% and 400 % thicker over about horizontal
2 surfaces than over sloped or vertical surfaces. The tops of the gates and the
3 substrate are about horizontal. The spacer sidewalls are sloped.

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5 The non-conformal layer 54 is thicker over the PFET cap 40 and
6 NFET cap 32 and the substrate than over the PFET and NFET spacer 36 28
7 sidewalls.

8 For example, the non-conformal layer 54 can have a thickness
9 between 300 and 400 angstroms over the PFET cap 40 and NFET cap 32 and the
10 substrate; and a thickness between 100 and 200 angstroms over the PFET and
11 NFET spacer 36 28 sidewalls.

12 **D. remove a first thickness of the non-conformal nitride layer in**
13 **the NFET region**

14 As shown in figure 3, we remove a first thickness (portion) of the
15 non-conformal nitride layer 54 in the NFET region 12 to expose at least a portion
16 of the conformal dielectric layer 52 over the NMOS spacers 28.

17 A photoresist layer 56 can be formed over the non-NMOS regions
18 (e.g. PMOS region 14 and peripheral region 16).

19 The etch can be an isotropic etch can be a such as a wet etch or
20 Chemical Down Stream Etch (CDE).

21 The first thickness is between about 33 and 66 % of the
22 maximum thickness of the non-conformal nitride layer 54.

23 Due to the poor step coverage of the non-conformal layer over
24 the spacers, the non-conformal layer is etched away before the non-conformal
25 layer over the horizontal surfaces (e.g., cap, silicide regions 26, isolation regions
26 24, etc.).

27

28 Next, we remove the NMOS spacers 28.

1 An example option is shown in figures 4 and 5.

2 **E. remove the conformal dielectric layer over the NMOS**
3 **spacers**

4 Figure 4 shows the PFET mask 56 over the NFET region 14 and
5 the peripheral region 16, We remove the exposed conformal dielectric layer 52
6 over the NMOS spacers 28 to expose the NMOS spacers 28. The conformal
7 dielectric layer 52 can be removed using an isotopic etch.

8 **F. remove the NMOS spacers**

9 As shown in figure 5, we etch the NMOS spacers 28. The etch
10 can be an isotropic etch that is selective to the spacer material. The etch
11 preferably exposed the substrate surface immediately adjacent to the gate 30.

12 Then we remove the mask 56.

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14 **G. remove the non-conformal nitride layer**

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16 As shown in figure 5, we remove the non-conformal layer 54. The
17 non-conformal nitride layer 54 can be removed using a etch selective to oxide.

18 The silicide regions 26 34 are protected by the conformal
19 dielectric layer 52 during this nitride etch.

20 **H. form a tensile dielectric layer**

21 As shown in figure 6, we form a tensile dielectric layer 60 (e.g.,
22 tensile stress nitride) which serves to put a compressive stress on the substrate
23 close to the gate (where the spacers 28 used to be) in the NMOS region 12, which
24 in turn cause a tensile strain in the NMOS channel region (Si below Poly 30),
25 thereby enhance the NMOS transistor performance. The tensile dielectric layer
26 can serve as a contact etch stop liner (ESL).

1 The PMOS transistor device is affected less than the NMOS
2 device because the PMOS spacers 36 separate and space the tensile nitride layer
3 60 from the substrate under the PMOS spacers 36 and the PMOS channel region.
4 The tensile dielectric (e.g., nitride) layer causes a tensile stress
5 in a channel region of the NMOS transistor.
6 The stress is preferably in an Uni-axial direction only. A preferred
7 channel has a 110 crystal orientation. Uni-axial strain means the strain is in X
8 and Y directions, not in the Z direction.
9 A feature of the embodiment is that because the spacers are
10 removed, the stressor is nearer to the channel thus enhancing the strain effect.
11 The device can be finished using conventional process such as
12 forming a ILD layer, contacts, and subsequent levels of IMD and interconnects.

13 **Alternate embodiment**

14 Figure 7 shows an alternate embodiment where the spacers on
15 the PMOS gate device 38 40 are removed. The process for this embodiment can
16 be similar to the first embodiment by masking the non-PMOS regions and
17 removing the PMOS spacers 36. Stress layer 61 is formed over the substrate
18 surface. For this PMOS embodiment, the stress layer 61 is a compressive film.
19 The stress layer 61 preferably puts a tensile stress on the
20 substrate near the PMOS gate, which in turn causes a compressive strain on the
21 PMOS channel (Si below Poly 38). This enhances the PMOS transistor.

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24 **A. non-limiting example embodiments**

25 In the above description numerous specific details are set forth
26 such as flow rates, pressure settings, thicknesses, etc., in order to provide a more
27 thorough understanding of the present invention. Those skilled in the art will

1 realize that power settings, residence times, gas flow rates are equipment specific
2 and will vary from one brand of equipment to another. It will be obvious,
3 however, to one skilled in the art that the present invention may be practiced
4 without these details. In other instances, well known process have not been
5 described in detail in order to not unnecessarily obscure the present invention.

6 Although this invention has been described relative to specific
7 insulating materials, conductive materials and apparatuses for depositing and
8 etching these materials, it is not limited to the specific materials or apparatuses but
9 only to their specific characteristics, such as conformal and nonconformal, and
10 capabilities, such as depositing and etching, and other materials and apparatus
11 can be substituted as is well understood by those skilled in the microelectronics
12 arts after appreciating the present invention

13 Unless explicitly stated otherwise, each numerical value and
14 range should be interpreted as being approximate as if the word about or
15 approximately preceded the value of the value or range.

16 Given the variety of embodiments of the present invention just
17 described, the above description and illustrations show not be taken as limiting the
18 scope of the present invention defined by the claims.

19 While the invention has been particularly shown and described
20 with reference to the preferred embodiments thereof, it will be understood by those
21 skilled in the art that various changes in form and details may be made without
22 departing from the spirit and scope of the invention. It is intended to cover various
23 modifications and similar arrangements and procedures, and the scope of the
24 appended claims therefore should be accorded the broadest interpretation so as to
25 encompass all such modifications and similar arrangements and procedures.

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What is claimed is:

1. A method of fabrication of a semiconductor device comprising:
 - providing a substrate having a first region and a second region;
 - providing a first transistor in said first region having a first gate with exposed first gate sidewalls, first source/drain regions adjacent to said first gate, and a first channel region under said first gate;
 - providing a second transistor in said second region having a second gate, second spacers over second gate sidewalls of said second gate, second source/drain regions adjacent to said second spacers, and a second channel region under said second gate;
 - and
 - forming a stress dielectric layer having a first stress over the first and second transistors, the stress dielectric layer contacting the exposed first gate sidewalls, the stress dielectric layer remains over the first and second transistors, wherein the second transistor is less affected by the stress dielectric layer than the first transistor.
2. A method of fabrication of a semiconductor device comprising the steps of:
 - a) providing a substrate having a first region and a second region;
 - b) providing a first gate dielectric layer, a first gate, first spacers on first gate sidewalls, and first source/drain regions in said first region adjacent to said first spacers; said first spacers having first spacer sidewalls;
 - c) providing a second gate dielectric layer, a second gate, second spacers on second gate sidewalls; and second source/drain regions in said second region adjacent to said second spacers; said second spacers having second spacer sidewalls;
 - d) forming a dielectric layer over the substrate over at least the first region and the second region;
 - e) forming a non-conformal dielectric layer over said substrate;
 - (1) the non-conformal dielectric layer is thicker over a top of the first gate, the second gate and the substrate, than over the first spacer sidewalls and the second spacer sidewalls;

- f) removing a first thickness of the non-conformal dielectric layer over the first region, using a first etch, to expose at least a portion of the dielectric layer over the first spacers;
- g) removing the exposed portion of the dielectric layer and said first spacers using an etch process;
- h) removing the non-conformal dielectric layer; and
- i) forming a stress dielectric layer over said substrate.

3. The method of claim 2 wherein said first region is a NFET region and said second region is a PFET region; and said stress dielectric layer produces a tensile stress on a NFET channel in a uni-axial direction; and the NFET channel has a 110 crystal orientation.

4. The method of claim 2 wherein said first region is a PFET region and said second region is a NFET region; and said stress dielectric layer produces a compressive stress on a PFET channel in a uni-axial direction; and the PFET channel has a 110 crystal orientation.

5. The method of claim 2 wherein forming the stress dielectric layer causes a tensile stress in a channel region of a NMOS transistor.

6. The method of claim 2 wherein said dielectric layer is comprised of oxide or silicon oxynitride; and said dielectric layer is a conformal dielectric layer.

7. The method of claim 2 wherein said non-conformal dielectric layer is thicker over about horizontal surfaces than over sloped or vertical surfaces; said non-conformal dielectric layer is thicker over the first spacer sidewalls than over a top of said first gate and over said first source/drain regions.

8. The method of claim 2 wherein said the non-conformal dielectric layer is between about 150% and 400% thicker over about horizontal surfaces than over sloped or vertical surfaces.

9. The method of claim 2 wherein the first thickness is between about 33 and 66% of a maximum thickness of said non-conformal dielectric layer.

10. A method of fabrication semiconductor device comprising the steps of:

- a) providing a substrate having a NFET region and a PFET region;
- b) providing a NFET gate dielectric, a NFET gate, NFET spacers on NFET gate sidewalls, NFET source/drain regions in said NFET region adjacent to said NFET spacers; and providing NFET S/D silicide regions over said NFET source/drain regions;
- c) providing a PFET gate dielectric, a PFET gate, PFET spacers on PFET gate sidewalls; PFET source/drain regions in said PFET region adjacent to said PFET spacers; and providing PFET S/D silicide regions over said PFET source/drain regions;
- d) forming a conformal dielectric layer over the substrate over at least the NFET region and the PFET region;
- e) forming a non-conformal dielectric layer over said conformal dielectric layer;
- f) removing a first thickness of the non-conformal dielectric layer over the NFET region, using a first etch, to expose the conformal dielectric layer over the NFET spacers;
 - (1) the first thickness is between about 33 and 66% of a maximum thickness of said non-conformal dielectric layer;
- g) removing the exposed conformal dielectric layer over the NFET spacers and the NFET spacers using an etch process;
- h) removing the non-conformal dielectric layer; and
- i) forming a tensile stress dielectric layer over said substrate.

11. The method of claim 10 wherein forming the tensile stress dielectric layer causes a tensile stress in a channel region of the NMOS transistor.

12. The method of claim 10 wherein the tensile stress dielectric layer produces a tensile stress on a NFET channel in a uni-axial direction; and the NFET channel has a 110 crystal orientation.

13. The method of claim 10 wherein the non-conformal dielectric layer is thicker over the PFET gate and NFET gate and the substrate than over PFET and NFET spacer sidewalls.

14. The method of claim 10 wherein the non-conformal dielectric layer is thicker over about horizontal surfaces than over sloped or vertical surfaces.
15. The method of claim 10 wherein the non-conformal dielectric layer is between about 150% and 400% thicker over about horizontal surfaces than over sloped or vertical surfaces.
16. The method of claim 10 wherein said conformal dielectric layer is comprised of oxide or silicon oxynitride; and said conformal dielectric layer has a thickness between 50 and 100 angstroms.
17. The method of claim 2 which further comprises:
providing silicide regions over said first source/drain regions and said second source/drain regions.
18. The method of claim 1 wherein:
the first transistor comprises a N-type transistor, the second transistor comprises a P-type transistor, and the first stress comprises a tensile stress; or
the first transistor comprises a P-type transistor, the second transistor comprises a N-type transistor, and the first stress comprises a compressive stress.
19. The method of claim 1 comprises:
forming a dielectric layer over the first and second transistors prior to forming the stress dielectric layer; and
removing the dielectric layer over the first transistor to expose the first gate sidewalls.
20. The method of claim 1 wherein the first transistor comprises first spacers on the first gate sidewalls, wherein the first spacers are removed to expose the first gate sidewalls.
21. The method of claim 20 wherein:

the first transistor comprises a N-type transistor, the second transistor comprises a P-type transistor, and the first stress comprises a tensile stress; or

the first transistor comprises a P-type transistor, the second transistor comprises a N-type transistor, and the first stress comprises a compressive stress.

22. The method of claim 20 comprises:

forming a dielectric layer over the first and second transistors prior to forming the stress dielectric layer; and

removing portions of the dielectric layer covering the first spacers on the first gate sidewalls to expose the first spacers.

23. The method of claim 22 wherein:

the first transistor comprises a N-type transistor, the second transistor comprises a P-type transistor, and the first stress comprises a tensile stress; or

the first transistor comprises a P-type transistor, the second transistor comprises a N-type transistor, and the first stress comprises a compressive stress.

24. The method of claim 20 comprises:

forming a dielectric layer over the first and second transistors prior to forming the stress dielectric layer;

forming a non-conformal layer over the dielectric layer; and

removing portions of the dielectric and non-conformal layer covering the first spacers on the first gate sidewalls to expose the first spacers.

25. The method of claim 24 wherein:

the first transistor comprises a N-type transistor, the second transistor comprises a P-type transistor, and the first stress comprises a tensile stress; or

the first transistor comprises a P-type transistor, the second transistor comprises a N-type transistor, and the first stress comprises a compressive stress.

26. A method of fabrication of a semiconductor device comprising:

providing a substrate having a first region and a second region;

providing a first transistor in the first region having a first gate, exposed first spacers over first gate sidewalls of the first gate, first source/drain regions adjacent to the first gate, and a first channel region under the first gate;

providing a second transistor in the second region having a second gate, second spacers over second gate sidewalls of the second gate, second source/drain regions adjacent to the second spacers, and a second channel region under the second gate;

forming a dielectric layer in the first and second regions;

forming a non-conformal dielectric layer over the dielectric layer;

removing portions of the dielectric and non-conformal dielectric layers over the first transistor to expose the first spacers;

removing the first spacers to expose the first gate sidewalls; and

forming a stress dielectric layer having a first stress over the first and second transistors, the stress dielectric layer remains over the first and second transistors and contacts the exposed first gate sidewalls, wherein the second transistor is less affected by the stress dielectric layer than the first transistor.

27. The method of claim 26 wherein:

the first transistor comprises a N-type transistor, the second transistor comprises a P-type transistor and the first stress comprises a tensile stress; or

the first transistor comprises a P-type transistor, the second transistor comprises a N-type transistor and the first stress comprises a compressive stress.

28. The method of claim 18 wherein the first stress is in a uni-axial direction, and the first channel has a 110 crystal orientation.

29. The method of claim 21 wherein the first stress is in a uni-axial direction, and the first channel has a 110 crystal orientation.

30. The method of claim 23 wherein the first stress is in a uni-axial direction, and the first channel has a 110 crystal orientation.

31. The method of claim 25 wherein the first stress is in a uni-axial direction, and the first channel has a 110 crystal orientation.