DESCRIPTION

SILICON CARBIDE-BASED COMPOSITE STRUCTURE HAVING GOOD VERTICAL ELECTRICAL CONDUCTION

FIELD OF THE INVENTION

[0001] The present invention relates to the field of microelectronics and semiconductors. In particular, the invention relates to a composite structure comprising a single-crystal silicon carbide working layer, a polycrystalline silicon carbide carrier substrate, and an intermediate region, between the working layer and the carrier substrate, favoring vertical electrical conduction.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

[0002] Silicon carbide (SiC) is increasingly used in the manufacture of high-performance power devices. High-quality single-crystal SiC substrates (c-SiC), intended for the microelectronics industry, remain expensive and difficult to supply in large size. It is therefore advantageous to resort to solutions for transferring layers, to produce composite structures typically comprising a thin film made of c-SiC (from a high-quality c-SiC substrate and intended to accommodate the sensitive functional parts of devices) on a lower-cost carrier substrate, for example made of polycrystalline SiC (p-SiC). It should also be noted that a composite structure can provide additional functionalities and performance, in particular by providing a carrier substrate with advantageous mechanical, electrical and/or thermal properties.

[0003] A well-known thin-film transfer solution is the Smart Cut® method, based on light-ion implantation in a donor substrate (c-SiC) and direct bonding at a bonding interface between the donor substrate and a carrier substrate (e.g. p-SiC).

[0004] In the field of power electronics, vertical components require good electrical conduction between the thin film (also known as the working layer) and the substrate supporting the composite structure. In particular, the bonding interface between a working layer and a carrier substrate must have a resistivity as low as possible, preferably less than 1 mohm.cm^2, or even less than 0.1 mohm.cm^2.

[0005] Document WO2022/008809 proposes to form an interface zone from a very thin layer of a metal material, such as tungsten, in a SiC/SiC semiconductor structure. Considering a working layer and a carrier substrate made of single-crystal SiC with a resistivity of 20 mohm.cm, and a tungsten

[0006] (W) layer of 1 nm to 3 nm sandwiched between the working layer and the carrier substrate, it is possible to achieve an interface zone resistivity of less than or equal to 0.1 mohm.cm^2, after application of an appropriate heat treatment and formation of very fine nodules largely consisting of metal (W), responsible for good vertical conduction of the

[0007] interface zone.

[0008] Document WO2022/129726 proposes to form an interface zone, in a SiC/SiC semiconductor structure, comprising regions of direct contact between the working layer and the carrier substrate, and agglomerates comprising a semiconductor material different from that or those of the working layer and the carrier substrate, and having a thickness less than or equal to 250 nm. The semiconductor material is chosen for its particular affinity with oxygen. Thus, the agglomerates are able to effectively trap the oxygen that may be present in the bonding interface; the regions of direct contact between the working layer and the carrier substrate, devoid of native oxide residues in particular, allow electrical conduction and/or a vertical semiconductor/semiconductor contact that is effective and of good quality. Considering a working layer and a carrier substrate made of c-SiC with a resistivity of 20 mohm.cm, and a silicon

semiconductor material, it is possible to achieve an interface zone resistivity of less than or equal to 0.1 mohm.cm^2, for example 0.032 mohm.cm^2 (after annealing the structure at 1370°C) or 0.0076 mohm.cm^2 (after annealing at a very high temperature, namely 1900°C).

OBJECT OF THE INVENTION

[0009] The present invention offers a particularly favorable alternative solution for achieving very low interface resistivities in composite structures with a c-SiC working layer and a p-SiC carrier substrate, and whose doping levels are not necessarily extremely high. The invention relates to a composite structure comprising an intermediate region including an interface zone between a bonded face of the working layer and a bonded face of the carrier substrate, and comprising single-crystal silicon carbide inclusions in direct contact with the working layer and extending between grains of the carrier substrate. These inclusions are particularly conducive to vertical electrical conduction. The invention also relates to a method for manufacturing said composite structure.

BRIEF DESCRIPTION OF THE INVENTION

[0010] The present invention relates to a composite structure having a front face and a rear face extending parallel to a main plane, and comprising:

[0011] - a working layer made of single-crystal silicon carbide, one free face of which forms the front face, with a first concentration of N-type dopants,

[0012] - a carrier substrate made of polycrystalline silicon carbide, one free face of which forms the rear face, with a second concentration of N-type dopants, the second concentration being higher than the first concentration,

[0013] - an intermediate region extending along the main plane and including an interface zone between a bonded face of the working layer and a bonded face of the carrier substrate.

[0014] The composite structure is remarkable in that the intermediate region comprises single-crystal silicon carbide inclusions in direct contact with the working layer and extending, in a direction normal to the main plane, between grains of the carrier substrate, said inclusions having a third N-type dopant concentration between the first and second concentrations.

[0015] According to advantageous features of the invention, taken alone or in any feasible combination:

• the carrier substrate, at least on the side of its bonded face, comprises silicon carbide grains having a size less than or equal to 500 nm, said grains covering, in the main plane, a surface area greater than or equal to 20% of the bonded face;

• the silicon carbide grains having a size less than 500 nm cover, in the main plane (x,y), a surface area greater than or equal to 50% or even 80% of the bonded face of the carrier substrate;

• at least 20% of the silicon carbide grains, on the side of the bonded face of the carrier substrate, have a misorientation, between themselves or with respect to the orientation [111], greater than or equal to 30°;

• the intermediate region comprises silicon nodules arranged in the interface zone or under the inclusions between grains of the carrier substrate;

• the first concentration is between $1x10^{18}/cm^3$ and $5x10^{18}/cm^3$;

• the second concentration is between $1x10^{20}/cm^3$ and $5x10^{20}/cm^3$, preferably between $1x10^{20}/cm^3$ and $2x10^{20}/cm^3$;

• the inclusions have a thickness, along an axis normal to the main plane, of between 20 nm and 70 nm, and a width, in the main plane, of between 100 nm and 700 nm;

• the intermediate region has a density of inclusions, in the main plane, of between $0.1/\mu m^2$ and $1/\mu m^2$.

[0016] The invention also relates to a method for manufacturing a composite structure as above, comprising the following steps:

[0017] a) providing a single-crystal silicon carbide donor substrate with a first concentration of N-type dopants, and comprising a buried brittle plane induced by ion implantation of light species;

[0018] b) providing a polycrystalline carrier substrate;

[0019] c) depositing a silicon film on a face to be bonded of the donor substrate and/or on the face to be bonded of the carrier substrate;

[0020] d) bonding the donor substrate and the carrier substrate at their faces to be bonded, so as to obtain a bonded assembly comprising a silicon interlayer, derived from the film(s) deposited in step c), between the donor substrate and the carrier substrate, said interlayer having a thickness of between 8 nm and 30 nm;

[0021] e) separating along the buried brittle plane to form a transferred structure comprising the working layer, transferred from the donor substrate, disposed on the interlayer, itself disposed on the carrier substrate;

[0022] f) applying a heat treatment to the transferred structure, at a plateau temperature of between 1500°C and 2000°C, to form the composite structure.

[0023] According to advantageous features of the invention, taken alone or in any feasible combination:

• the carrier substrate comprises, at least on the side of a face to be bonded, silicon carbide grains having a size less than or equal to 500 nm, said grains covering, in the main plane, a surface area greater than or equal to 20% of the face to be bonded;

• at least 20% of the silicon carbide grains, on the side of the bonded face of the carrier substrate, have a misorientation, between themselves or with respect to the orientation [111], greater than or equal to 30°;

• the plateau temperature is maintained for a duration of between 30 minutes and 4 hours;

• the treatment in step f) has a temperature ramp-up of less than or equal to 20°C/min, or even less than or equal to 10°C/min;

• the second concentration is of the order of $1\times10^{20}/cm^3$, the first concentration is of the order of $3\times10^{18}/cm^3$, and the silicon carbide grains having a size less

than or equal to 500 nm cover, in the main plane, a surface area greater than or equal to 50% or even 60% of the face to be bonded of the carrier substrate;

• the second concentration is of the order of $1\times10^{20}/cm^3$, the first concentration is of the order of $1\times10^{18}/cm^3$, and the silicon carbide grains having a size less than or equal to 500 nm cover, in the main plane, a surface area greater than or equal to 80% of the face to be bonded of the carrier substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Other features and advantages of the invention will emerge from the following detailed description with reference to the appended figures, in which:

[0025] [Fig. 1] [Fig. 1] shows a composite structure according to the invention;

[0026] [Fig. 2] [Fig. 2] shows the intermediate region of a composite structure according to the invention, schematically on the left in the figure, with a transmission electron microscopy image on the right;

[0027] [Fig. 3a]

[0028] [Fig. 3b]

[0029] [Fig. 3c]

[0030] [Fig. 3d]

[0031] [Fig. 3e]

[0032] [Fig. 3f] Figures 3a to 3f show steps of a method for manufacturing a composite structure, according to the present invention;

[0033] [Fig. 4] [Fig. 4] shows the intermediate region of a composite structure according to the invention, schematically on the left in the figure, with a transmission electron microscopy image on the right;

[0034] [Fig. 5] [Fig. 5] shows the intermediate region of a composite structure according to the invention, with a transmission electron microscopy image;

[0035] [Fig. 6] [Fig. 6] shows theoretical curves (numerical simulations) relating the resistivity of the intermediate region of a composite structure to the percentage of the carrier substrate surface area in which the p-SiC grains have a size less than or equal to 500 nm, for different doping concentrations of the working layer ($N_{monoSiC}$) and the carrier substrate ($N_{polySiC}$).

[0036] Some figures are schematic depictions which, for the sake of readability, are not to scale. In particular, the thicknesses of the layers along the z-axis are not to scale with respect to the lateral dimensions along the x- and y-axes.

[0037] The same references in the figures or description may be used for elements of the same type.

DETAILED DESCRIPTION OF THE INVENTION

[0038] The invention relates to a composite structure 100 and an associated manufacturing method. The composite structure 100 has a front face 100a and a rear face 100b extending parallel to a main plane (x,y). It comprises a working layer 10 made of single-crystal silicon carbide, preferably of polytype 4H, one free face of which forms the front face 100a, and a carrier substrate 20 made of polycrystalline silicon carbide 3C, one free face of which forms the rear face 100b ([Fig. 1]). The composite structure 100 also comprises an intermediate region 30 extending along the main plane (x,y) and including an interface zone between a bonded face of the working layer 10 and a bonded face of the carrier substrate 20. The intermediate region 30 comprises single-crystal silicon carbide inclusions 31 in direct contact with the working layer 10 and extending, in a direction (z) normal to the main plane (x,y), between grains 21i, 21j of the carrier substrate 20 ([Fig. 2]).

[0039] To facilitate understanding of the particular properties of the composite structure 100, linked in particular to this intermediate region 30, we will first describe the method for manufacturing said structure 100.

[0040] The method according to the invention comprises a step a) of providing a single-crystal silicon carbide (e.g. polytype 4H) donor substrate 1 with a given concentration of N-type dopants (called the first concentration). Typically, the

first concentration is between $1\times10^{18}/cm^3$ and $5\times10^{18}/cm^3$, corresponding to a resistivity range of between 20 and 30 mohm.cm.

[0041] The donor substrate 1 comprises a front face 1a intended to be bonded, and a rear face 1b ([Fig. 3a]). It comprises a buried brittle plane 11 induced by ion implantation of light species (in reference to the Smart Cut method). These species are for instance hydrogen, helium or a combination of these two species. The buried brittle plane delimits, together with the front face 1a of the donor substrate 1, the working layer 10 to be transferred.

[0042] The method comprises a step b) of providing a polycrystalline silicon carbide (polytype 3C) carrier substrate 20. The carrier substrate 20 comprises a front face 20a intended to be bonded, and a rear face 20b ([Fig. 3b]). It has a higher concentration of N-type dopants (called the second concentration) than the first concentration. Typically, the second concentration is between $1\times10^{20}/cm^3$ and $5\times10^{20}/cm^3$. To make it easier to provide the carrier substrate 20, the second concentration of dopants may preferably be limited to the range between $1\times10^{20}/cm^3$ and $2\times10^{20}/cm^3$.

[0043] The N-type dopant in the donor substrate 1 or in the carrier substrate 20 may notably be nitrogen.

[0044] Normally, in the field of microelectronics, the carrier substrate 20 and the donor substrate 1 take the form of circular wafers with diameters typically between 100 mm and 200 mm (if not larger). The (circular) front 1a, 20a and rear 1b, 20b faces of the wafers 1, 20 extend parallel to the main plane (x,y). The thicknesses of the donor substrate 1 and carrier substrate 20 are typically between 200 µm and 800 µm.

[0045] Advantageously, the carrier substrate 20 has the particularity of comprising, at least on the side of its face to be bonded 20a, silicon carbide grains 21i, 21j having a size less than or equal to 2 µm, less than or equal to 1

μm, or even less than or equal to 500 nm, said grains covering, in the main plane (x,y), a surface area greater than or equal to 20% of the face to be bonded 20a. The size of a grain 21i, 21j, bounded by grain boundaries 22, corresponds to the largest dimension of said grain 21i, 21j, in the main plane (x,y). To measure grain dimensions 21i, 21j or distances between grain boundaries 22, it is possible to use images obtained by conventional scanning electron microscopy (SEM) or electron back-scattered diffraction (EBSD). X-ray crystallography can also be used.

[0046] Advantageously, p-SiC grains 21i, 21j having a size less than or equal to 2 μm, less than or equal to 1 μm, or even less than or equal to 500 nm, cover, in the main plane (x,y), a surface area greater than or equal to 30%, 40%, 50%, 60%, 70%, or even greater than or equal to 80% of the front face to be bonded 20a of the carrier substrate 20. It is understood that the remainder of the surface area is occupied by larger grains.

[0047] The manufacturing method then comprises a step c) of depositing an (amorphous or polycrystalline) silicon film 3' on the face to be bonded 1a of the donor substrate 1, on the face to be bonded 20a of the carrier substrate 20, or on both faces 1a, 20a ([Fig. 3c]). Advantageously, this deposition is carried out by low-temperature sputtering, and involves a high vacuum, typically between $3x10^{-6}$ Pa and $8x10^{-6}$ Pa, before injecting the sputtering gas (Ar), then an atmosphere around 10^{-1} Pa and 10^{-2} Pa during deposition. The thickness of the deposited film 3' can vary from a few nm to several tens of nm.

[0048] The following step d) corresponds to directly bonding the donor substrate 1 and the carrier substrate 20 at their faces to be bonded 1a, 20a, so as to obtain a bonded assembly 50 comprising a silicon interlayer 3, derived from the film(s) 3' deposited in step c), between the donor substrate 1 and the carrier substrate 20 ([Fig. 3d]). This interlayer 3 advantageously has a thickness of between 8 nm and 30 nm.

[0049] This bonding is carried out by molecular-adhesion bonding, which consists in bringing the faces to be bonded 1a, 20a into contact without adding any adhesive material. It may be direct bonding between the working layer 10 and the silicon film 3', when the latter has been deposited only on the carrier substrate 20, or direct bonding between the carrier substrate 20 and the film 3', when the latter has been deposited only on the donor substrate 1, or even direct bonding between two silicon films 3', when these have been deposited on the donor substrate 1 and on the carrier substrate 20. Direct bonding is preferably carried out under a high vacuum, of the order of 10^{-6} Pa or less.

[0050] Advantageously, the deposition of step c) and the direct bonding of step d) are linked without breaking the vacuum, in situ or in a multi-chamber apparatus. By way of example, mention will be made of Atomic Diffusion Bonding BV7000 from the company Canon, wherein it is possible to successively carry out the deposition of the film 3' and direct bonding, by maintaining a controlled atmosphere.

[0051] The method then comprises a step e) involving separation along the buried brittle plane 11 to form a transferred structure 100' comprising the working layer 10, transferred from the donor substrate 1, disposed on the interlayer 3, itself disposed on the carrier substrate 20. Such a separation can be carried out during a heat treatment, typically around 900°C-1000°C, capable of growing cavities and microcracks, induced by the implanted species, in the buried brittle plane 11. The separation can also be carried out by applying mechanical stress, or by the combination of thermal and mechanical stresses, as is well known in reference to the Smart Cut method.

[0052] Sequences for cleaning, smoothing, polishing or etching the separated face 10a of the working layer 10 and/or of the separate face 1'a of the rest 1' of the donor substrate will be able to be operated so as to restore a good surface quality, in particular in terms of roughness, defectivity and other contaminations.

[0053] Finally, the method comprises a step f) which corresponds to applying a heat treatment to the transferred structure 100', at a plateau temperature of between 1500°C and 2000°C, advantageously between 1750°C and 2000°C, to form the composite structure 100 ([Fig. 3f], on the left). This temperature range causes the silicon in the interlayer 3 to melt. The interlayer 3 will segment into droplets to optimize its surface energy, and the liquid silicon 3'' of at least some of these droplets will diffuse into the grain boundaries 22. It will then be able to interact with the SiC grains 21i, 21j of the carrier substrate and dissolve a certain quantity of them. The dissolved carbon, the diffusion coefficient of which in liquid silicon is 1.7×10^{-8} m^2/s, is then transported from the dissolution zone to the interface between the liquid silicon and the single-crystal working layer 10. By recombining with the silicon, the carbon will enable single-crystal SiC to grow from the working layer 10, the latter acting as a seed ([Fig. 3f], on the right). This is similar to a TSSG ("Top Seeded Solution Growth") method, which consists in placing liquid silicon in a graphite crucible and then positioning a high-quality, single-crystal SiC seed on the surface of the liquid silicon; the carbon present on the crucible walls will dissolve on contact with the liquid silicon and diffuse therein via a temperature gradient up to the SiC seed. A single-crystal SiC then grows from this seed. In the present invention, this growth process takes place on a very local scale and at the interface between the working layer 10 and the carrier substrate 20: the graphite crucible is replaced by the grains 21i, 21j of the p-SiC carrier substrate, the seed is replaced by the c-SiC working layer 10, and the silicon source comes from the interlayer 3.

[0054] The composite structure 100 resulting from this step f) thus has an intermediate region 30, which extends along the main plane (x,y) and comprises inclusions 31 of single-crystal silicon carbide in direct contact with the working layer 10 and extending, in a direction (z) normal to the main plane (x,y), between grains 21i, 21j of the carrier substrate 20. The growth mode of these inclusions 31 favors the diffusion of dopants, present in grains 21i, 21j,

into said inclusions 31. As a result, the latter have a third concentration of N-type dopants between the first and second concentrations, which is highly conducive to establishing good electrical conduction between the working layer 10 and the carrier substrate 20. By way of example, for a first dopant concentration of $5\times10^{18}/cm^3$ and a second dopant concentration of $5\times10^{20}/cm^3$, the third dopant concentration is expected to be between 1×10^{20} and $1.5\times10^{20}/cm^3$.

[0055] The inclusions 31 typically have a thickness, along an axis (z) normal to the main plane (x,y), of between 20 nm and 70 nm, and a width, in the main plane (x,y), of between 100 nm and 700 nm. The size of the inclusions 31 depends in particular on the thickness of the silicon interlayer 3.

[0056] The intermediate region 30 has a density of inclusions 31, in the main plane (x,y), typically between $0.1/\mu m^2$ and $1/\mu m^2$. This density is all the greater when small-sized grains 21i, 21j (less than or equal to 2 µm, less than or equal to 1 µm, or even less than or equal to 500 nm) cover a large surface area of the bonded face 20a of the carrier substrate 20. According to the invention, these small grains cover more than 20% of the surface area of said bonded face 20a, more than 30%, more than 40%, more than 50%, more than 60%, more than 70%, or even 80% and more.

[0057] The crystallographic orientations of the grains 21i, 21j on the bonded face 20a of the carrier substrate 20 can also influence the formation, size and density of the inclusions 31. The density of inclusions 31 is also related to the thickness of the silicon interlayer 3, a greater quantity of silicon being able to increase said density in the intermediate region 30.

[0058] It should be noted that a significant misorientation of the grains between themselves or with respect to the orientation [111] is favorable to the interaction between the silicon droplets and the grain boundaries 22, since this misorientation is accompanied by grain boundaries 22 that are not very stable,

and it is then energetically favorable for the silicon to dissolve carbon atoms at said grain boundaries 22. A misorientation of more than 10°, 20° or even 30° appears to be particularly advantageous. Grain orientation can be observed by transmission electron microscopy (TEM) or electron back-scattered diffraction (EBSD).

[0059] Such a misorientation is expected between the grains 21i, 21j covering at least 20%, 30%, 40%, or even more than 50% of the surface area of the bonded face 20a of the carrier substrate 20; this objective can be assessed by statistical measurements on said face 20a.

[0060] The c-SiC inclusions 31 between the p-SiC grains (3C) have a special geometry. For example, in the case of a working layer 10 made of polytype 4H c-SiC, it has been observed that the base of inclusions 31 is perpendicular to the direction [0004] of the c-SiC of the working layer 10, parallel to the {0004} planes. Thus, the base of at least some inclusions 31 is not parallel to the main plane (x,y), but misoriented by 4° with respect to it. This is due to the fact that the {0004} planes of the SiC-4H single crystal are misoriented by 4° with respect to the bonded face 1a of the working layer 10 (and therefore with respect to the main plane) prior to step e). As the SiC in the form of inclusions 31 grows epitaxially from the working layer 10, the crystal planes maintain the same orientation. Growth therefore ends on {0004} planes, 4° from the main plane (x,y).

[0061] The orientation of the sidewalls of the c-SiC inclusion 31 seems to depend on the stability of the facets between the hexagonal single crystal and the cubic polycrystal. The inclination of the sidewalls also depends on the respective orientations of the grains 21i, 21j in contact with said inclusion 31. In general, the sidewalls of the inclusions 31 have an inclination of between 110° and 135° relative to the base.

[0062] The heat treatment in step f) plays an important role in the formation of these c-SiC inclusions 31. Thus, beyond a plateau temperature of between 1500°C and 2000°C, the duration of this plateau and the temperature ramp-ups and ramp-downs can also play a role.

[0063] The plateau temperature is preferably 1600°C, 1700°C, 1750°C, 1800°C, 1850°C, 1900°C or 1950°C. The duration of the plateau is set to allow carbon diffusion into the liquid silicon from the droplets at the grain boundaries 22, and the growth of inclusions 31 from the working layer 10. It is these inclusions 31 that promote vertical electrical conduction; the size and density thereof should therefore be optimized. Preferably, the plateau temperature is maintained for a duration of 30 minutes, 1 hour, 2 hours, 3 hours, 4 hours, or even longer.

[0064] The temperature ramp-up (to the plateau) is advantageously chosen to be less than or equal to 20°C/min, less than or equal to 10°C/min, or even less than or equal to 5°C/min, as this favors the flow of silicon from the interlayer 3 toward the grain boundaries 22. The same ramping ranges can be applied to lowering the temperature. In addition, these ramping ranges reduce the risk of "bubble"-type defects forming at the bonding interface.

[0065] The intermediate region 30 may further comprise silicon nodules 33, 32, arranged in the interface zone, or under inclusions 31 between grains 21i, 21j of the carrier substrate 20 ([Fig. 4]). In fact, some silicon droplets resulting from the segmentation of the interlayer 3 during the heat treatment in step f) may be located opposite a grain 21i, 21j and not a grain boundary 22: in this case, following their solidification during the temperature ramp-down of the heat treatment, they form silicon nodules 33 arranged between the working layer 10 and the carrier substrate 20 in the composite structure 100. Such a nodule 33 may have a thickness, along an axis (z) normal to the main plane (x,y), of between 50 nm and 200 nm, and a width, in the main plane (x,y), of between 200 nm and 400 nm.

[0066] It is also observed that liquid silicon 3'' that has diffused between grains 21i, 21j, along grain boundaries 22, can form a nodule 32 if it is not totally consumed in the growth of an inclusion 31: in this case, a silicon nodule 32 is again found, arranged under an inclusion 31 and between grains 21i, 21j of the carrier substrate 20, in the composite structure 100 at the end of step e). This type of nodule 32 may have dimensions, in the main plane (x,y), of the order of 200 nm to 400 nm, and a typical thickness, along the (z) axis, ranging from a few nm to a few μm. The interface between the c-SiC inclusion 31 and the underlying silicon nodule 32 is misoriented by 4° with respect to the main plane (x,y).

[0067] The intermediate region 30 further comprises an interface zone between a bonded face 1a of the working layer 10 and a bonded face 20a of the carrier substrate 20, said interface zone being due to the segmentation of the interlayer 3 which causes the appearance of direct contact zones between the c-SiC working layer 10 and the p-SiC carrier substrate 20. These direct contact zones can form steps 34, as can be seen in [Fig. 5]. It is assumed that the solubilization of p-SiC (3C) in liquid silicon 3'' during step f) enables the c-SiC (4H) of the working layer 10 to be reconstructed in the form of step bunching 34 in at least some of the direct contact zones between the thin layer 10 and the carrier substrate 20. It would appear that the steps 34 are located in direct contact zones where the grains 21i, 21j of the carrier substrate 20 exhibit little misorientation between themselves, whereas the c-SiC inclusions 31 described above are located in highly misoriented and/or thermodynamically unstable grains 21i, 21j.

[0068] The total thickness of the intermediate region 30, along an axis (z) normal to the main plane (x,y), is greater than or equal to the maximum thickness of the inclusions 31. The presence of silicon nodules 32 under all or some of the inclusions 31 can of course increase this total thickness.

[0069] To achieve good vertical electrical conduction, in other words, a resistivity of the intermediate region 30 that is as low as possible, preferably less than 1 mohm.cm^2, or even less than 0.1 mohm.cm^2, certain preferred embodiments are proposed, depending on the doping levels of the working layer 10 and the carrier substrate 20.

[0070] According to a first embodiment, the first concentration (working layer 10) of N-type dopants (nitrogen) is of the order of 5×10^{18}/cm^3, and the second concentration (carrier substrate 20) of N-type dopants (nitrogen) is of the order of 1×10^{20}/cm^3. To obtain the desired low resistivity, the carrier substrate 20 is chosen such that silicon carbide grains 21i, 21j having a size less than or equal to 500 nm cover, in the main plane (x,y), a surface area greater than or equal to 20% of its face to be bonded. This helps to achieve a density of c-SiC inclusions 31, which are favorable to vertical electrical conduction, compatible with the desired objective. The third concentration of dopants (inclusions) is between the first and second concentrations.

[0071] According to a second embodiment, the first concentration of N-type dopants (working layer) is of the order of 3×10^{18}/cm^3, and the second concentration of N-type dopants (carrier substrate) is of the order of 1×10^{20} /cm^3. To obtain the desired low resistivity, the carrier substrate is chosen such that silicon carbide grains having a size less than or equal to 500 nm cover, in the main plane, a surface area greater than or equal to 50%, or even 60% of its face to be bonded. This helps to achieve a density of c-SiC inclusions 31 with a third dopant concentration between the first and second concentrations, which inclusions are favorable to vertical electrical conduction, compatible with the desired objective.

[0072] According to a third embodiment, the first concentration of N-type dopants (working layer) is of the order of 1×10^{18}/cm^3, and the second concentration of N-type dopants (carrier substrate) is of the order of 1×10^{20}/cm^3. To obtain the desired low resistivity, the carrier substrate is chosen

such that silicon carbide grains having a size less than or equal to 500 nm cover, in the main plane, a surface area greater than or equal to 80% of its face to be bonded. Here again, this helps to achieve a density of c-SiC inclusions 31 with a third dopant concentration between the first and second concentrations, which inclusions are favorable to vertical electrical conduction, compatible with the desired objective.

[0073] [Fig. 6] shows theoretical curves obtained by numerical simulations of vertical electron transport in the composite structure 100. They show the evolution of the resistivity of the intermediate region 30 as a function of the percentage of the surface area of the carrier substrate 20 (on the side of its bonded face 20a) in which the grains 21i, 21j have a size less than or equal to 500 nm. When the second dopant concentration of the carrier substrate 20 (denoted $N_{polySiC}$ in [Fig. 6]) is very high (typically $5\times10^{20}/cm^3$), it is not critical that the carrier substrate 20 has a certain percentage of small grains (< 500 nm), as a resistivity of less than 10^{-5} ohm.cm^2 can be achieved regardless of the doping level of the working layer 10 (between $1\times10^{18}/cm^3$ and $5\times10^{18}/cm^3$). On the other hand, when the second dopant concentration is of the order of $1\times10^{20}/cm^3$, achieving a resistivity of less than 10^{-5} ohm.cm^2 will depend on the presence of small grains favorable to the formation of c-SiC inclusions 31, which benefit from a third dopant concentration higher than the first concentration of the working layer 10. The lower the first concentration, the higher the percentage of surface area of the bonded face 20a of the carrier substrate 20 containing grains 21i, 21j having a size less than or equal to 500 nm.

[0074] The invention also relates to a composite structure 100 having a front face 100a and a rear face 100b extending parallel to the main plane (x,y) ([Fig. 1]). It comprises a working layer 10 with a first concentration of N-type dopants. Typically, the first concentration is between $1\times10^{18}/cm^3$ and $5\times10^{18}/cm^3$.

[0075] It also comprises a carrier substrate 20 with a second concentration of N-type dopants, said second concentration being higher than the first concentration. Typically, the second concentration is between $1\times10^{20}/cm^3$ and $5\times10^{20}/cm^3$, or even preferably limited to the range between $1\times10^{20}/cm^3$ and $2\times10^{20}/cm^3$.

[0076] Advantageously, the carrier substrate 20, at least on the side of its bonded face 20a, comprises silicon carbide grains 21i, 21j having a size less than or equal to 2 µm, less than or equal to 1 µm, or even less than or equal to 500 nm, said grains covering, in the main plane (x,y), a surface area greater than or equal to 20% of the bonded face 20a. In particular embodiments, silicon carbide grains 21i, 21j having a size less than or equal to 2 µm, less than or equal to 1 µm, or even less than 500 nm, cover, in the main plane (x,y), a surface area greater than or equal to 30%, 40%, 50%, 60%, 70%, or even 80% of the bonded face 20a of the carrier substrate 20.

[0077] Advantageously, the grains of the carrier substrate 20, on the side of its bonded face 20a, are significantly misoriented between themselves (that is, between two adjacent grains) or with respect to the orientation [111]: as previously mentioned in the method according to the invention, this is favorable to the interaction between the silicon droplets and the grain boundaries 22 (in step f), as the low stability of the grain boundaries 22, associated with this misorientation, makes it energetically favorable for the silicon to dissolve carbon atoms at said grain boundaries 22. A misorientation of more than 10°, 20° or even 30° appears to be particularly favorable. Such a misorientation is expected between grains 21i, 21j covering at least 20%, 30%, 40%, or even more than 50% of the surface area of the bonded face 20a of the carrier substrate 20.

[0078] The composite structure 100 also comprises an intermediate region 30 extending along the main plane (x,y) and including an interface zone between

a bonded face 1a of the working layer 10 and a bonded face 20a of the carrier substrate 20.

[0079] The intermediate region 30 comprises single-crystal silicon carbide inclusions 31 in direct contact with the working layer 10 and extending, in a direction (z) normal to the main plane (x,y), between grains 21i, 21j of the carrier substrate 20. Said inclusions 31 have a third concentration of N-type dopants between the first and second concentrations. The presence of these inclusions 31 provides an important advantage in terms of electrical conduction of the intermediate region 30 of the composite structure 100.

[0080] The intermediate region 30 may have a density of inclusions 31, in the main plane (x,y), between $0.1/\mu m^2$ and $1/\mu m^2$.

[0081] The inclusions 31 typically have a thickness, along an axis (z) normal to the main plane (x,y), of between 20 nm and 70 nm, and a width, in the main plane (x,y), of between 100 nm and 700 nm.

[0082] As already mentioned in the description of the method for manufacturing the composite structure 100, the intermediate region 30 may also comprise silicon nodules 32, 33 and steps 34 at the interface zone between the bonded face of the working layer 10 and that of the carrier substrate 20.

[0083] Of course, the invention is not limited to the described embodiments, and variant embodiments may be envisaged without departing from the scope of the invention as defined by the claims.

Claims

[Claim 1] A composite structure (100) having a front face (100a) and a rear face (100b) extending parallel to a main plane (x,y), and comprising:
- a working layer (10) made of single-crystal silicon carbide, one free face of which forms the front face (100a), with a first concentration of N-type dopants,
- a carrier substrate (20) made of polycrystalline silicon carbide, one free face of which forms the rear face (100b), with a second concentration of N-type dopants, the second concentration being higher than the first concentration,
- an intermediate region (30) extending along the main plane (x,y) and including an interface zone between a bonded face (1a) of the working layer (10) and a bonded face (20a) of the carrier substrate (20);
the composite structure (100) being characterized in that the intermediate region (30) comprises single-crystal silicon carbide inclusions (31) in direct contact with the working layer (10) and extending, in a direction (z) normal to the main plane (x,y), between grains (21i, 21j) of the carrier substrate (20), said inclusions (31) having a third N-type dopant concentration between the first and second concentrations.

[Claim 2] The composite structure (100) according to claim 1, wherein the carrier substrate (20), at least on the side of its bonded face (20a), comprises silicon carbide grains (21i, 21j) having a size less than or equal to 500 nm, said grains (21i, 21j) covering, in the main plane (x,y), a surface area greater than or equal to 20% of the bonded face (20a).

[Claim 3] The composite structure (100) according to any one of the preceding claims, wherein the silicon carbide grains (21i, 21j) having a size less than 500 nm cover, in the main plane (x,y), a surface area greater than or equal to 50% or even 80% of the bonded face (20a) of the carrier substrate (20).

[Claim 4] The composite structure (100) according to any one of the preceding claims, wherein at least 20% of the silicon carbide grains (21i, 21j), on the side of the bonded face (20a) of the carrier substrate (20), have a misorientation, between themselves or with respect to the orientation [111], greater than or equal to 30°.

[Claim 5] The composite structure (100) according to any one of the preceding claims, wherein the intermediate region (30) comprises silicon nodules (32, 33) arranged in the interface zone or under the inclusions (31) between grains (21i, 21j) of the carrier substrate (20).

[Claim 6] The composite structure (100) according to any one of the preceding claims, wherein the first concentration is between $1\times10^{18}/cm^3$ and $5\times10^{18}/cm^3$.

[Claim 7] The composite structure (100) according to any one of the preceding claims, wherein the second concentration is between $1\times10^{20}/cm^3$ and $5\times10^{20}/cm^3$, preferably between $1\times10^{20}/cm^3$ and $2\times10^{20}/cm^3$.

[Claim 8] The composite structure (100) according to any one of the preceding claims, wherein the inclusions (31) have a thickness, along an axis (z) normal to the main plane (x,y), of between 20 nm and 70 nm, and a width, in the main plane (x,y), of between 100 nm and 700 nm.

[Claim 9] The composite structure (100) according to any one of the preceding claims, wherein the intermediate region (30) has a density of inclusions (31), in the main plane (x,y), of between $0.1/\mu m^2$ and $1/\mu m^2$.

[Claim 10] A method for manufacturing a composite structure (100) according to any one of claims 1 to 9, comprising the following steps:
a) providing a single-crystal silicon carbide donor substrate (1) with a first concentration of N-type dopants, and comprising a buried brittle plane (11)

induced by ion implantation of light species;
b) providing a polycrystalline carrier substrate (20);
c) depositing a silicon film (3') on a face to be bonded (1a) of the donor substrate (1) and/or on the face to be bonded (20a) of the carrier substrate (20);
d) bonding the donor substrate (1) and the carrier substrate (20) at their faces to be bonded (1a, 20a), so as to obtain a bonded assembly (50) comprising a silicon interlayer (3), derived from the film(s) (3') deposited in step c), between the donor substrate (1) and the carrier substrate (20), said interlayer (3) having a thickness of between 8 nm and 30 nm;
e) separating along the buried brittle plane (11) to form a transferred structure (100') comprising the working layer (10), transferred from the donor substrate (1), disposed on the interlayer (3), itself disposed on the carrier substrate (20);
f) applying a heat treatment to the transferred structure (100'), at a plateau temperature of between 1500°C and 2000°C, to form the composite structure (100).

[Claim 11] The method for manufacturing a composite structure (100) according to claim 10, wherein the carrier substrate (20) comprises, at least on the side of a face to be bonded (20a), silicon carbide grains (21i, 21j) having a size less than or equal to 500 nm, said grains (21i, 21j) covering, in the main plane (x,y), a surface area greater than or equal to 20% of the face to be bonded (20a).

[Claim 12] The method for manufacturing a composite structure (100) according to any one of claims 10 and 11, wherein at least 20% of the silicon carbide grains (21i, 21j), on the side of the bonded face (20a) of the carrier substrate (20), have a misorientation, between themselves or with respect to the orientation [111], greater than or equal to 30°.

[Claim 13] The method for manufacturing a composite structure (100) according to any one of claims 10 to 12, wherein the plateau temperature is maintained for a duration of between 30 minutes and 4 hours.

[Claim 14] The method for manufacturing a composite structure (100) according to any one of claims 10 and 13, wherein the treatment in step f) has a temperature ramp-up of less than or equal to 20°C/min, or even less than or equal to 10°C/min.

[Claim 15] The method for manufacturing a composite structure (100) according to any one of claims 10 to 14, wherein:
- the second concentration is of the order of $1\times10^{20}/cm^3$,
- the first concentration is of the order of $3\times10^{18}/cm^3$, and
- the silicon carbide grains (21i, 21j) having a size less than or equal to 500 nm cover, in the main plane (x,y), a surface area greater than or equal to 50% or even 60% of the face to be bonded (20a) of the carrier substrate (20).

[Claim 16] The method for manufacturing a composite structure (100) according to any one of claims 10 to 14, wherein:
- the second concentration is of the order of $1\times10^{20}/cm^3$,
- the first concentration is of the order of $1\times10^{18}/cm^3$, and
- the silicon carbide grains (21i, 21j) having a size less than or equal to 500 nm cover, in the main plane (x,y), a surface area greater than or equal to 80% of the face to be bonded (20a) of the carrier substrate (20).