ABSTRACT OF THE DISCLOSURE

SIMULTANEOUS DEPOSIT AND ETCH METHOD FOR FORMING A VOID–FREE AND GAP–FILLING INSULATOR LAYER UPON A PATTERNED SUBSTRATE LAYER

A method for forming a void-free and gap-filling doped silicon oxide insulator layer upon a patterned substrate layer within an integrated circuit. Formed upon a semiconductor substrate is a patterned substrate layer. Formed upon the patterned substrate layer is a doped silicon oxide insulator layer. The doped silicon oxide insulator layer is formed through a Plasma Enhanced Chemical Vapor Deposition (PECVD) deposition method undertaken simultaneously with a Reactive Ion Etch (RIE) etch-back method. The Plasma Enhanced Chemical Vapor Deposition (PECVD) deposition method and the Reactive Ion Etch (RIE) etch-back method simultaneously employ a Tetra Ethyl Ortho Silicate (TEOS) silicon source material, a dopant source material, an oxygen source material and an etching gas.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)