

ABSTRACT

A memory module includes first memory chips, each having a first input/output width, and configured to store data, a second memory chip having a second input/output width and configured to store an error correction code for correcting an error in the data, and a driver
5 circuit configured to receive a clock signal, a command, and an address from a memory controller and to transmit the clock signal, the command, and the address to the first memory chips and the second memory chip. An address depth of each of the first memory chips and an address depth of the second memory chip are different from each other.

FIG. 1