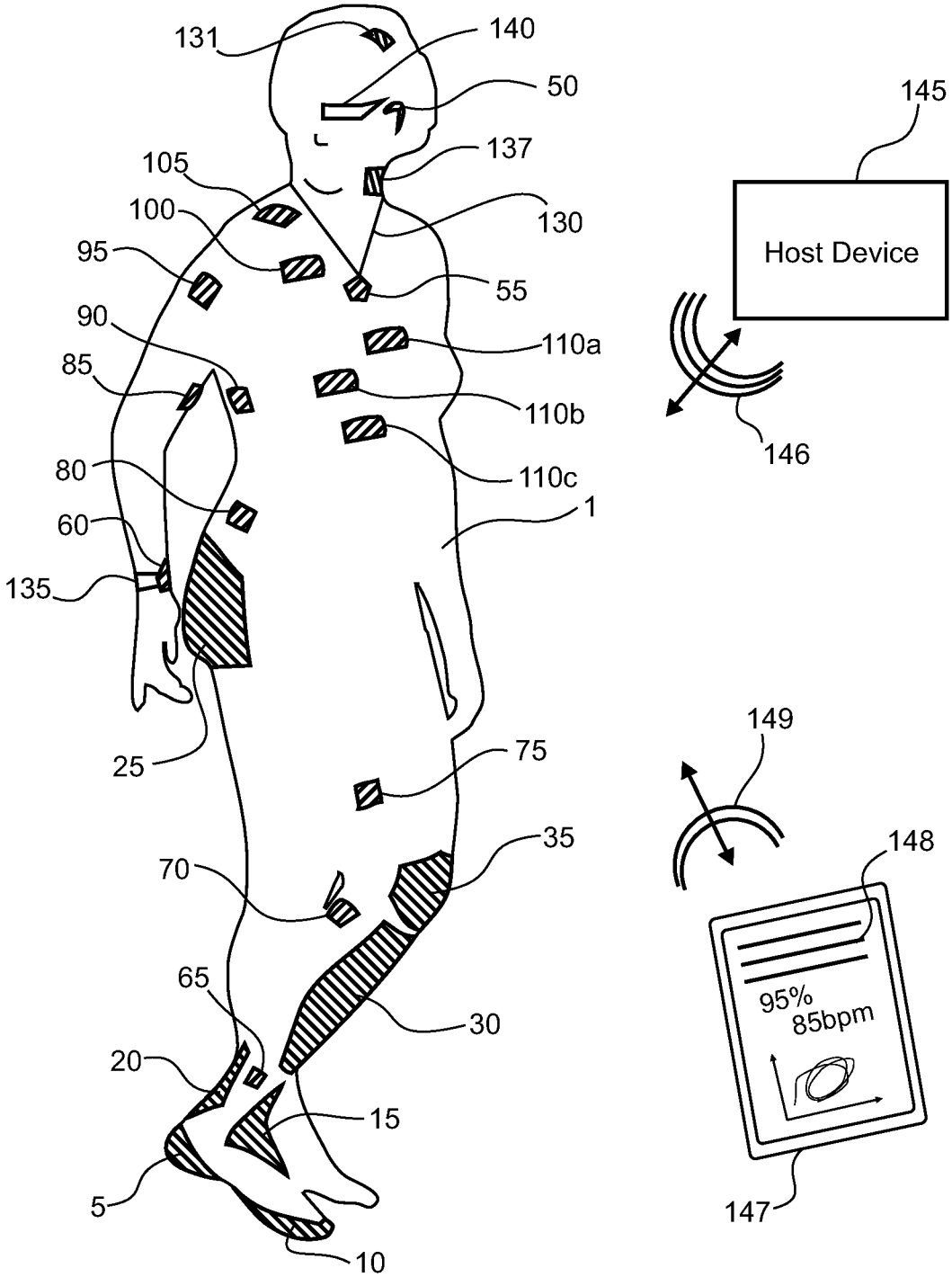

131
140
50
145
105
137
100
130
Host Device
95
55
90
110a
85
110b
110c
80
1
60
135
146
149
75
25
35
148
70
65
30
95%
85bpm
20
15
5
147
10

Fig 1a

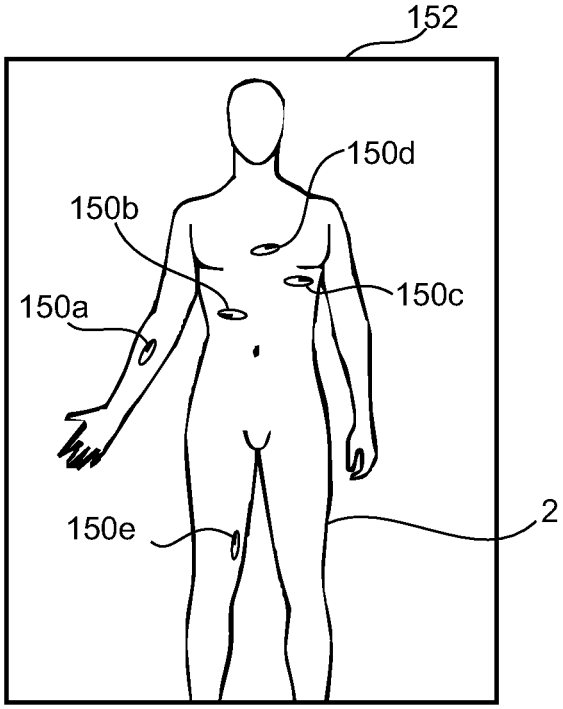


Fig 1b

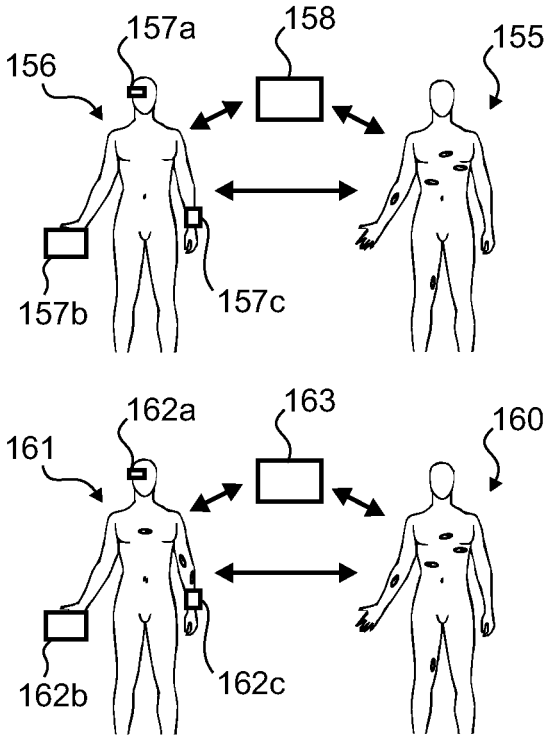


Fig 1c

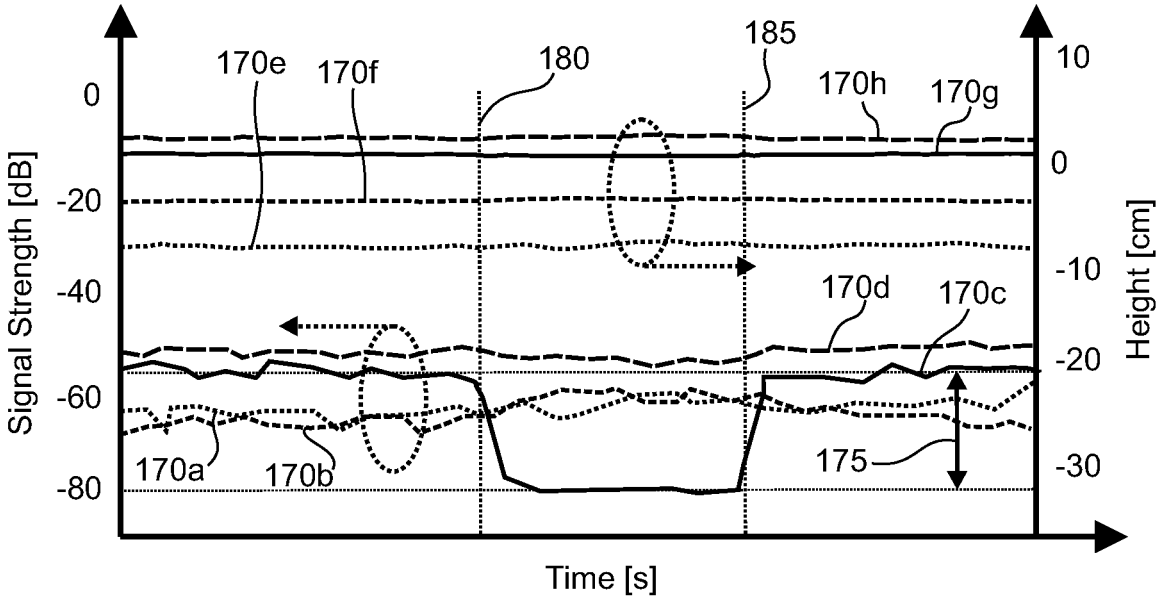


Fig 1d

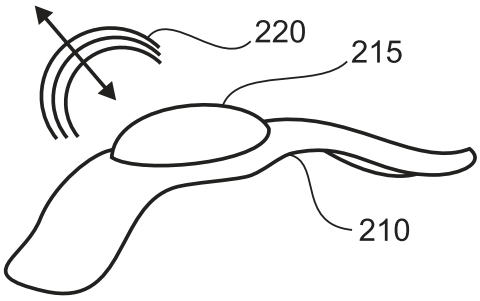


Fig 2a

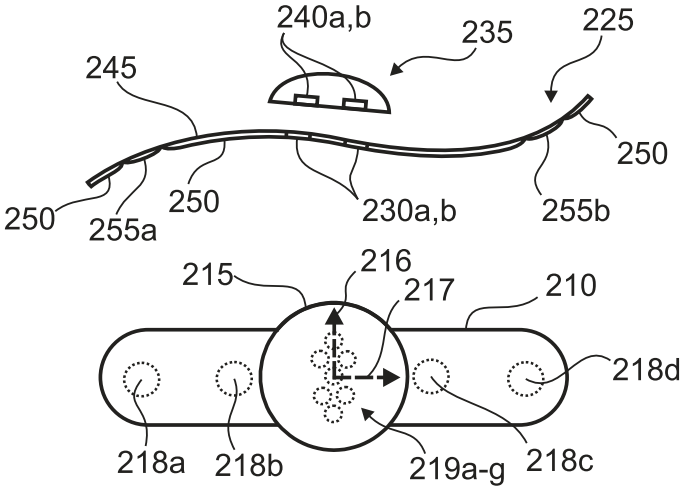


Fig 2b

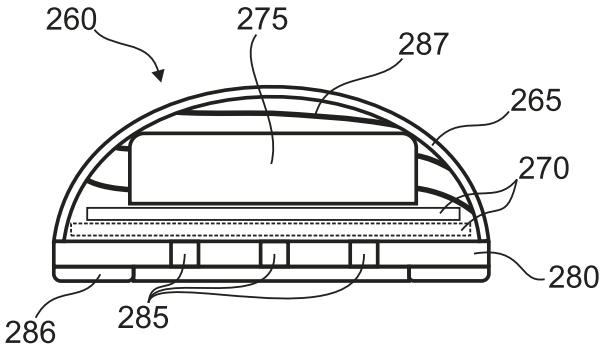


Fig 2c

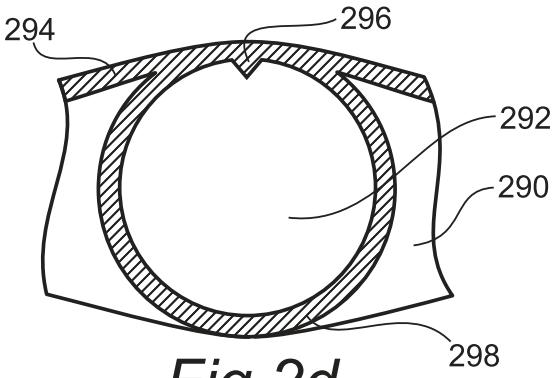


Fig 2d

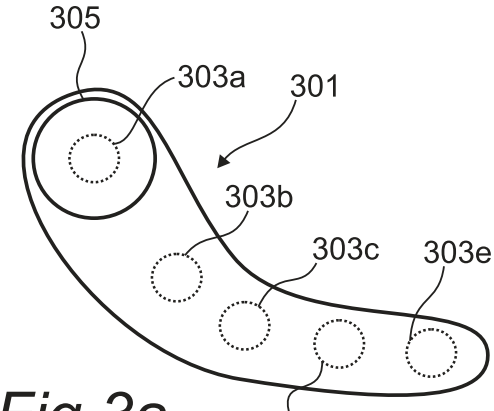


Fig 3a

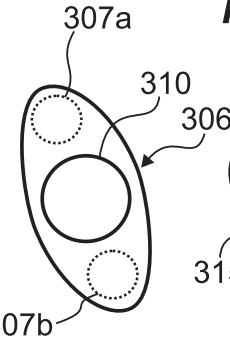


Fig 3b

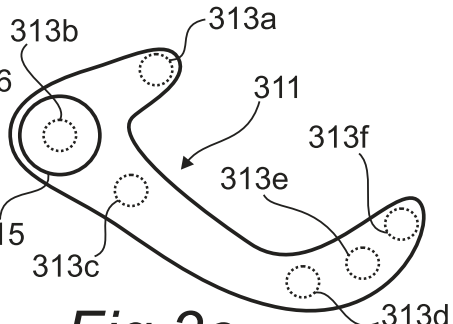


Fig 3c

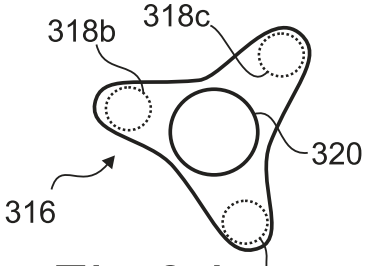


Fig 3d

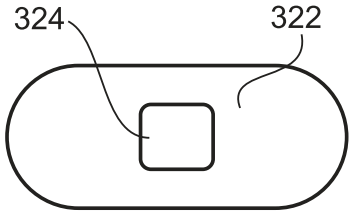


Fig 3e

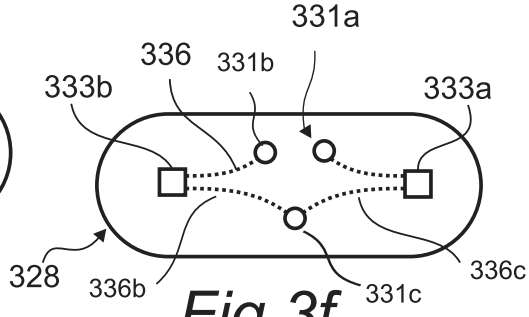


Fig 3f

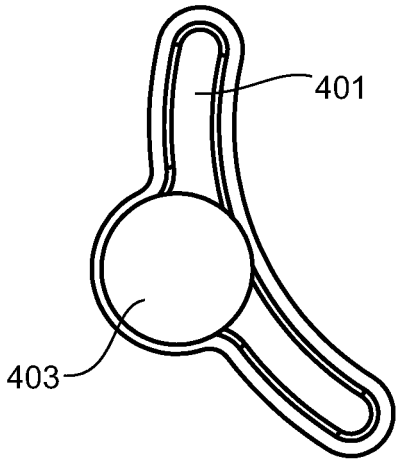


Fig 4a

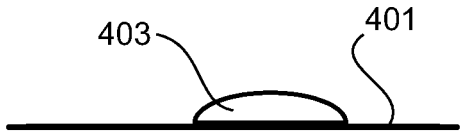


Fig 4b

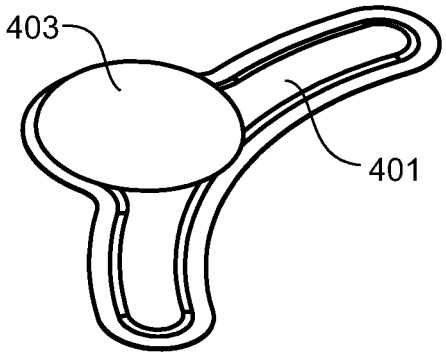


Fig 4c

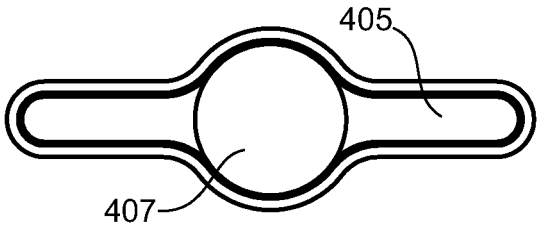


Fig 4d



Fig 4e

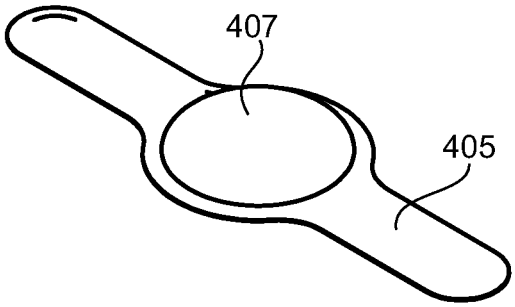


Fig 4f

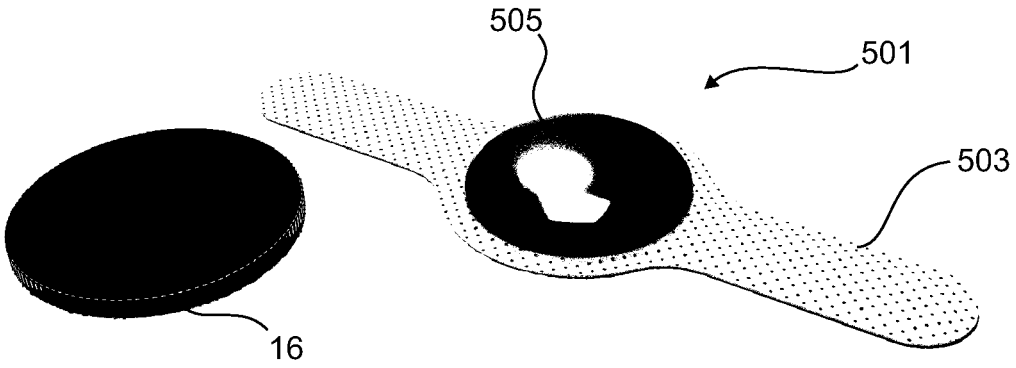

505
501
503
16

Fig 5

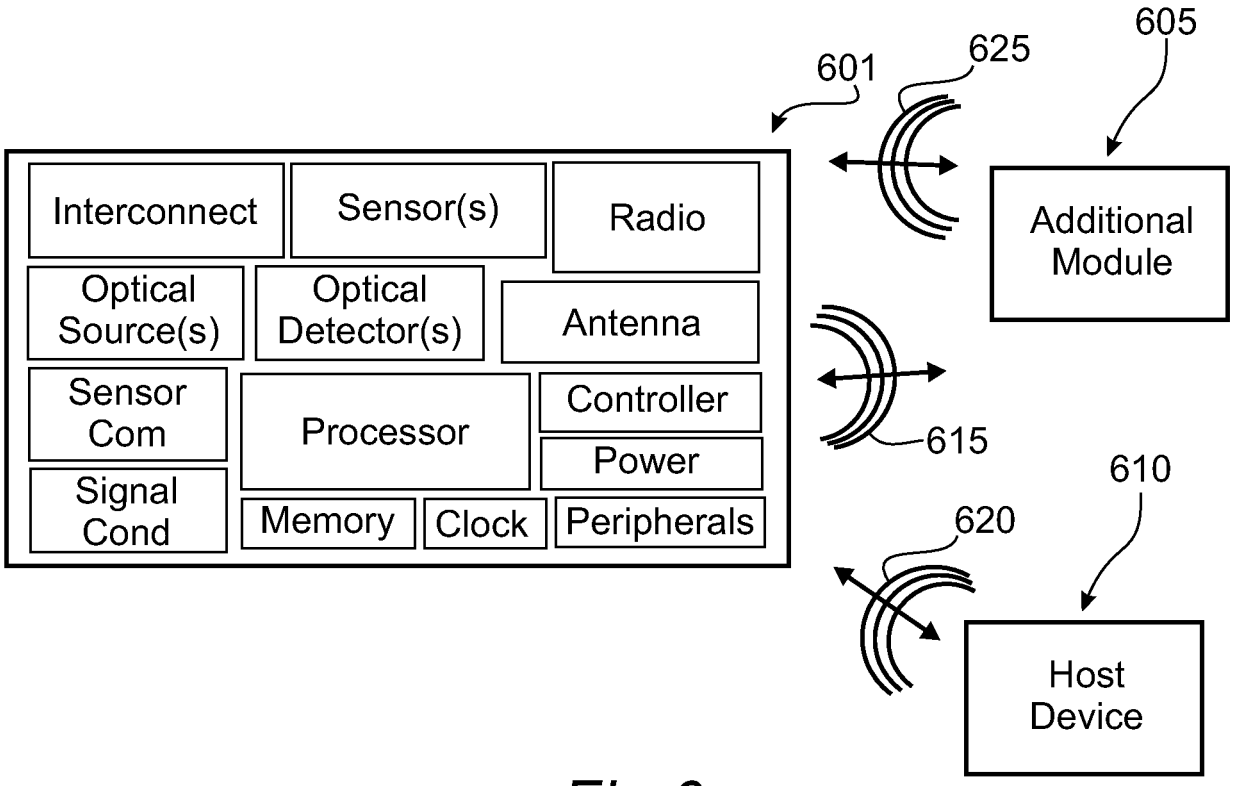

605
601
625
Interconnect
Sensor(s)
Radio
Optical Source(s)
Optical Detector(s)
Antenna
Additional Module
Sensor Com
Processor
Controller
Power
615
Signal Cond
Memory
Clock
Peripherals
610
620
Host Device

Fig 6

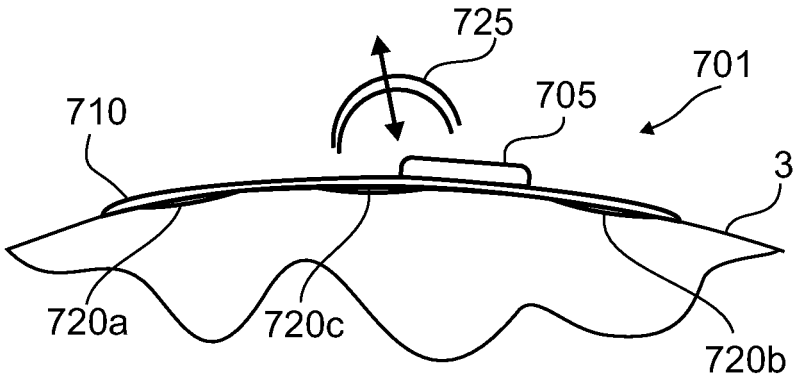


Fig 7

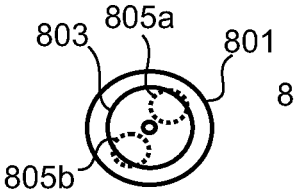


Fig 8a

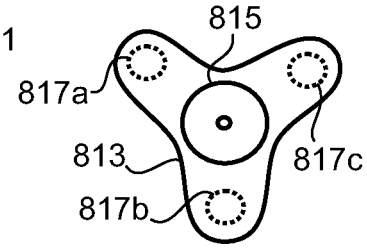


Fig 8c

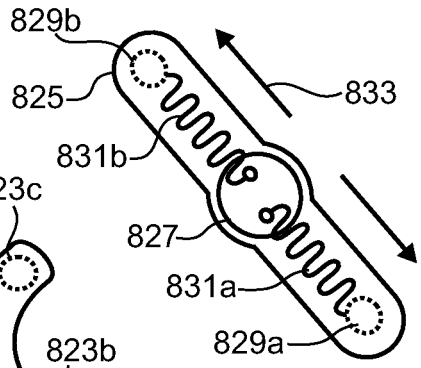


Fig 8e

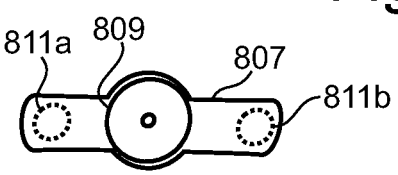


Fig 8b

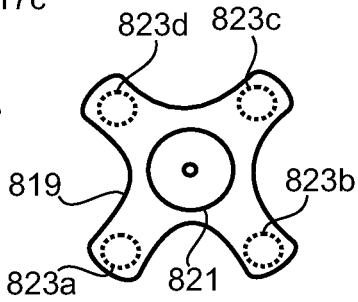
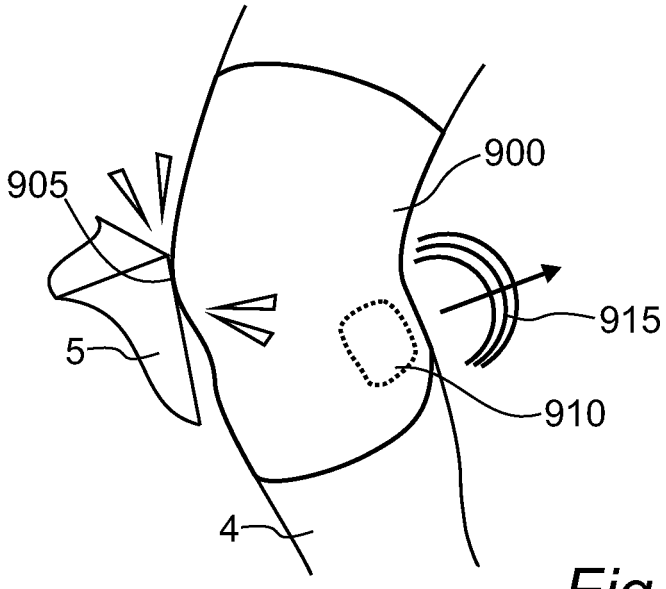


Fig 8d



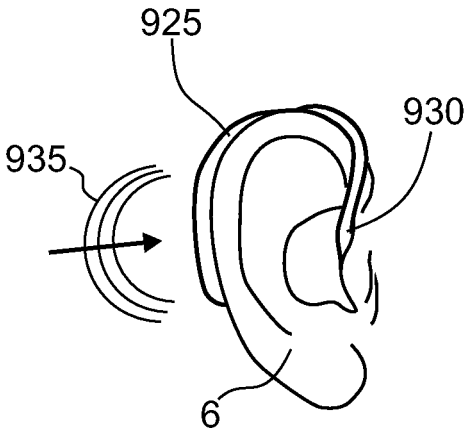


Fig 9

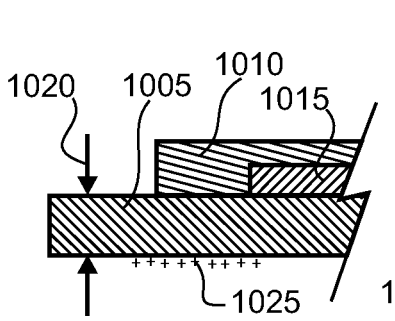


Fig 10a

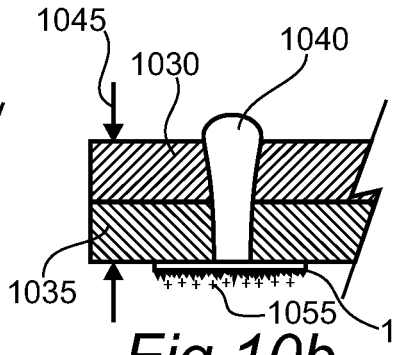


Fig 10b

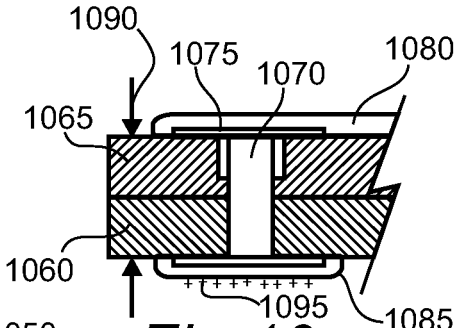


Fig 10c

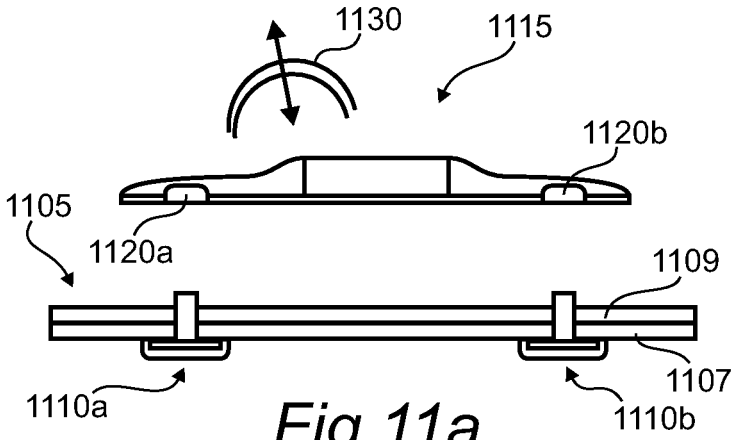


Fig 11a

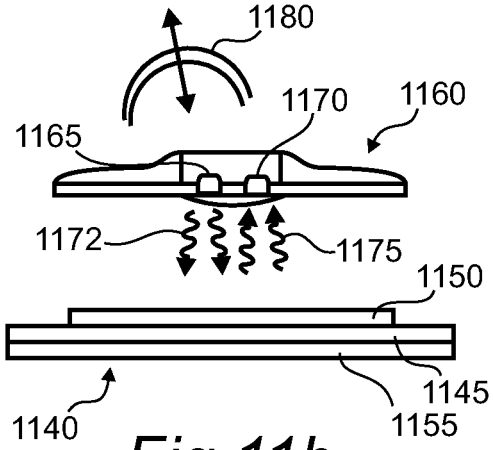


Fig 11b

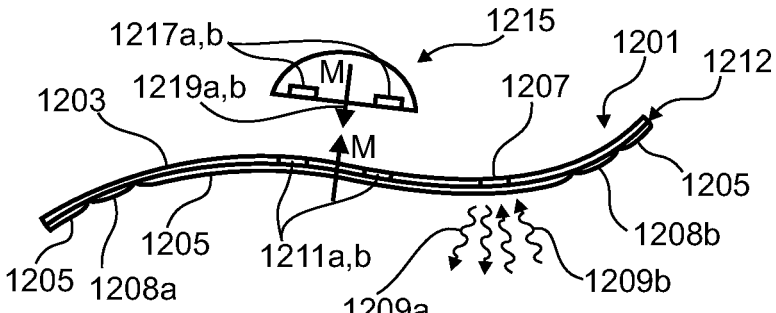


Fig 12a

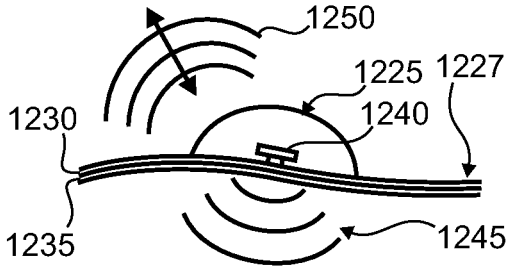


Fig 12b

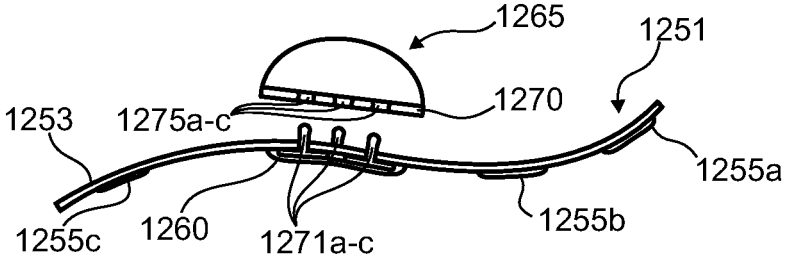


Fig 12c

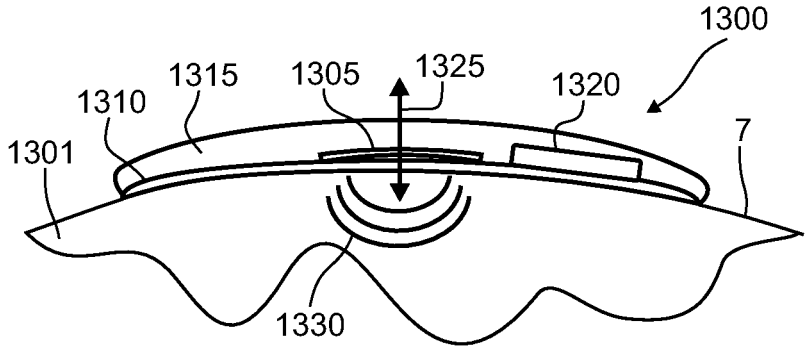


Fig 13

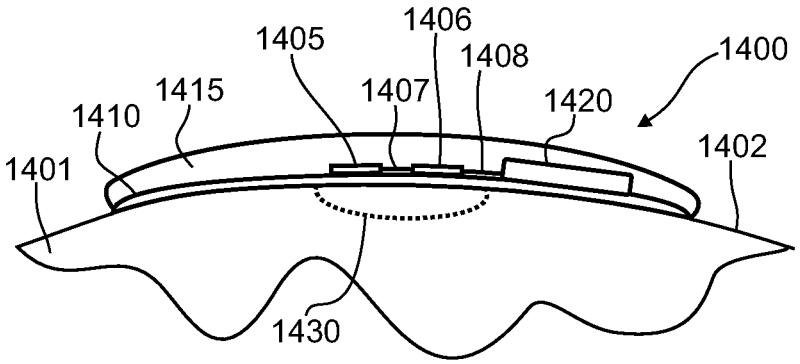


Fig 14

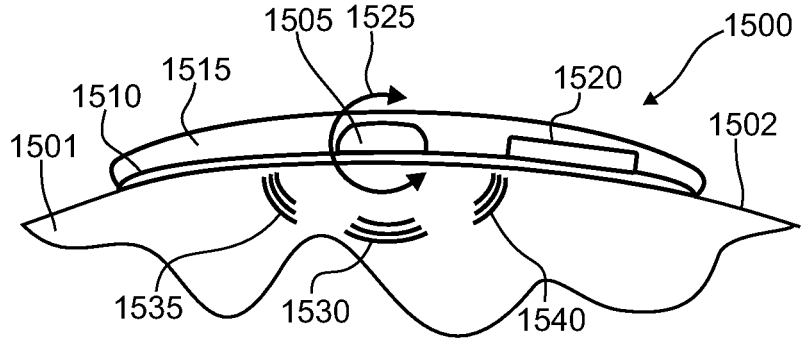


Fig 15

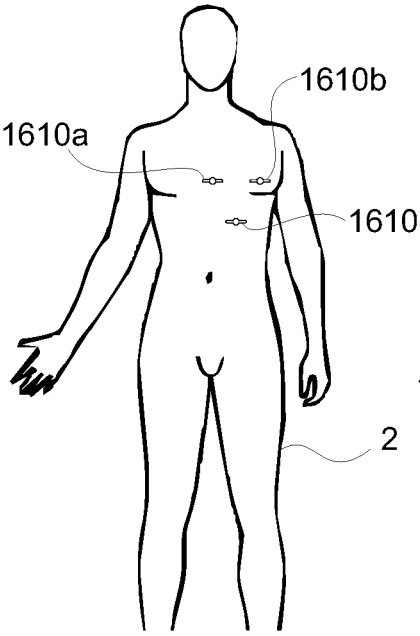


Fig 16a

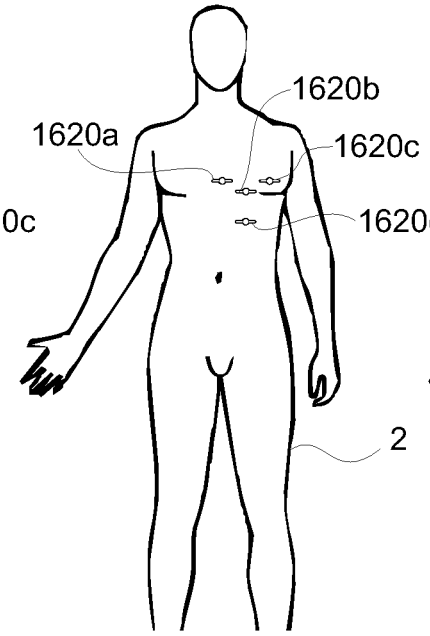


Fig 16b

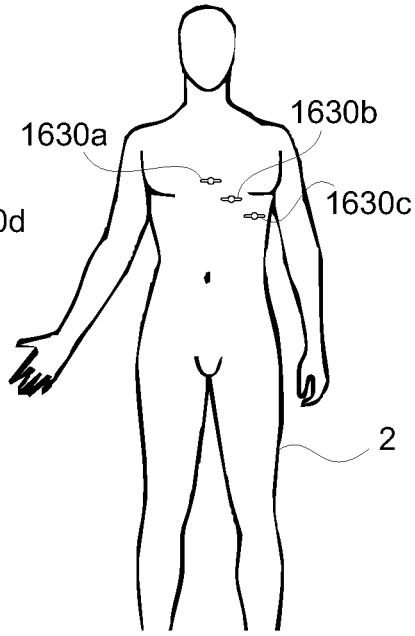


Fig 16c

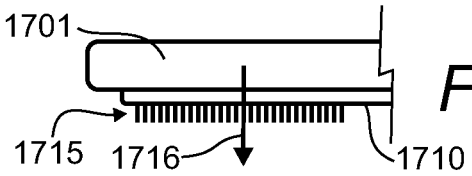


Fig 17a

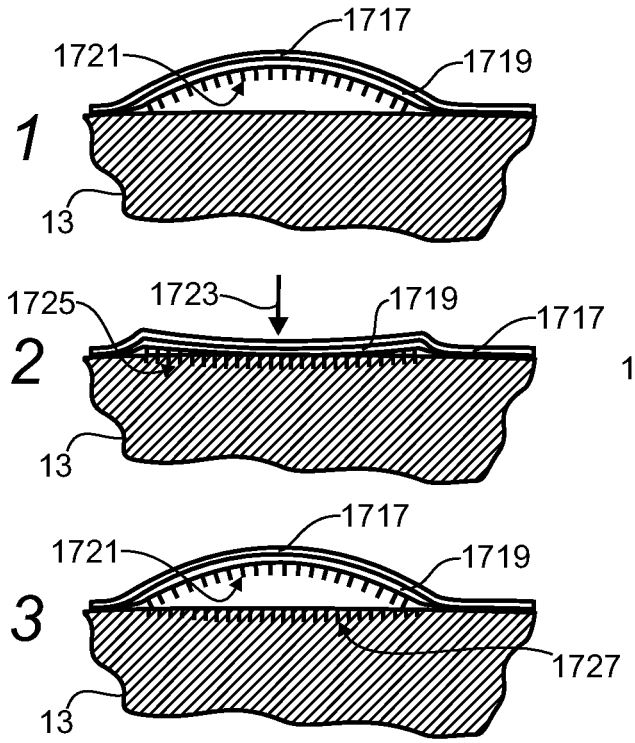


Fig 17b

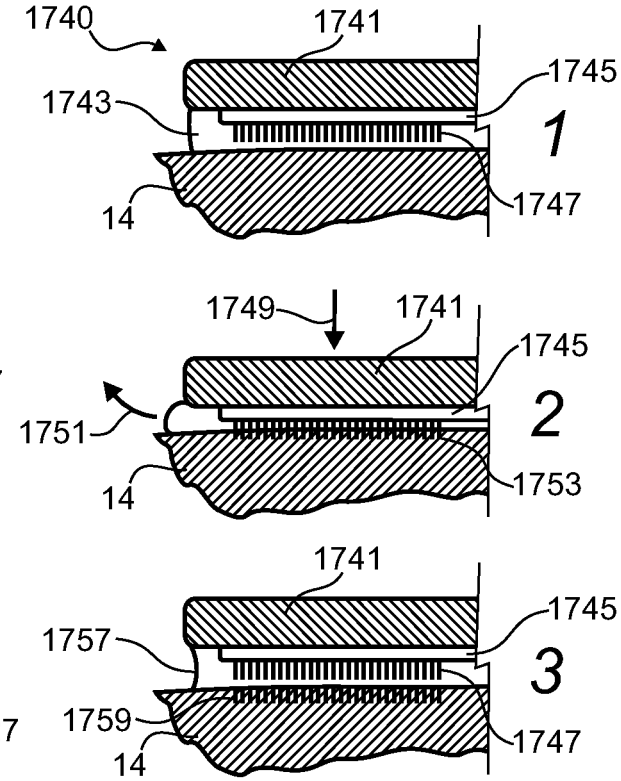


Fig 17c

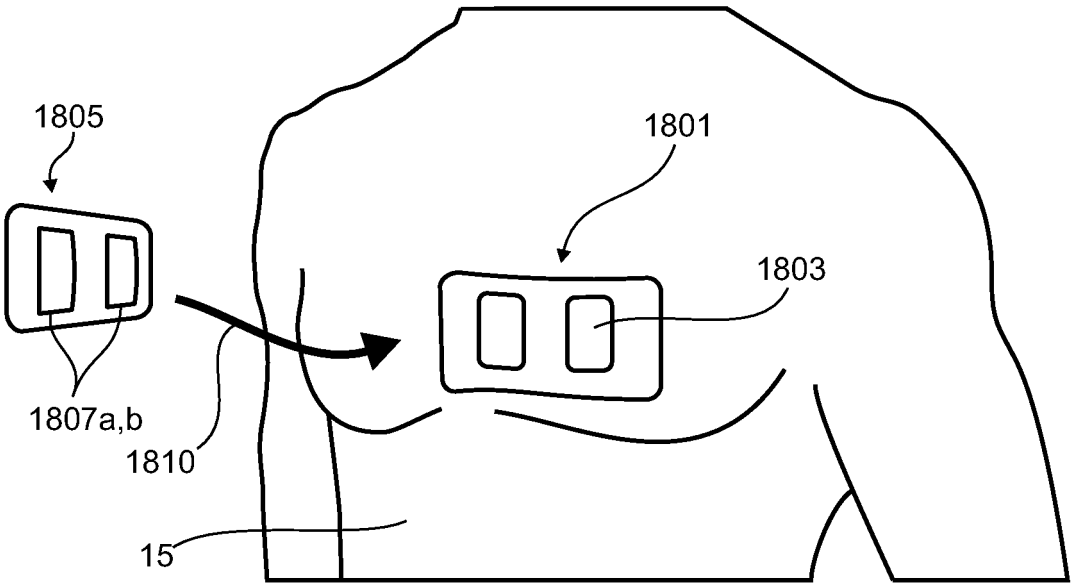

1805
1801
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Fig 18

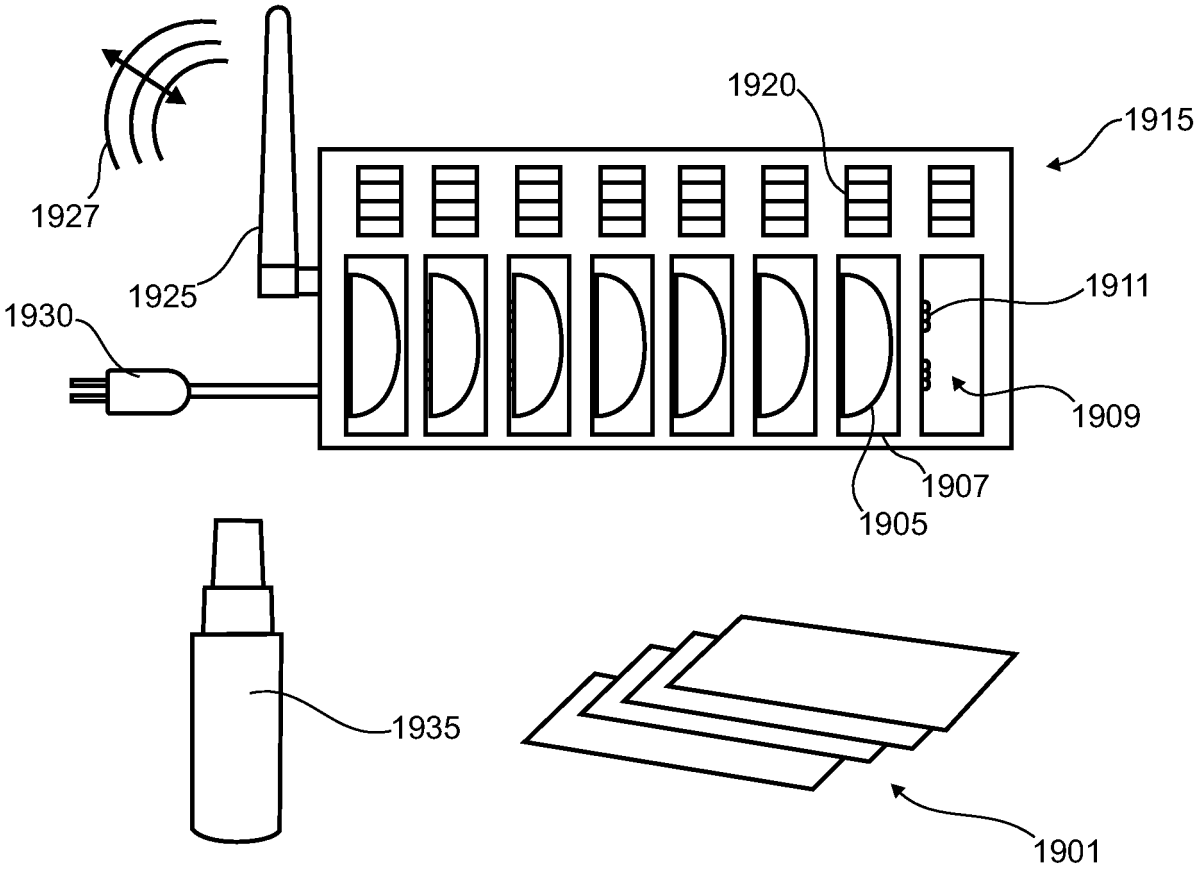

1920
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1901

Fig 19