WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array including memory cells connected to word lines which are arranged in order depending on a change of a row address;

a row decoder configured to scramble a first bit of the row address and a second bit of the row address depending on a selection signal, thereby forming a scrambled row address, to decode the scrambled row address, and to select the word lines; and

an anti-fuse array including an anti-fuse in which a logical value of the selection signal is stored,

wherein a first word line and a second word line of the word lines are adjacent to each other, and

wherein a difference between a first value of the row address corresponding to the first word line and a second value of the row address corresponding to the second word line is a value corresponding to the first bit.

2. The memory device of claim 1, wherein:

the first bit is a least significant bit of each row address, and

the second bit is an upper bit other than the least significant bit of each row address.

3. The memory device of claim 1 or claim 2, wherein the row decoder includes:

a first multiplexer configured to output the second bit instead of the first bit depending on the selection signal; and

a second multiplexer configured to output the first bit instead of the second bit depending on the selection signal,

wherein the scrambled row address includes the second and first bits respectively output from the first and second multiplexers.

4. The memory device of claim 3, wherein the memory cell array includes a sub word line driver driving each of the word lines,

wherein the row decoder is configured to provide a first decoding signal to a power terminal of the sub word line driver and to provide a second decoding signal to an input terminal of the sub word line driver, and

wherein the row decoder is configured to generate the first decoding signal by decoding a first bit of the scrambled row address, which is identical to the second bit of the row address, and an upper bit of the scrambled row address following the first bit of the scrambled row address.

5. The memory device of claim 4, wherein the row decoder is configured to generate the second decoding signal by decoding a second bit of the scrambled row address, which is identical to the first bit of the row address, and an upper bit of the scrambled row address following the second bit of the scrambled row address, and

wherein the second bit of the scrambled row address is not used to generate the first decoding signal.

6. The memory device of any one of claims 3 to 5, wherein the memory cell array further includes bit line sense amplifiers connected to bit lines connected to the memory cells,

wherein the memory cells are divided into mats with respect to regions in which the bit line sense amplifiers are placed, and

wherein the row decoder is configured to select the mats by decoding a first bit of the

scrambled row address, which is identical to the first bit of the row address, and an upper bit of the scrambled row address following the first bit of the scrambled row address.

7. The memory device of any one of claims 3 to 6, wherein the row decoder further includes:

a third multiplexer configured to output a fourth bit of the row address instead of a third bit of the row address depending on the selection signal; and

a fourth multiplexer configured to output the third bit instead of the fourth bit depending on the selection signal,

wherein the scrambled row address includes the second, first, fourth, and third bits respectively output from the first, second, third, and fourth multiplexers.

8. The memory device of any one of claims 1 to 7, further comprising:

a command decoder configured to receive a command and an address from an outside of the memory device and to transmit the address to the row decoder as the row address depending on the command.

9. The memory device of any one of claims 1 to 8, configured such that after the memory device is packaged and is mounted on a module, the logical value of the selection signal can be used to program the anti-fuse.

10. The memory device of any one of claims 1 to 9, wherein each of the memory cells includes one transistor connected to each of the word lines and one capacitor connected to the transistor.

11. A memory device comprising:

a memory cell array including memory cells connected to word lines which are arranged in sequential order depending on a sequential change of a row address;

a row decoder configured to scramble a particular-positioned bit of the row address and another-positioned bit of the row address based on a selection signal, thereby forming a scrambled row address, to decode the scrambled row address, and to select the word lines; and

an anti-fuse array including an anti-fuse in which a logical value of the selection signal is stored,

wherein a first word line corresponding to a first value of the row address and a second word line corresponding to a first value of the scrambled row address are not adjacent to each other,

wherein the first word line corresponding to the first value of the row address and a third word line corresponding to a second value of the row address are adjacent to each other, and

wherein a difference between the first value of the row address and the second value of the row address is a decimal value of 1.

12. The memory device of claim 11, wherein:

the row decoder includes multiplexers configured to receive the selection signal and an address including the particular-positioned bit and the another-positioned bit as inputs, and to output an address having the particular-positioned bit and the another-positioned bit swapped when the selection signal has a particular state.

13. The memory device of claim 11 or claim 12, wherein:

the particular-positioned bit is a least significant bit; and

the another-positioned bit is a different-positioned bit other than the least significant bit.

14. A memory device comprising:

a memory cell array including first memory cells connected to a first word line, second memory cells connected to a second word line adjacent to the first word line, and third memory cells connected to a third word line not adjacent to the first and second word lines;

a command decoder configured to receive a first activate command for activating the first memory cells, to receive a first deactivate command for deactivating the first memory cells, and to receive a second activate command for activating the second memory cells; and

a row decoder configured to activate the first word line corresponding to a first value of a row address received together with the first activate command, to deactivate the first word line depending on the first deactivate command, and to activate the third word line corresponding to a third, scrambled, value of the row address instead of the second word line corresponding to a second value of the row address, when the second value of the row address is received together with the second activate command.

15. The memory device of claim 14, wherein the row decoder is configured to scramble the first value of the row address received together with the first activate command and to scramble the second value of the row address received together with the second activate command, depending on a selection signal, and

wherein the first value of the row address received together with the first activate command is not changed by a scramble operation of the row decoder, and the second value of the row address received together with the second activate command is changed to the third value by the scramble operation of the row decoder.

16. The memory device of claim 15, further comprising:

an anti-fuse array including an anti-fuse in which a logical value of the selection signal is stored.

17. The memory device of any one of claims 14 to 16, wherein the memory cell array further includes:

fourth memory cells connected to at least one fourth word line interposed between the third word line and any one of the first and second word lines.

18. The memory device of any one of claims 14 to 17, wherein the memory cell array further includes:

bit line sense amplifiers interposed between the third word line and any one of the first and second word lines and configured to sense data stored in the first and second memory cells through bit lines.

19. The memory device of claim 18, wherein the bit line sense amplifiers do not sense data stored in the third memory cells.

20. The memory device of any one of claims 14 to 19, wherein the command decoder further receives a first refresh command and a second refresh command for refreshing the memory cell array, and

wherein the row decoder activates and deactivates the first word line depending on the first refresh command and activates and deactivates the third word line depending on the second refresh command.