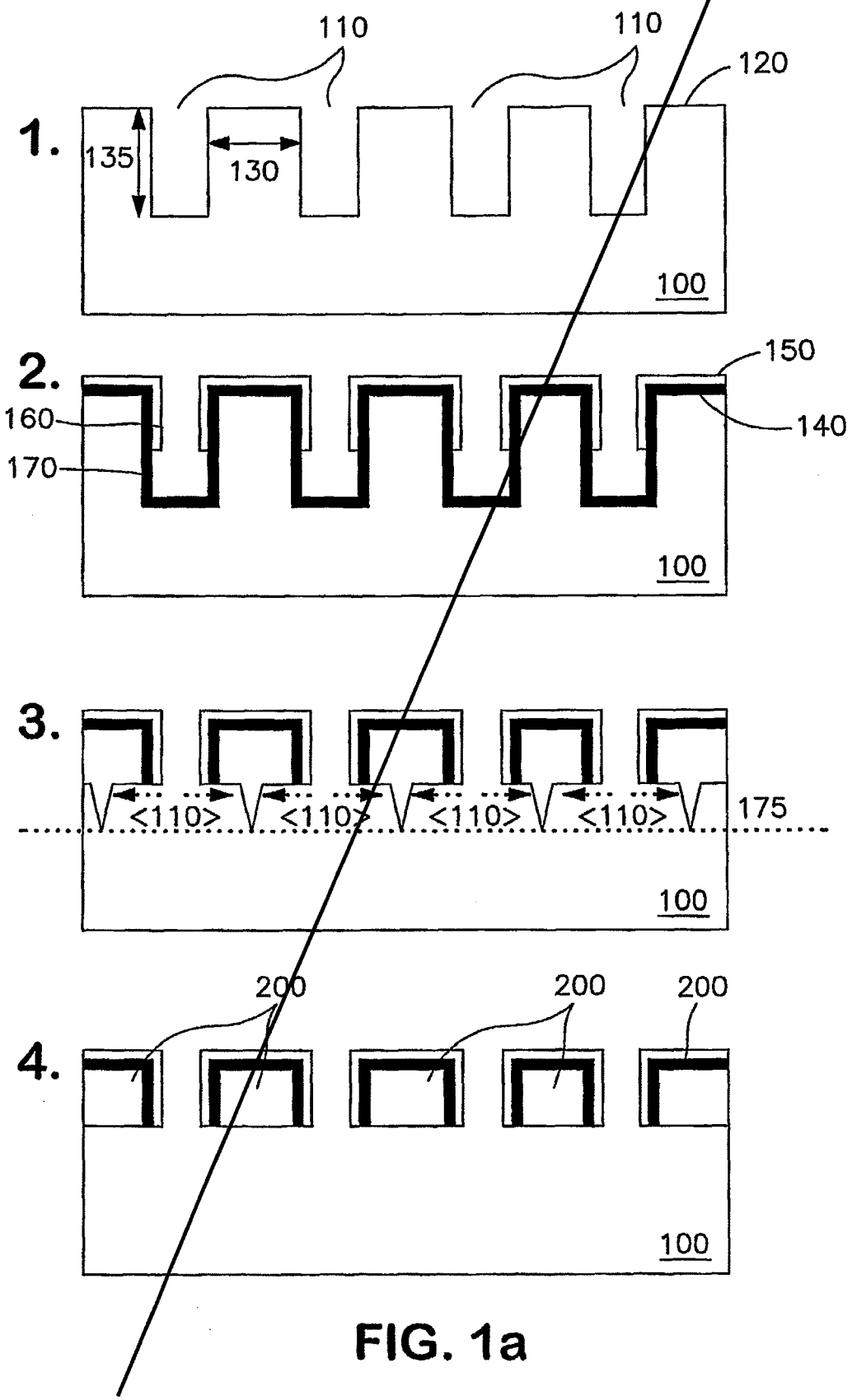

1.
110
110
120
135
130
100
2.
150
160
140
170
100
3.
<110>
<110>
<110>
<110>
175
100
4.
200
200
200
100

FIG. 1a

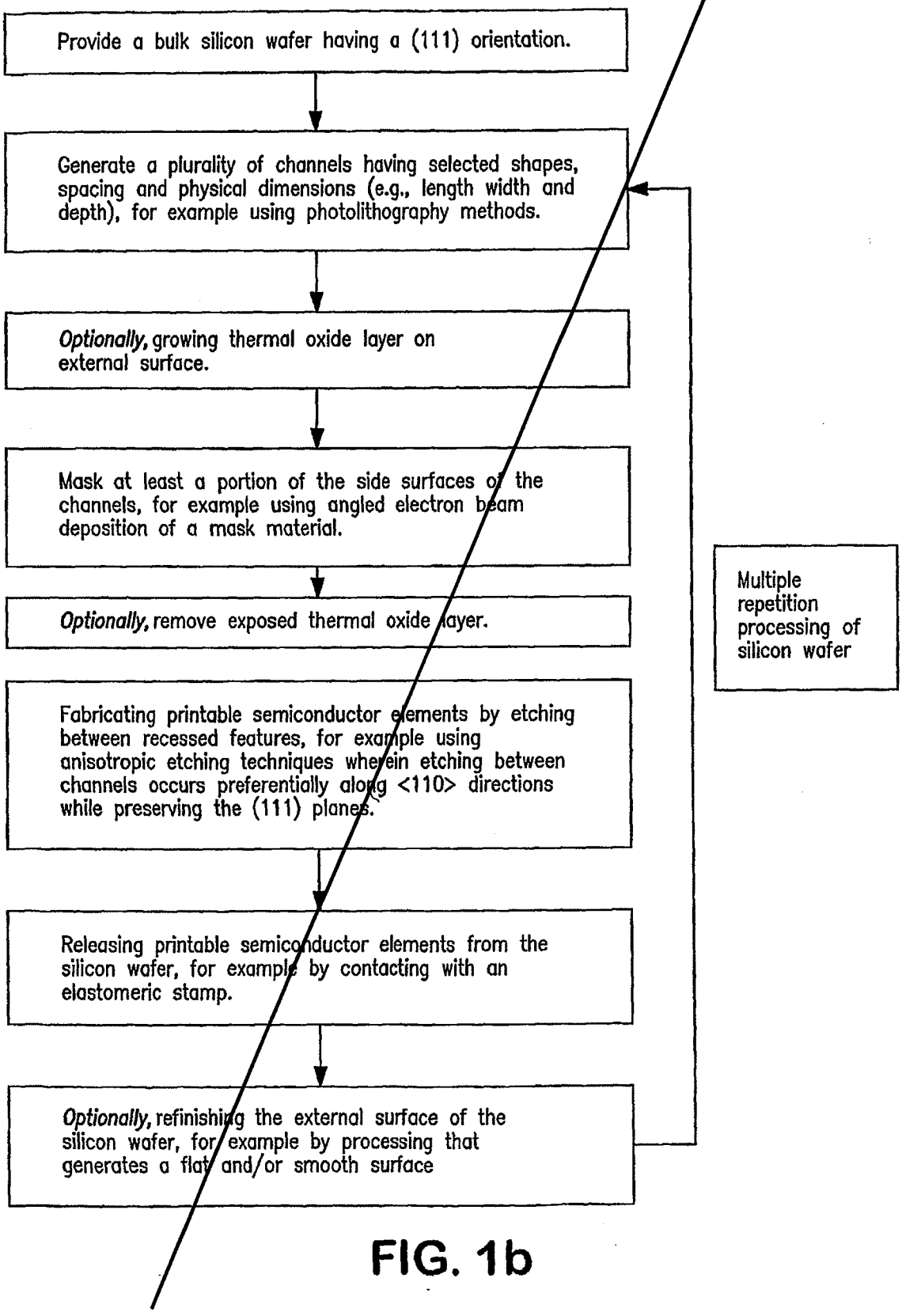

Provide a bulk silicon wafer having a (111) orientation.
Generate a plurality of channels having selected shapes, spacing and physical dimensions (e.g., length width and depth), for example using photolithography methods.
Optionally, growing thermal oxide layer on external surface.
Mask at least a portion of the side surfaces of the channels, for example using angled electron beam deposition of a mask material.
Optionally, remove exposed thermal oxide layer.
Fabricating printable semiconductor elements by etching between recessed features, for example using anisotropic etching techniques wherein etching between channels occurs preferentially along <110> directions while preserving the (111) planes.
Releasing printable semiconductor elements from the silicon wafer, for example by contacting with an elastomeric stamp.
Optionally, refinishing the external surface of the silicon wafer, for example by processing that generates a flat and/or smooth surface
Multiple repetition processing of silicon wafer

FIG. 1b

FIG. 1c

FIG. 1d

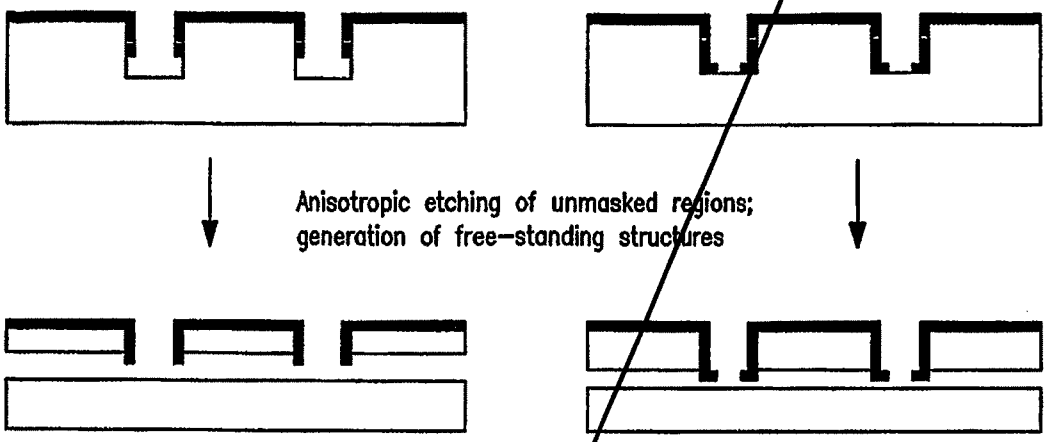


FIG. 1e

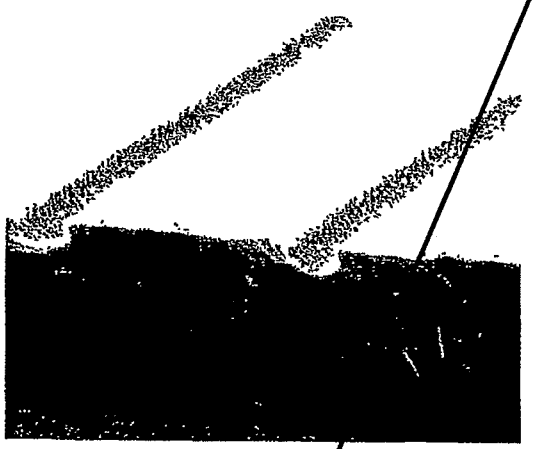
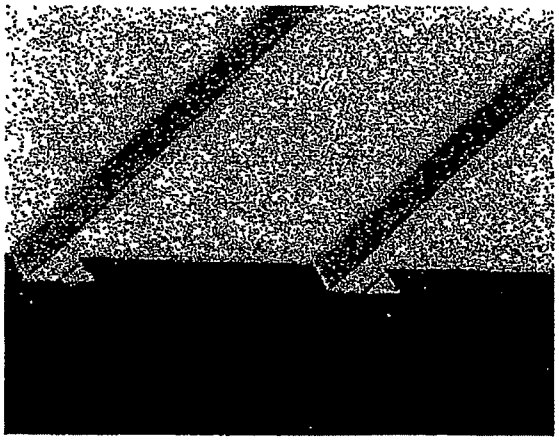


FIG. 1f



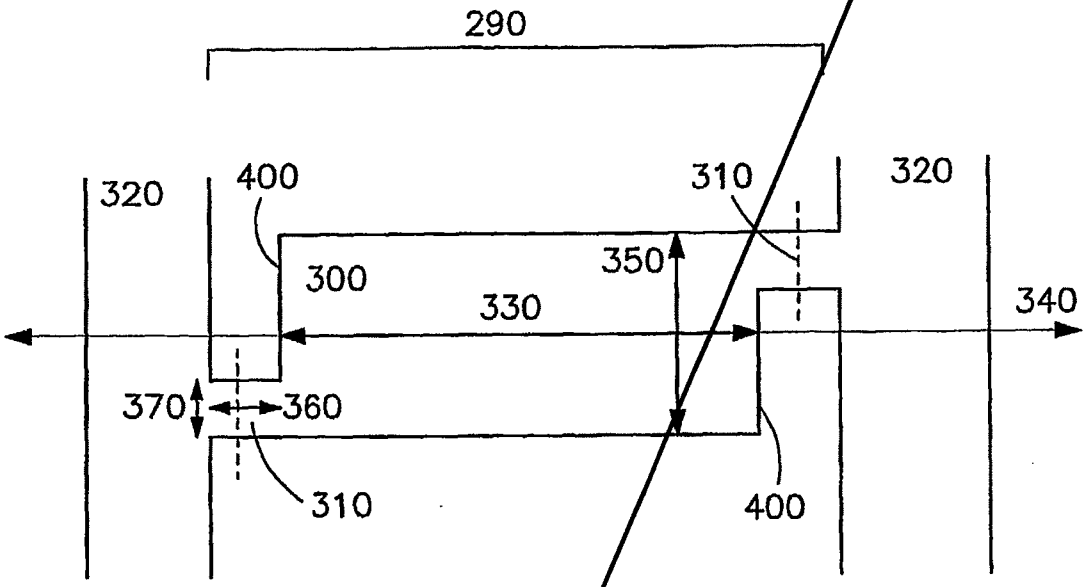

290
320
400
310
320
300
350
330
340
370
360
310
400

FIG. 2a

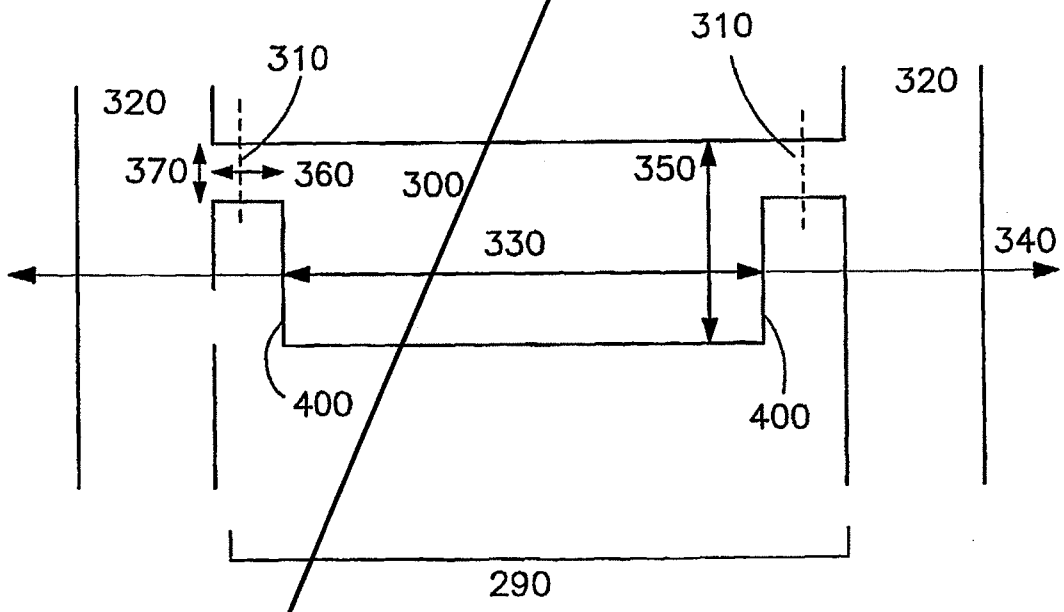

310
310
320
320
370
360
300
350
330
340
400
400
290

FIG. 2b

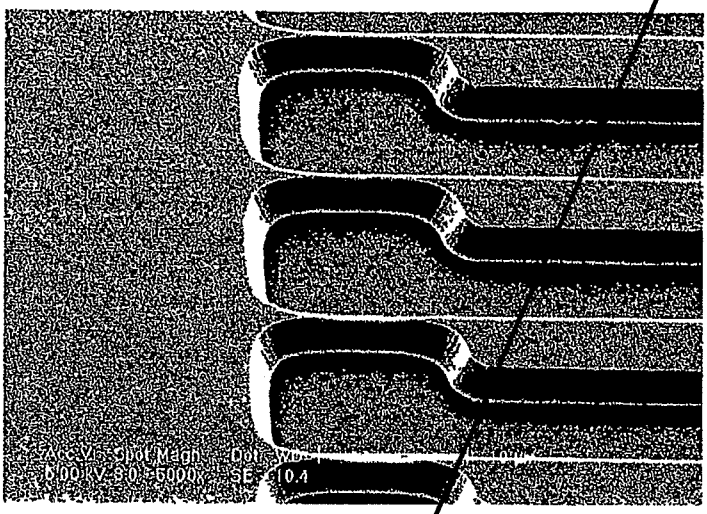


FIG. 2c

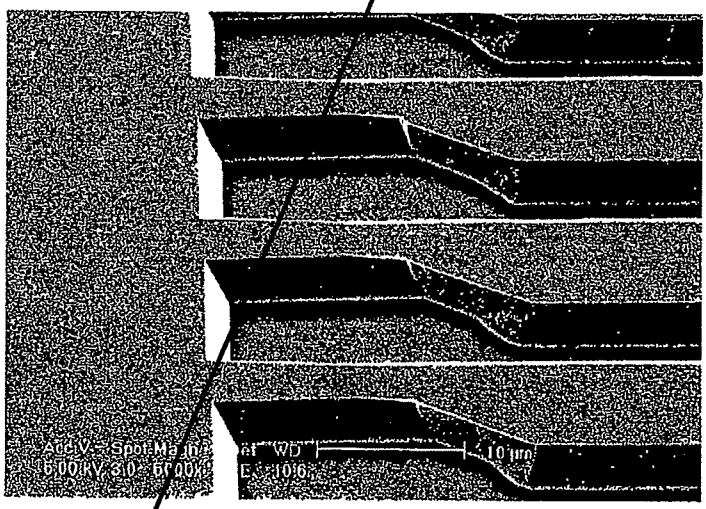


FIG. 2d

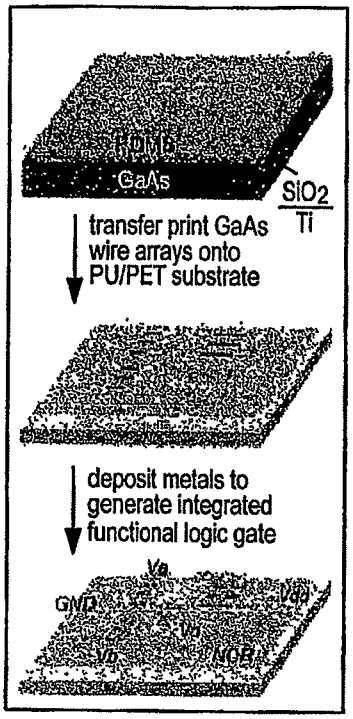


FIG. 3a

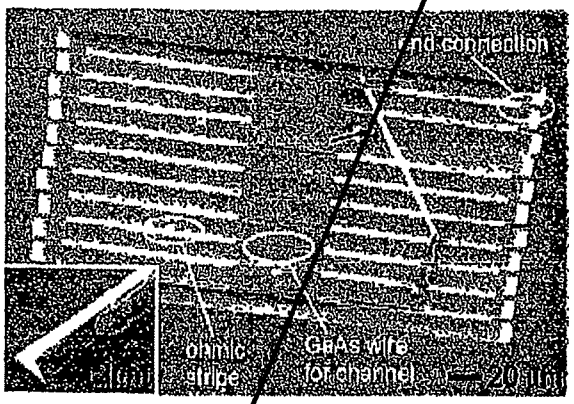


FIG. 3b

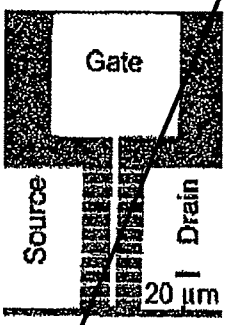


FIG. 3c

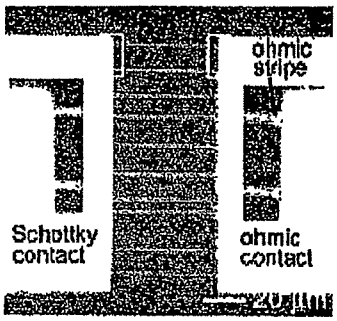


FIG. 3d

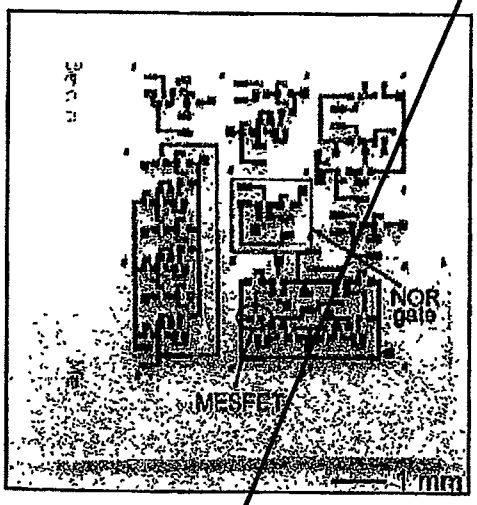


FIG. 3e

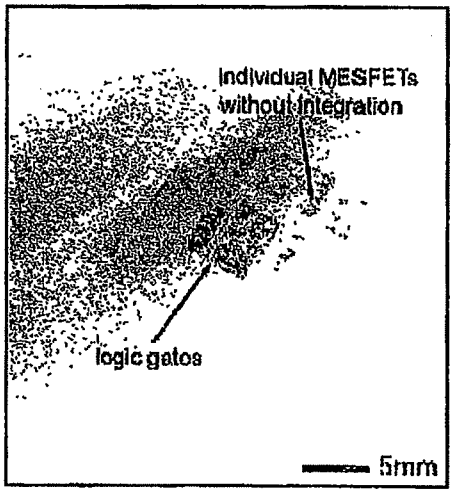


FIG. 3f

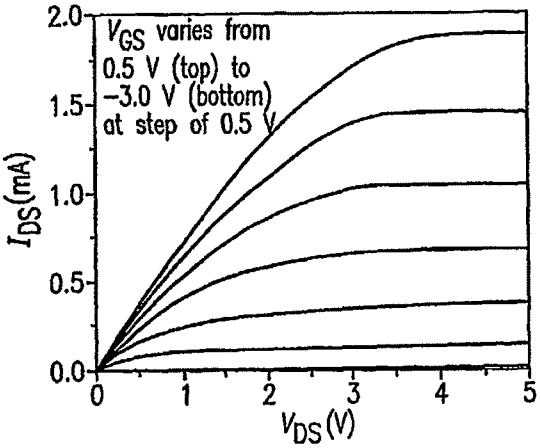


FIG. 4a

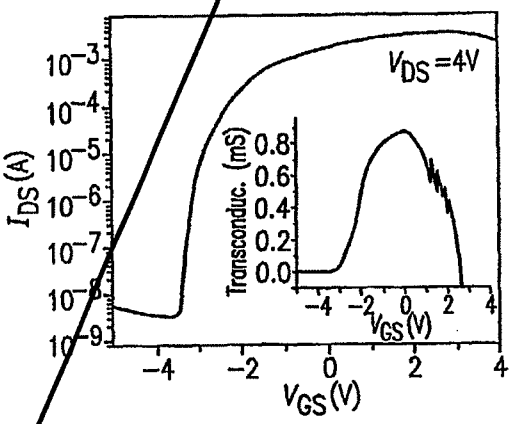


FIG. 4b

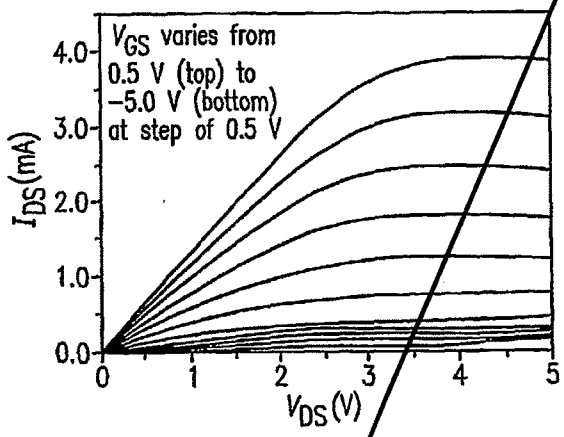


FIG. 4c

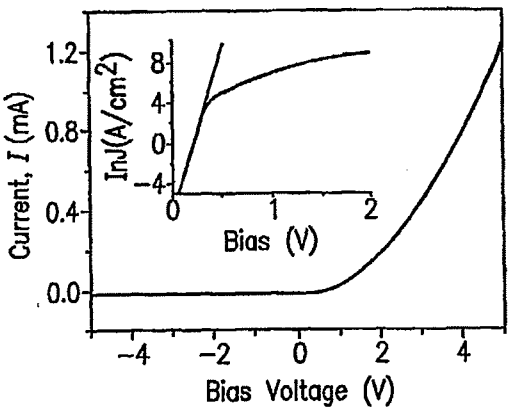


FIG. 4d

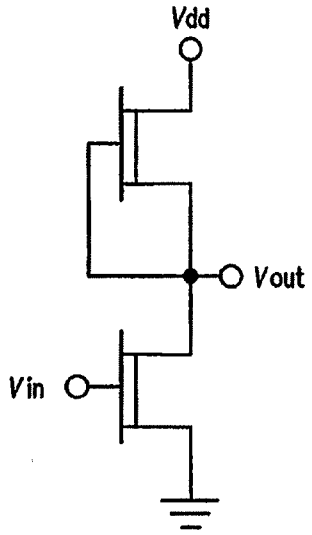


FIG. 5a

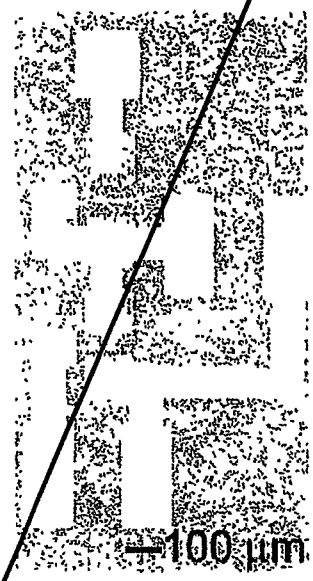


FIG. 5b

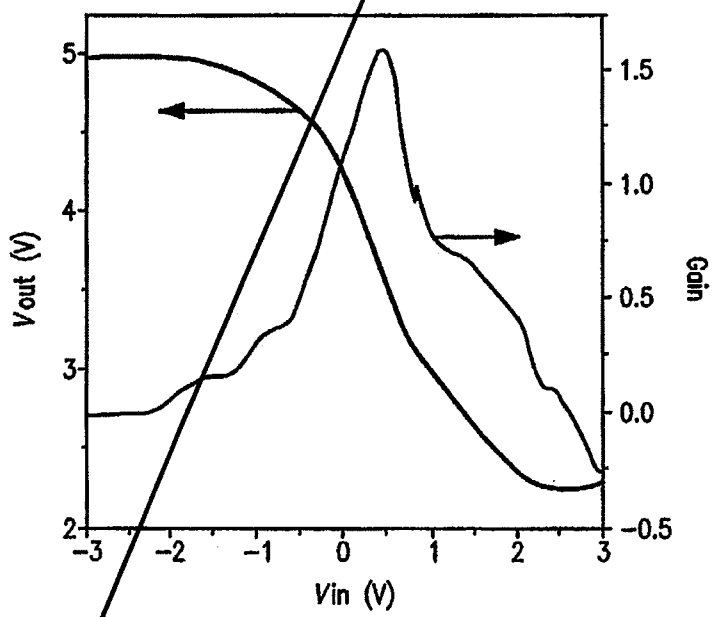


FIG. 5c

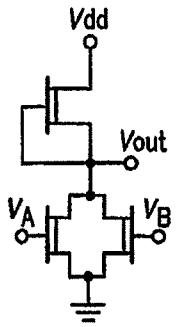


FIG. 6a

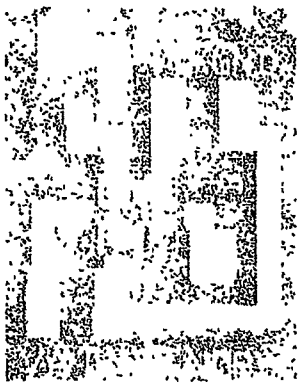


FIG. 6b

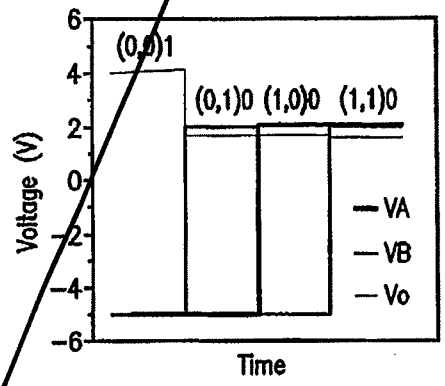


FIG. 6c

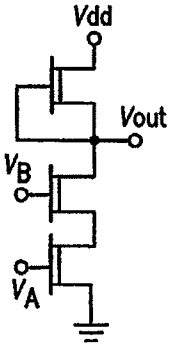


FIG. 6d

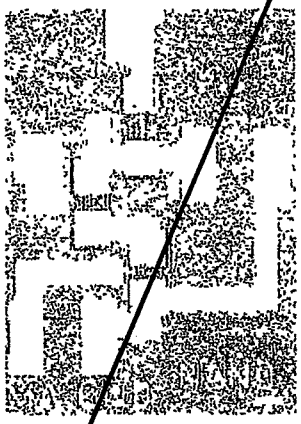


FIG. 6e

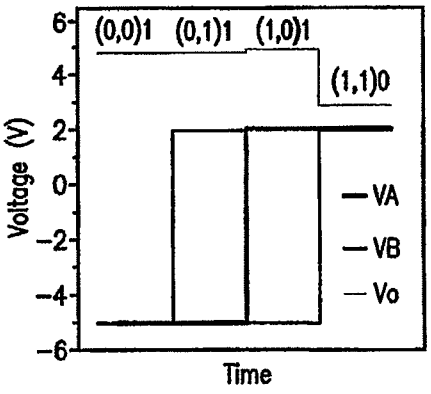


FIG. 6f

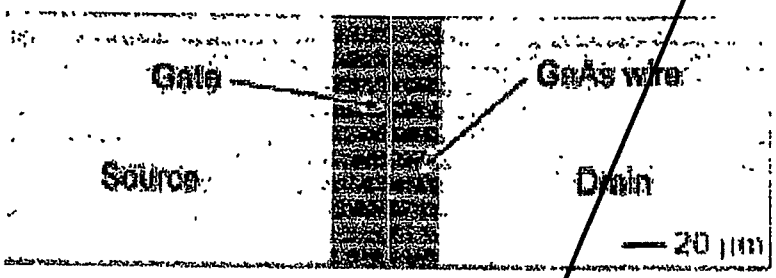

Gate
GaAs wire
Source
Drain
20 μm

FIG. 7a

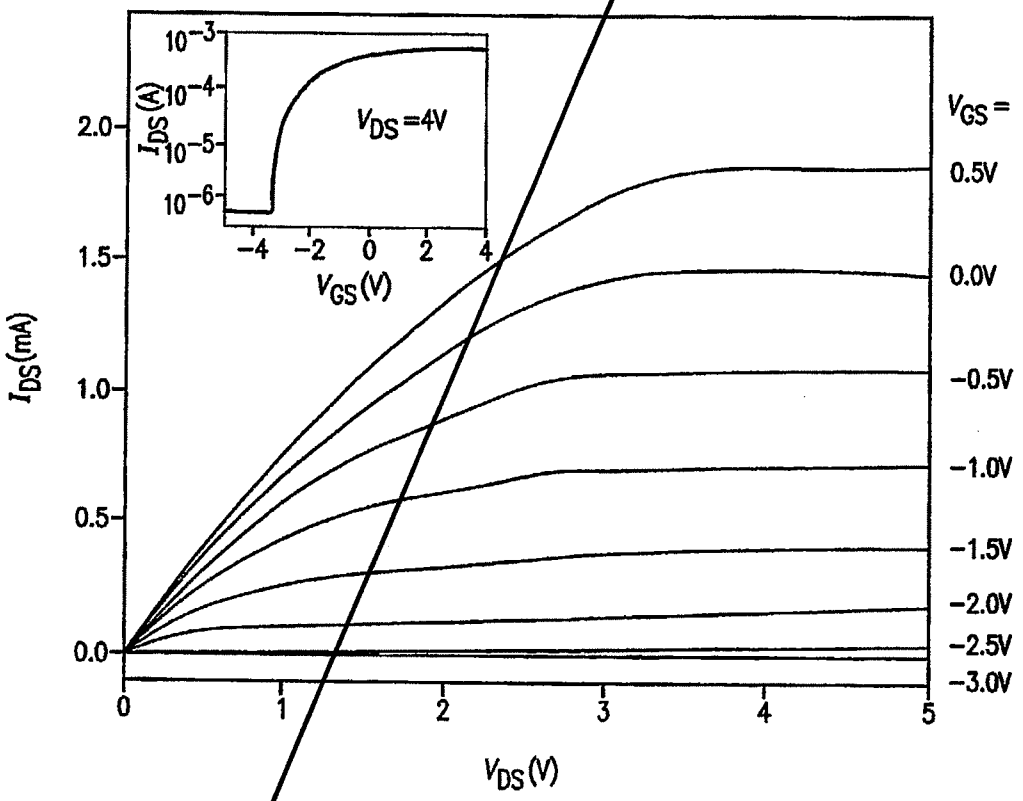

I_{DS}(mA)
2.0
1.5
1.0
0.5
0.0
0
1
2
3
4
5
V_{DS}(V)
V_{GS} =
0.5V
0.0V
−0.5V
−1.0V
−1.5V
−2.0V
−2.5V
−3.0V
I_{DS}(A)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
V_{DS}=4V
−4
−2
0
2
4
V_{GS}(V)

FIG. 7b

FIG. 8a

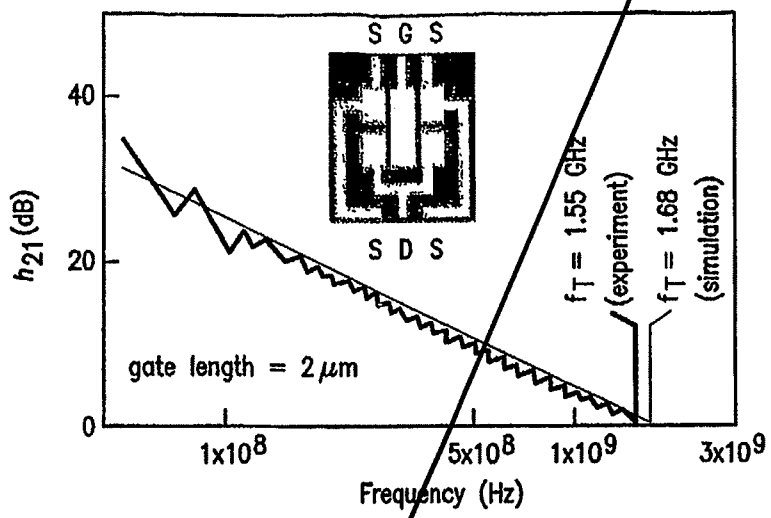


FIG. 8b

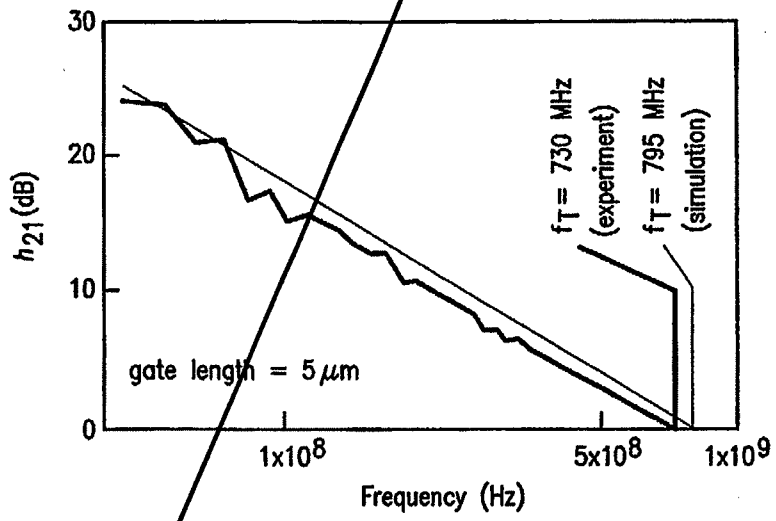


FIG. 8c

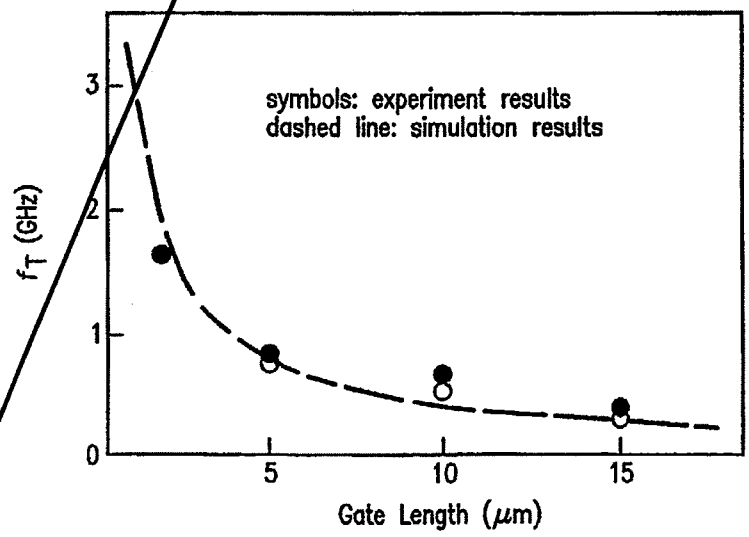


FIG. 9a

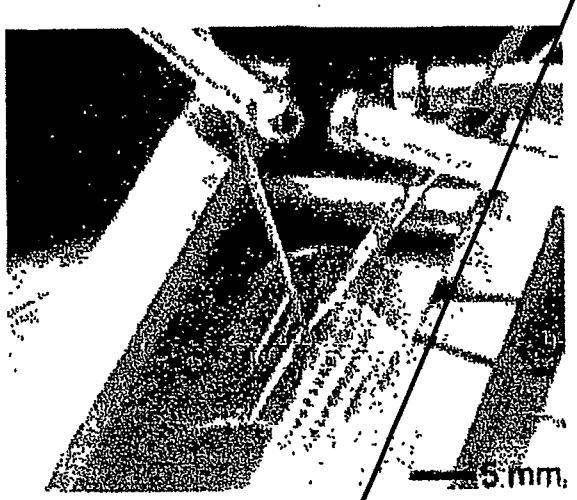


FIG. 9b

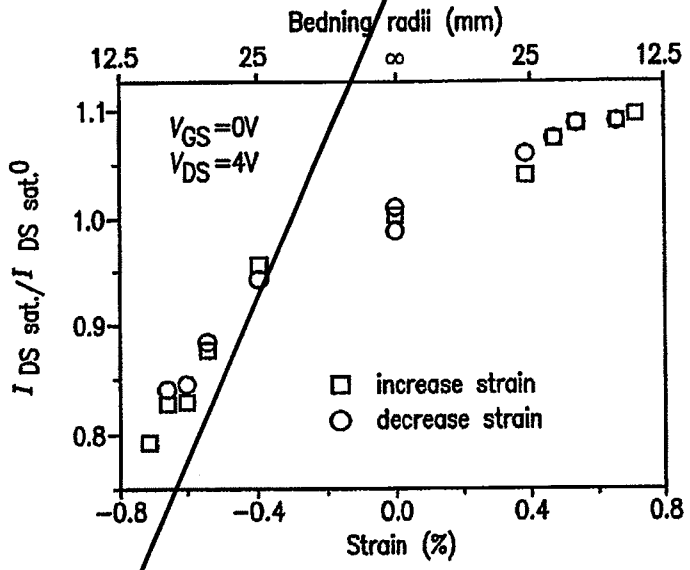


FIG. 9c

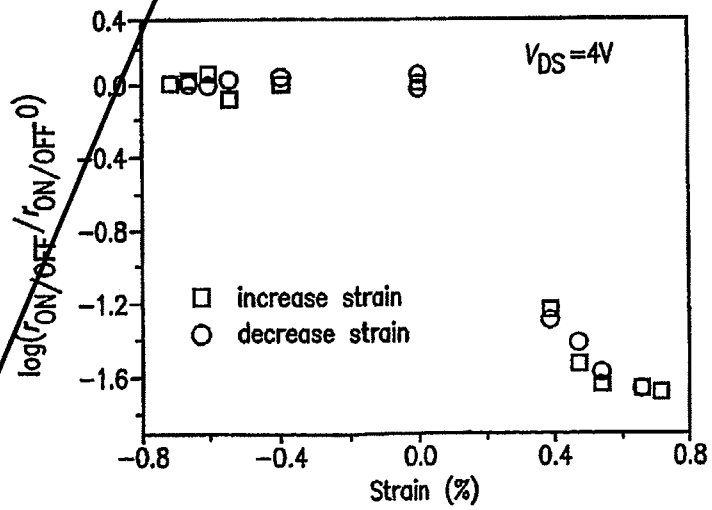


FIG. 10a

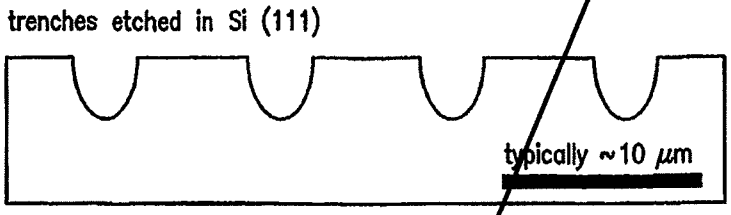


FIG. 10b

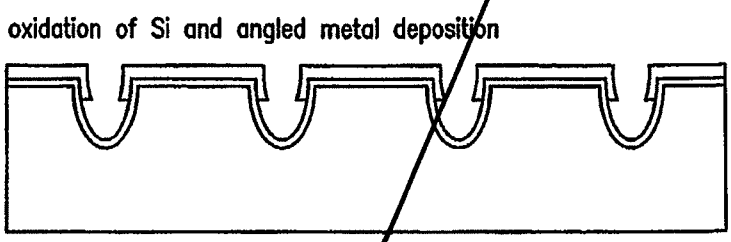


FIG. 10c

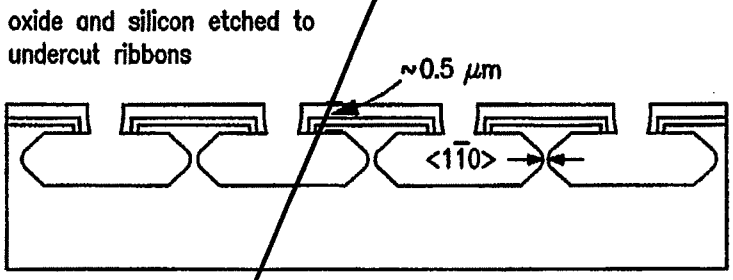


FIG. 10d

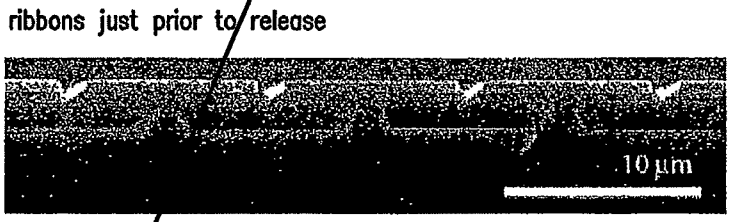


FIG. 10e



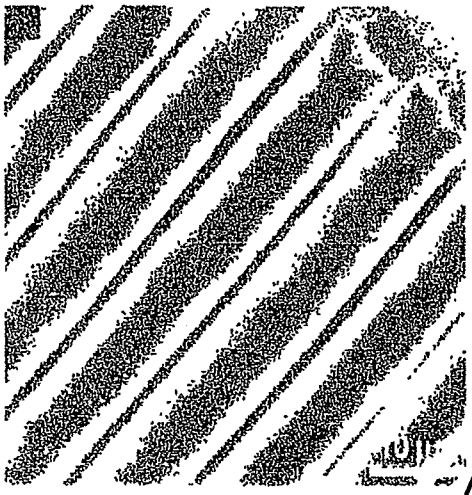


FIG. 11a

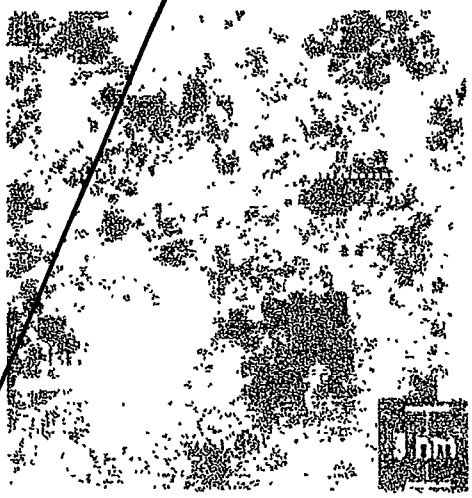


FIG. 11b

apply stamp to donor substrate

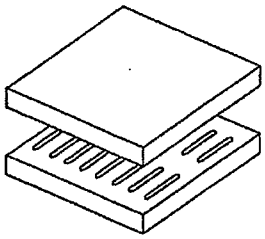


FIG. 12a

retrieve ribbons

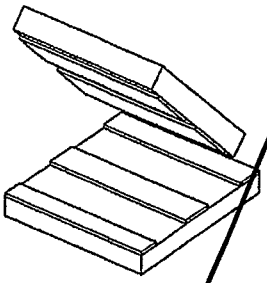


FIG. 12b

print ribbons onto plastic sheet

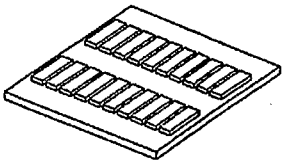


FIG. 12c



FIG. 12d



FIG. 12e



FIG. 12f

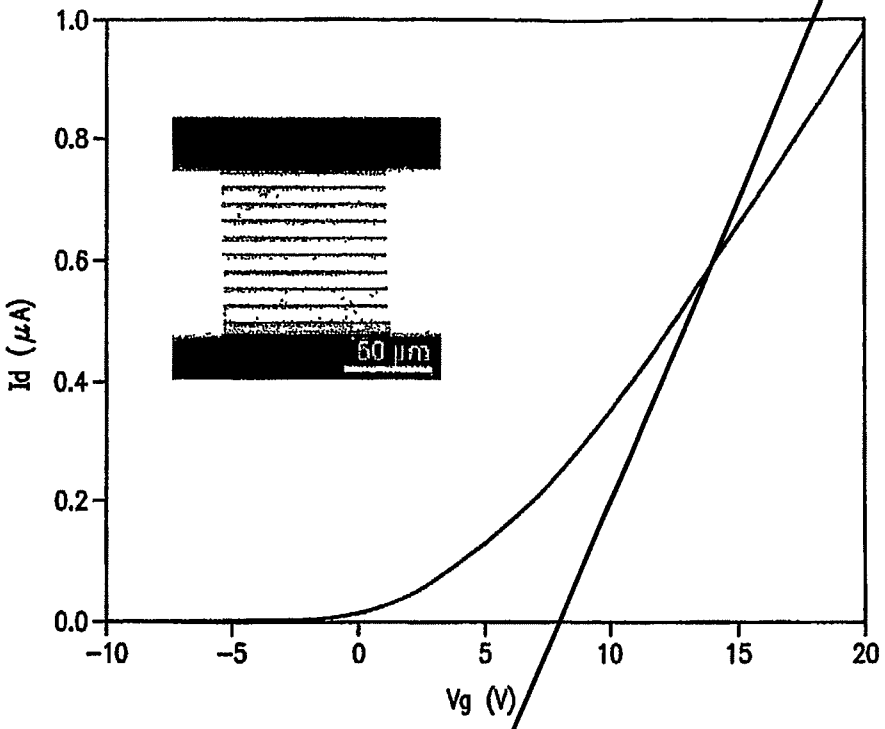


FIG. 13a

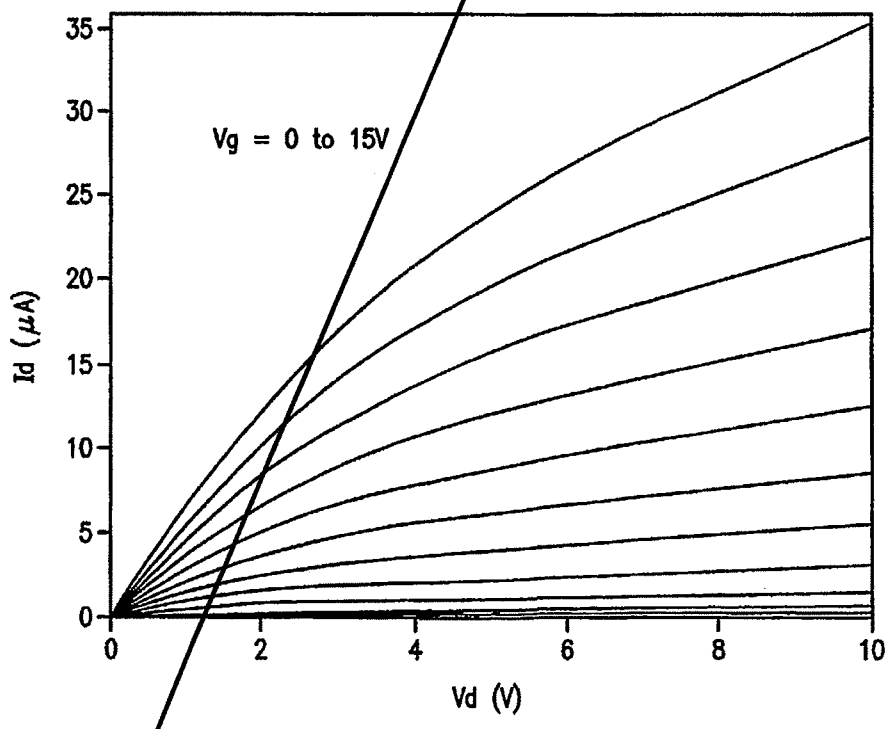


FIG. 13b

FIG. 14a

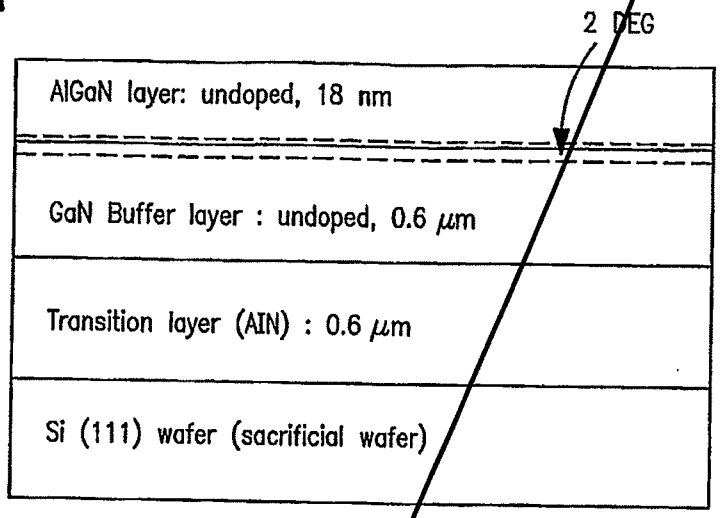


FIG. 14b

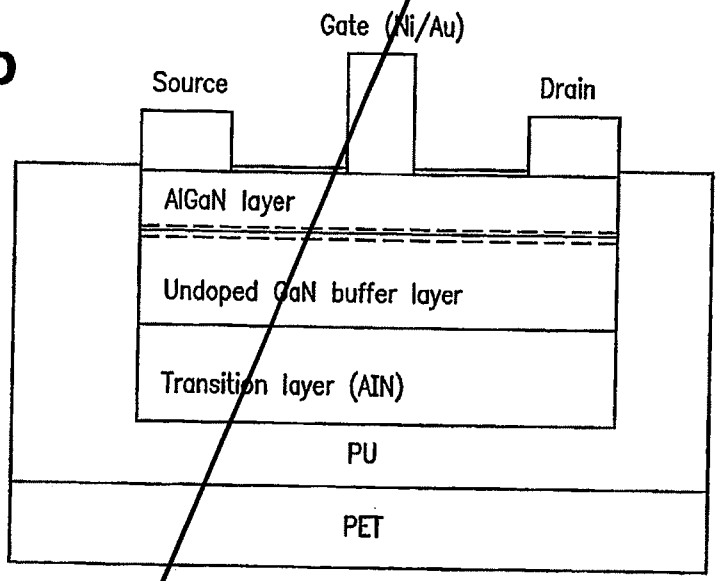
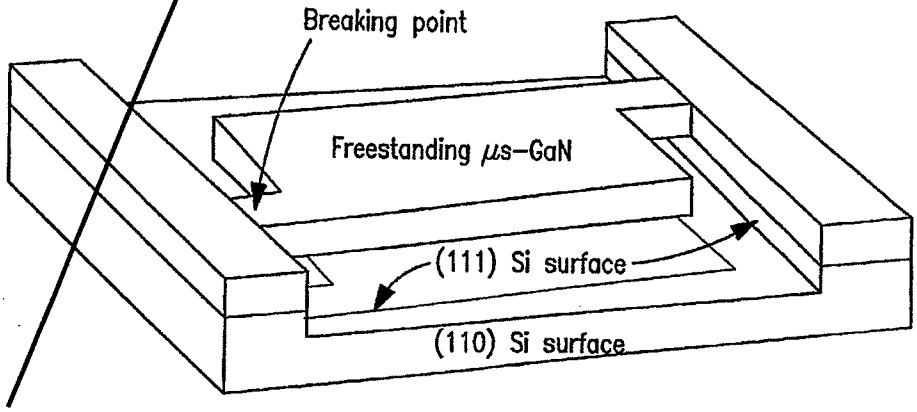


FIG. 14c



Ohmic contact on GaN stack

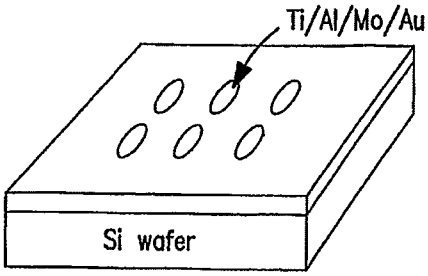


FIG. 15a

Ribbon pattern with PEO/Cr

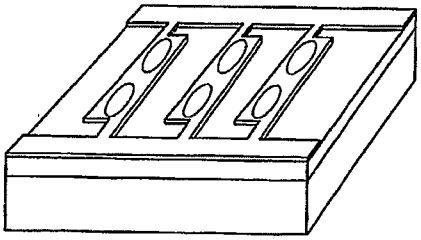


FIG. 15b

ICP etching of GaN

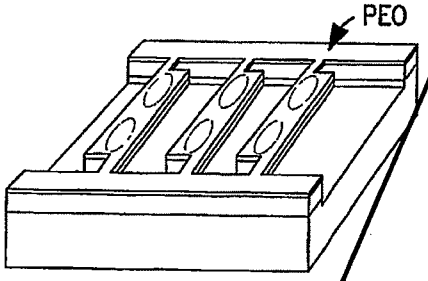


FIG. 15c

TMAH etching of underlying Si

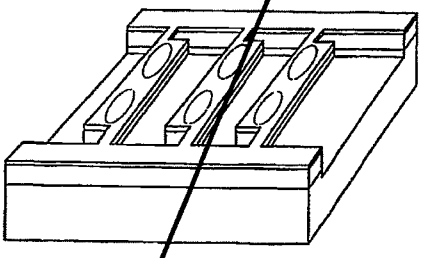


FIG. 15d

Transfer to PDMS

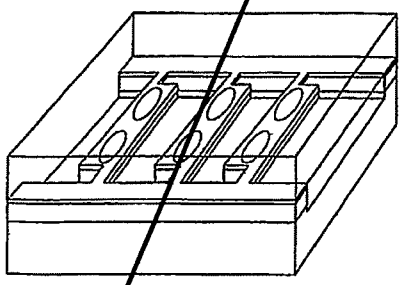


FIG. 15e

Spincast PU on plastic

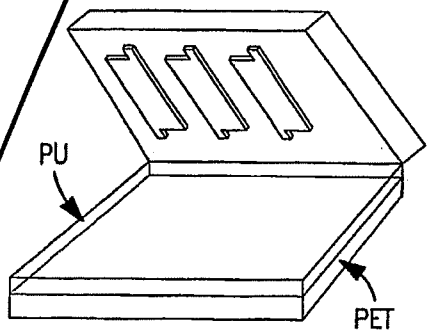


FIG. 15f

Contact PDMS to PET

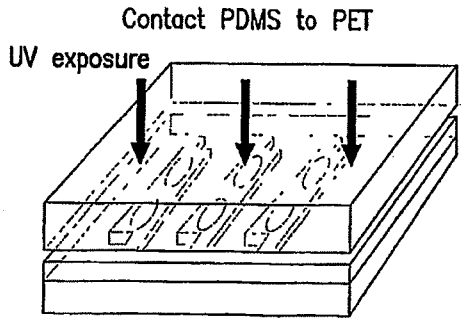


FIG. 15g

Removing oxide & metal contact

Gate (Schottky contact, Ni/Au)

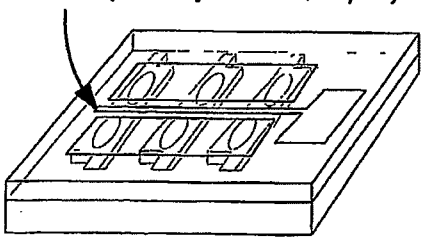


FIG. 15h

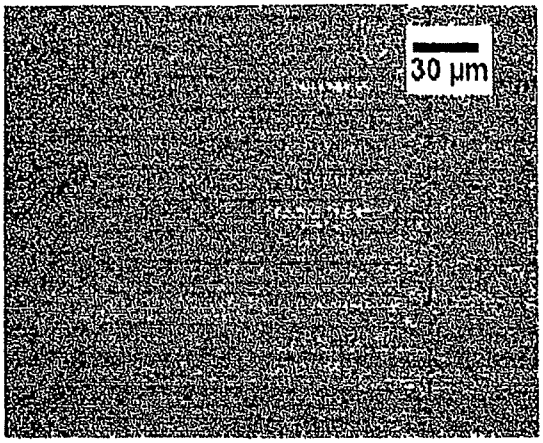


FIG. 16a

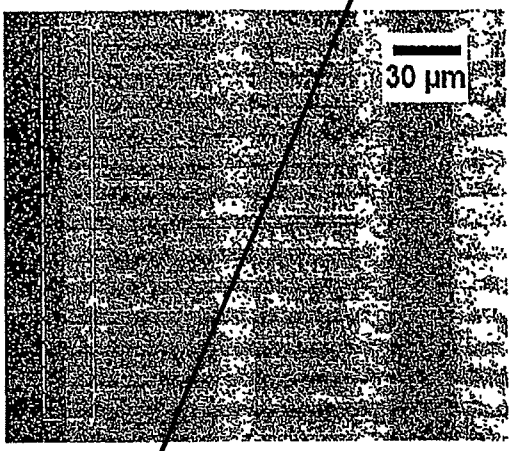


FIG. 16b

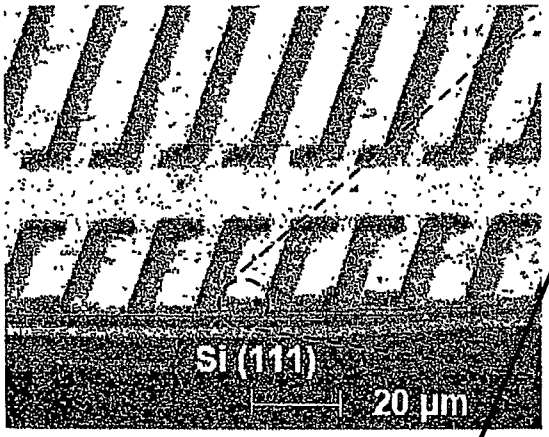


FIG. 16c

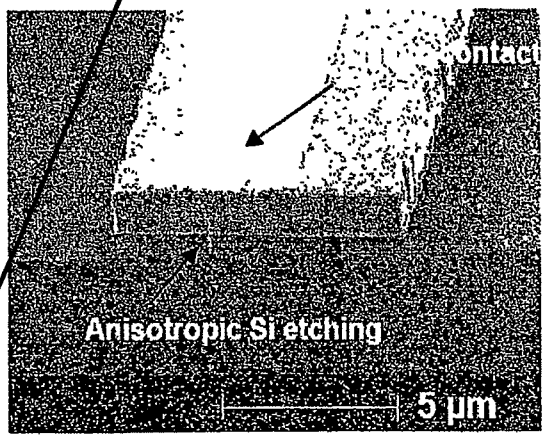


FIG. 16d

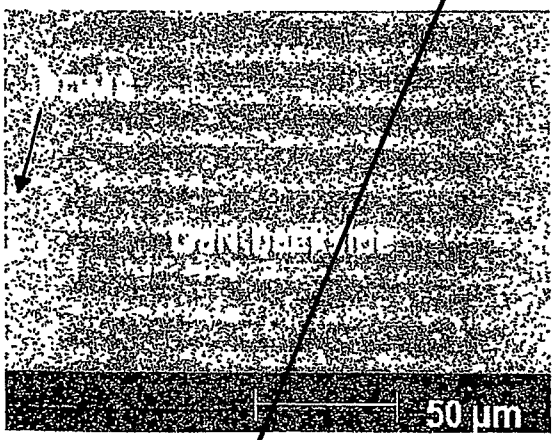


FIG. 16e

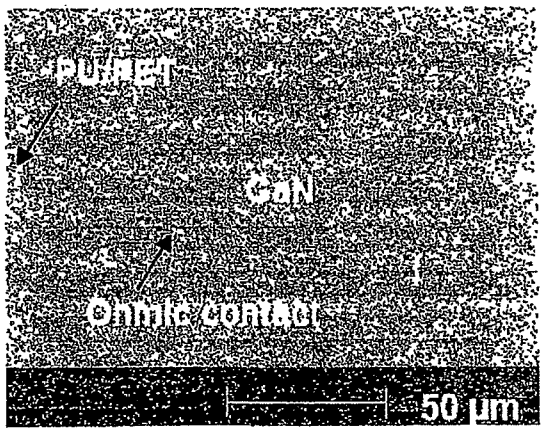


FIG. 16f

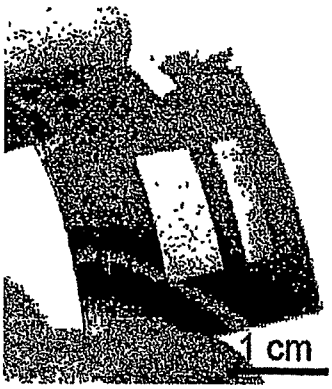


FIG. 17a

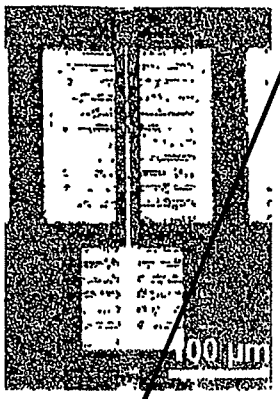


FIG. 17b

FIG. 17c

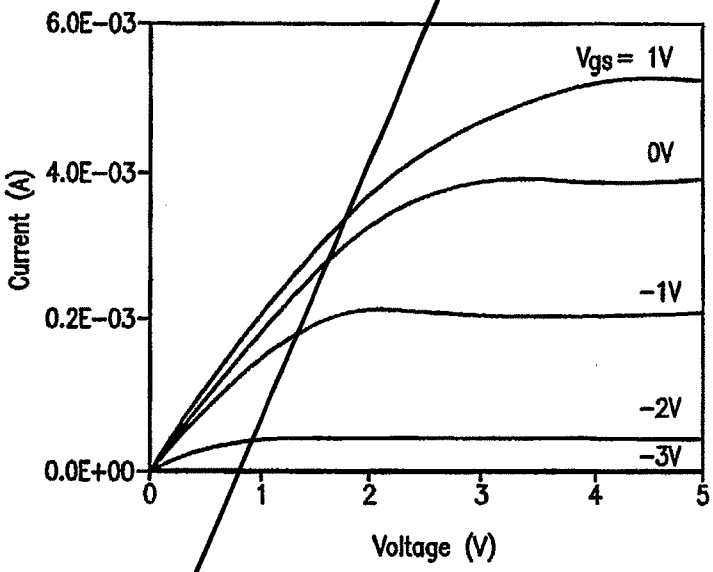


FIG. 17d

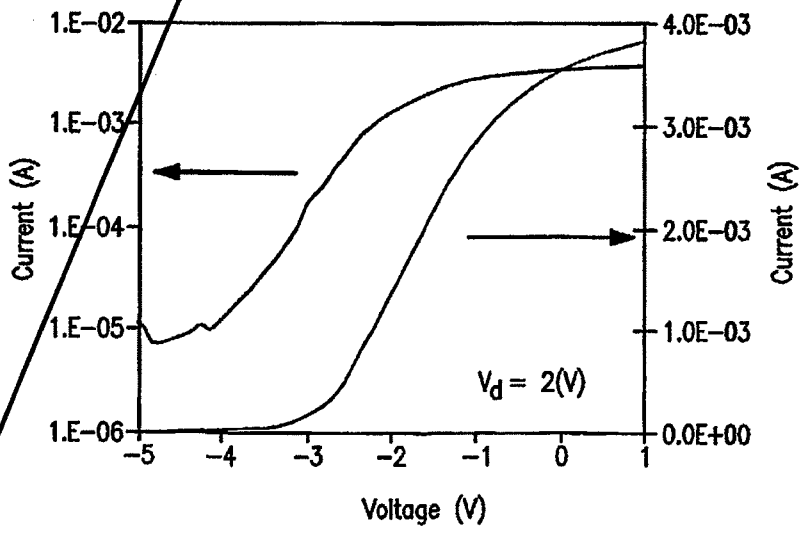


FIG. 18a

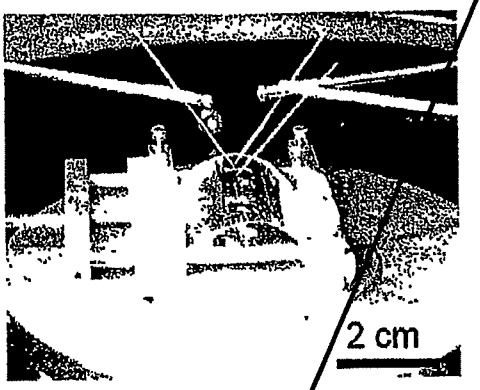


FIG. 18b

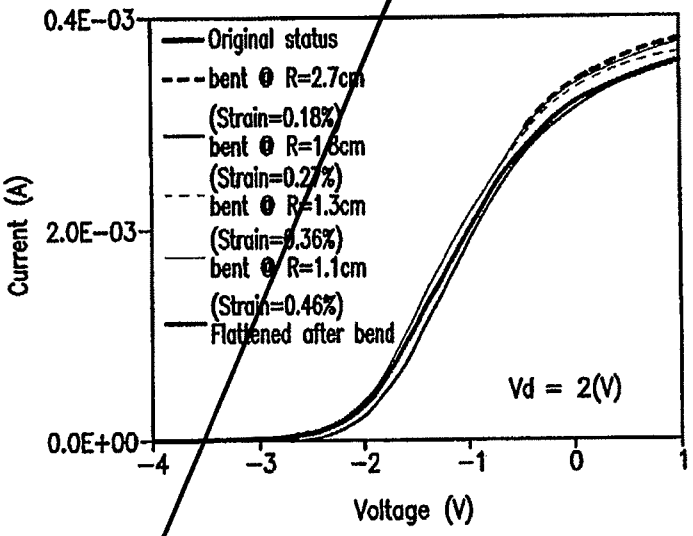
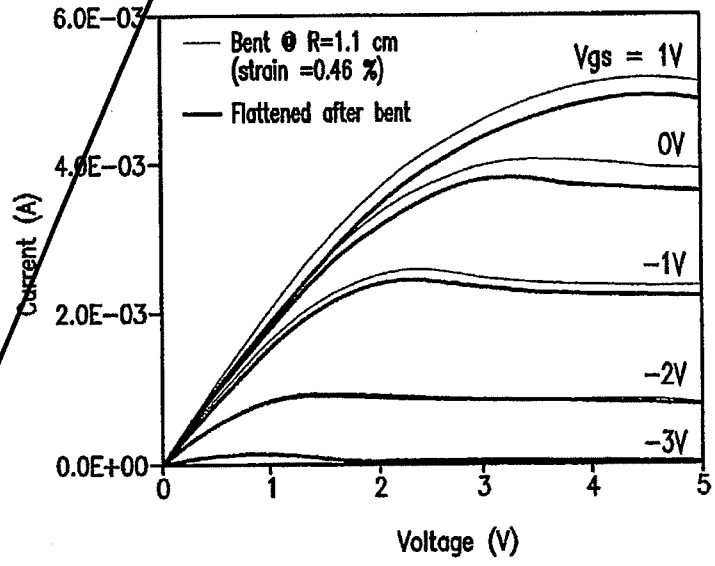


FIG. 18c



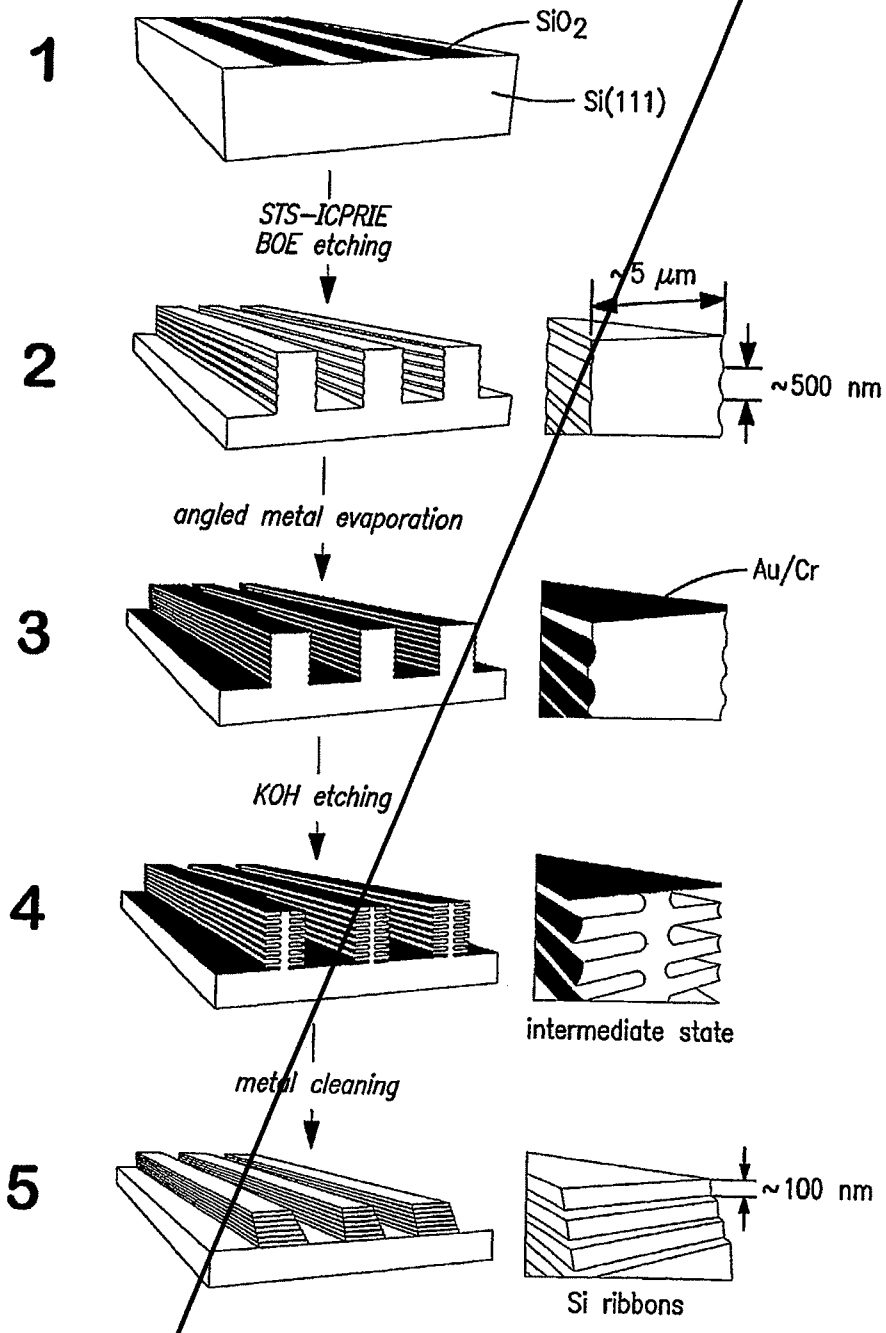

1
SiO_2
Si(111)
STS–ICPRIE
BOE etching
2
~5 μm
~500 nm
angled metal evaporation
3
Au/Cr
KOH etching
4
intermediate state
metal cleaning
5
~100 nm
Si ribbons

FIG. 19

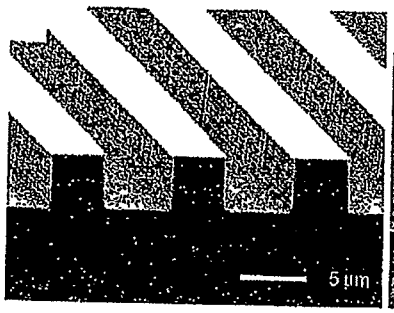


FIG. 20a

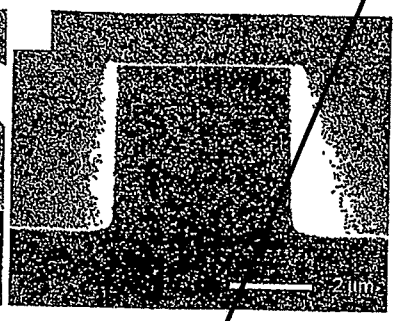


FIG. 20b

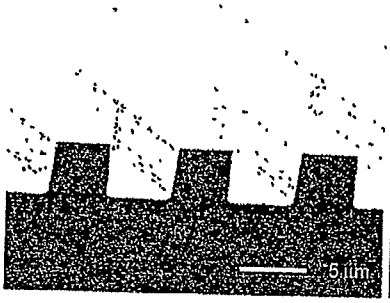


FIG. 20c

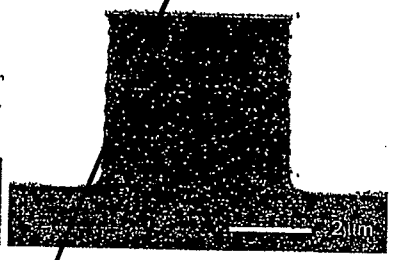


FIG. 20d

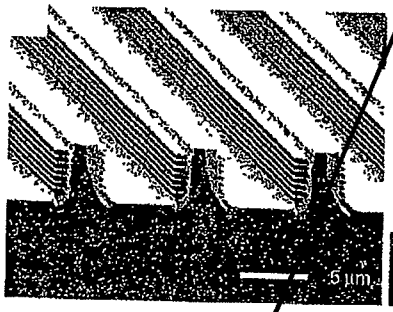


FIG. 20e

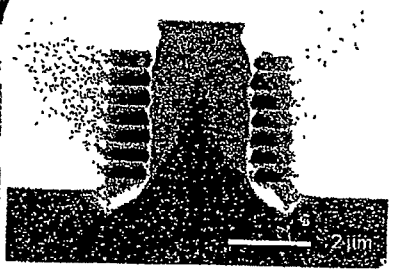


FIG. 20f

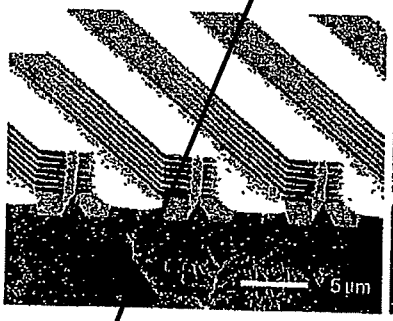


FIG. 20g

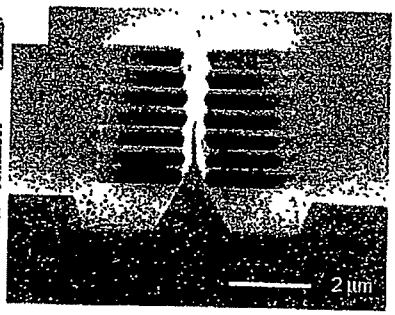


FIG. 20h

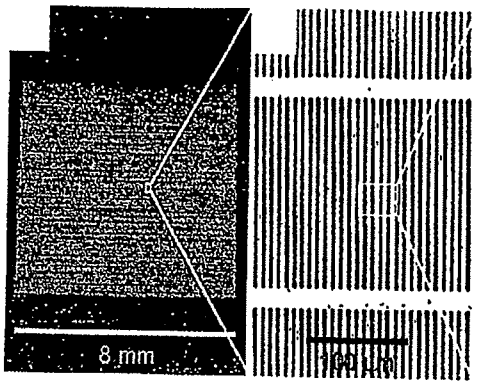


FIG. 21a FIG. 21b

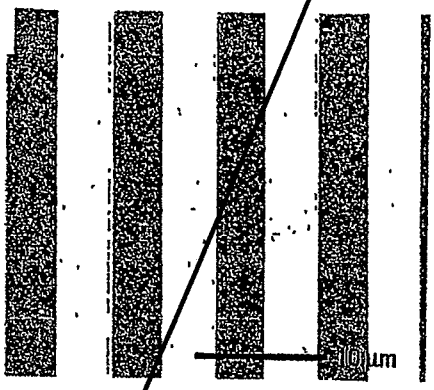


FIG. 21c

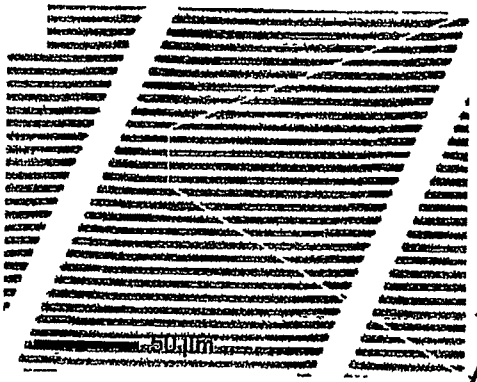


FIG. 21d

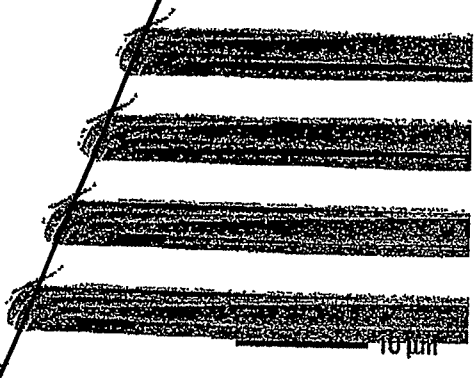


FIG. 21e



FIG. 22a

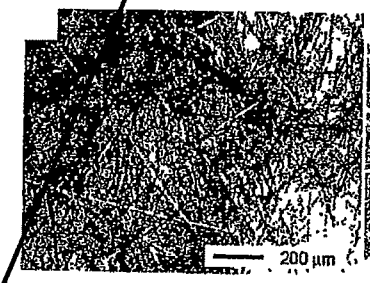


FIG. 22b

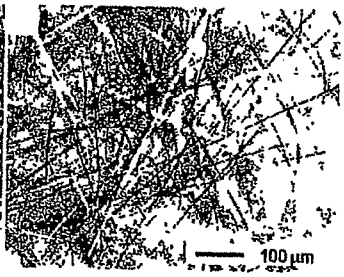


FIG. 22c

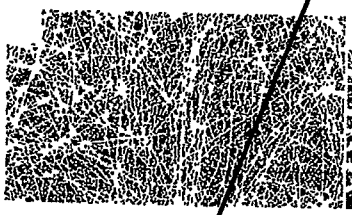


FIG. 22d

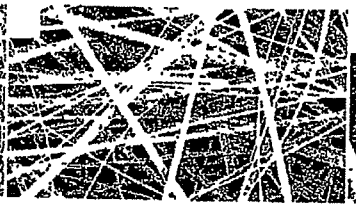


FIG. 22e



FIG. 22f

FIG. 23a

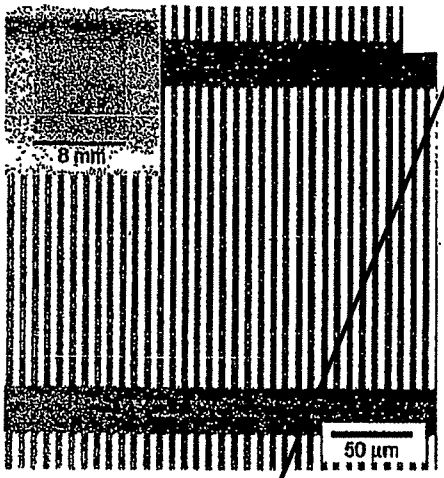


FIG. 23b

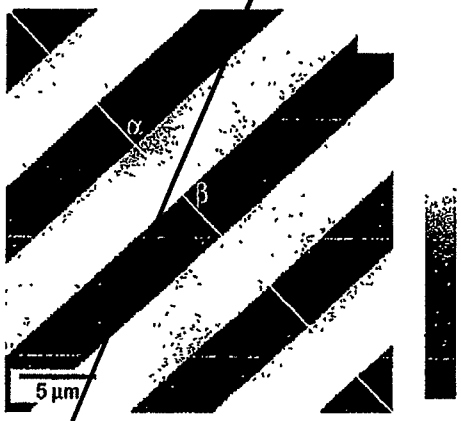


FIG. 23c

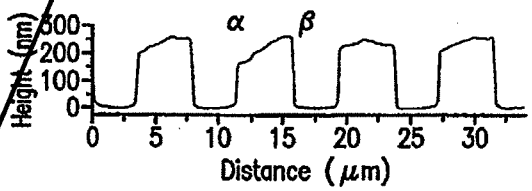


FIG. 23d



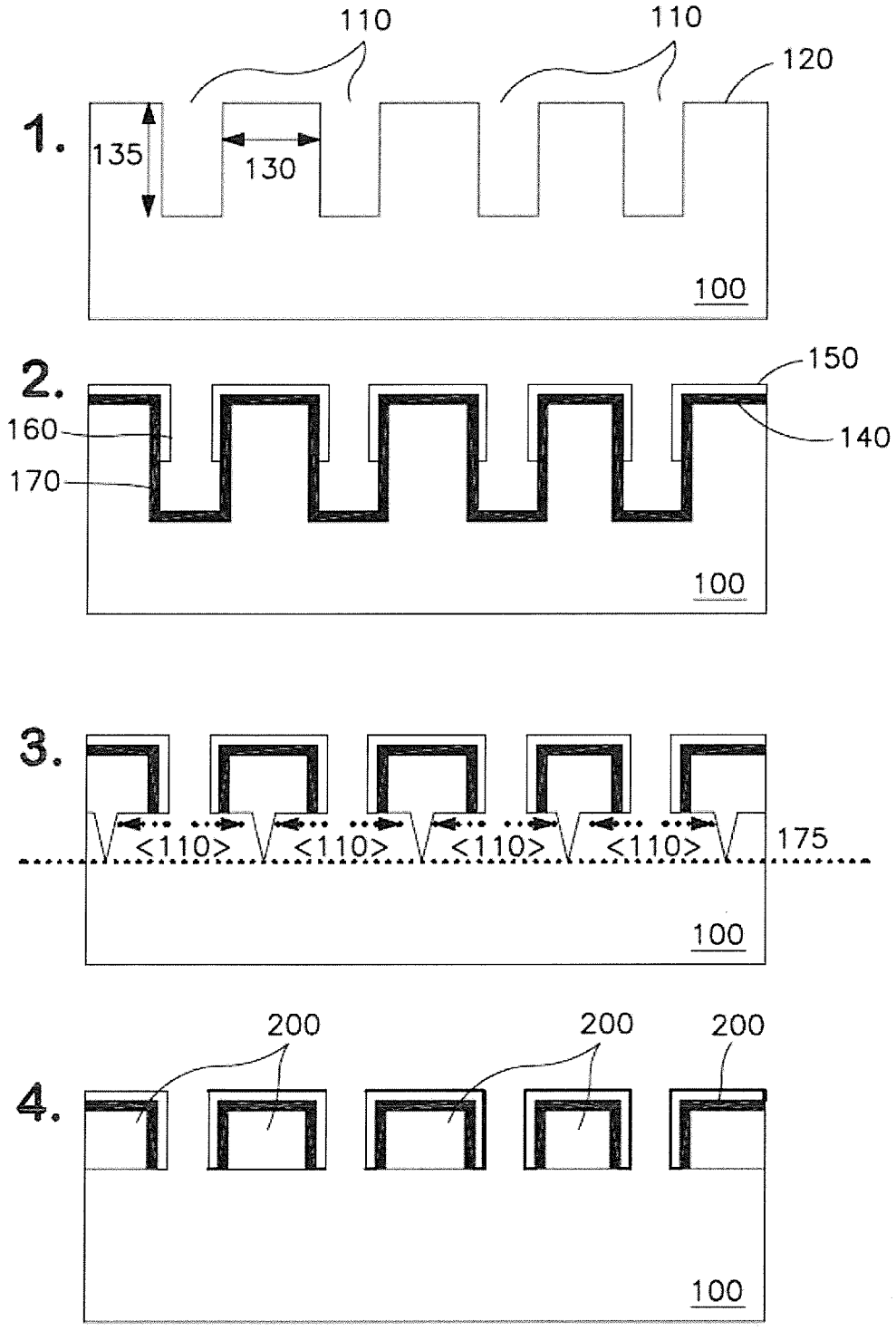

1.
110
110
120
135
130
100
2.
150
160
140
170
100
3.
<110>
<110>
<110>
<110>
175
100
4.
200
200
200
100

FIG. 1a

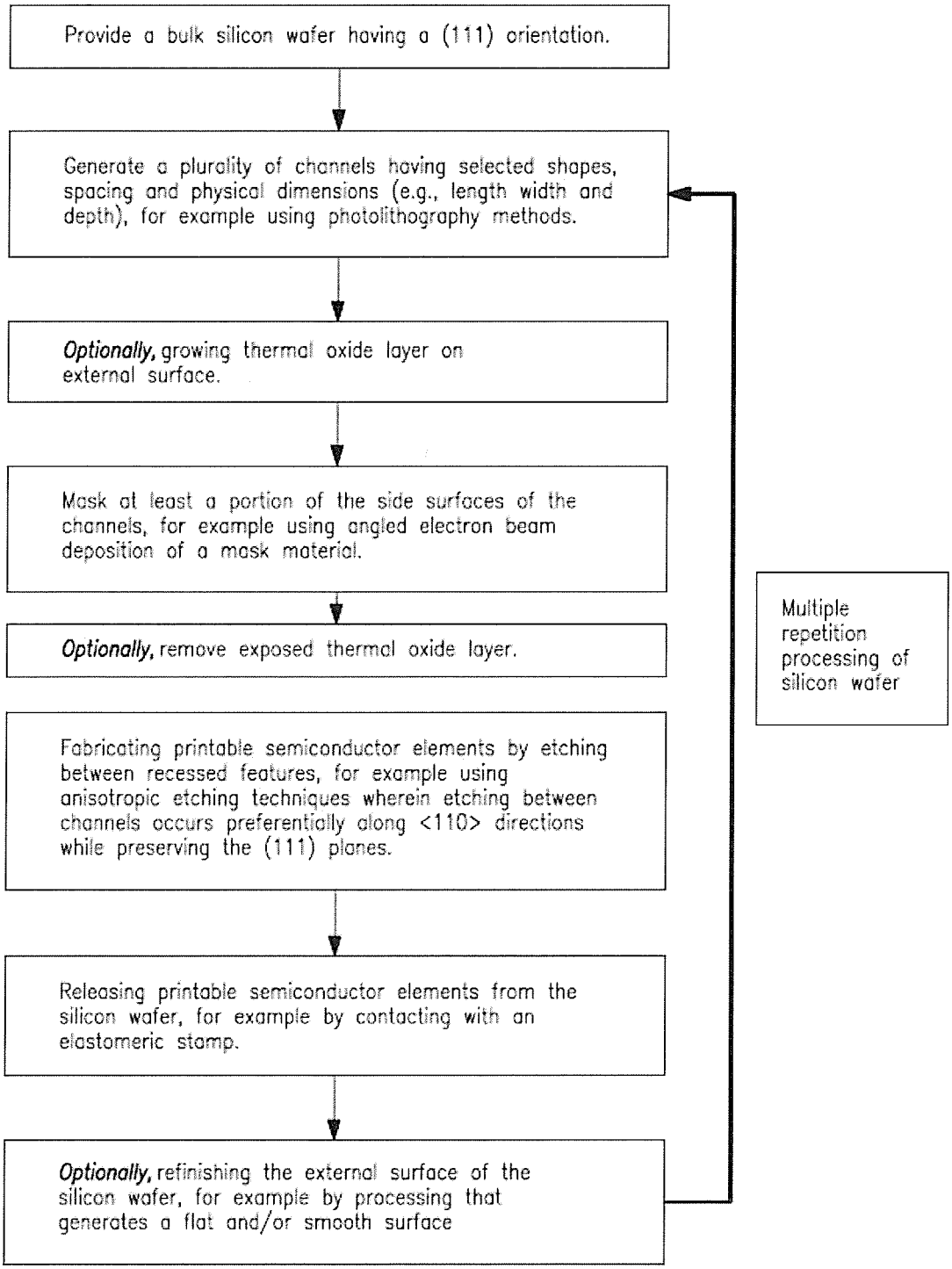

Provide a bulk silicon wafer having a (111) orientation.
Generate a plurality of channels having selected shapes, spacing and physical dimensions (e.g., length width and depth), for example using photolithography methods.
Optionally, growing thermal oxide layer on external surface.
Mask at least a portion of the side surfaces of the channels, for example using angled electron beam deposition of a mask material.
Optionally, remove exposed thermal oxide layer.
Fabricating printable semiconductor elements by etching between recessed features, for example using anisotropic etching techniques wherein etching between channels occurs preferentially along <110> directions while preserving the (111) planes.
Releasing printable semiconductor elements from the silicon wafer, for example by contacting with an elastomeric stamp.
Optionally, refinishing the external surface of the silicon wafer, for example by processing that generates a flat and/or smooth surface
Multiple repetition processing of silicon wafer

FIG. 1b

FIG. 1c

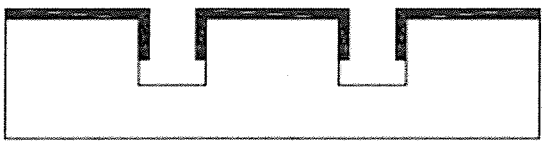
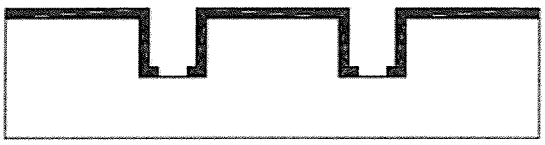


FIG. 1d



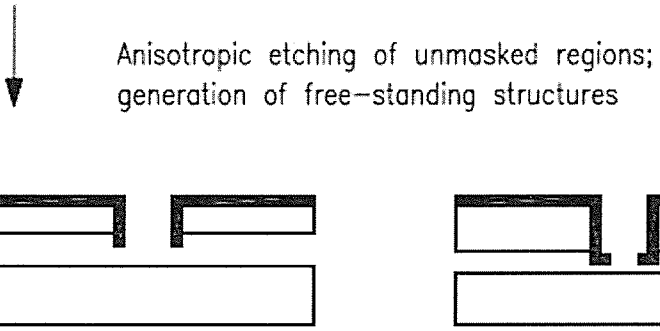


FIG. 1e

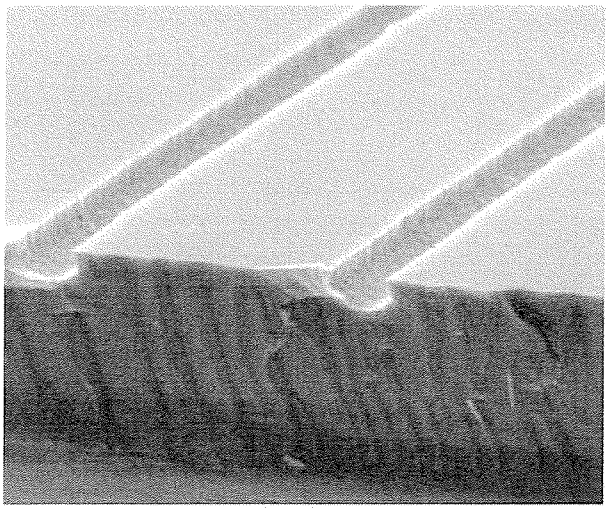
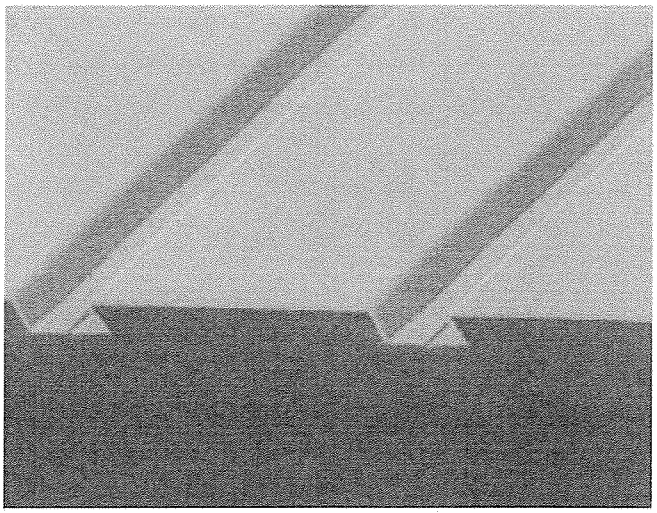


FIG. 1f



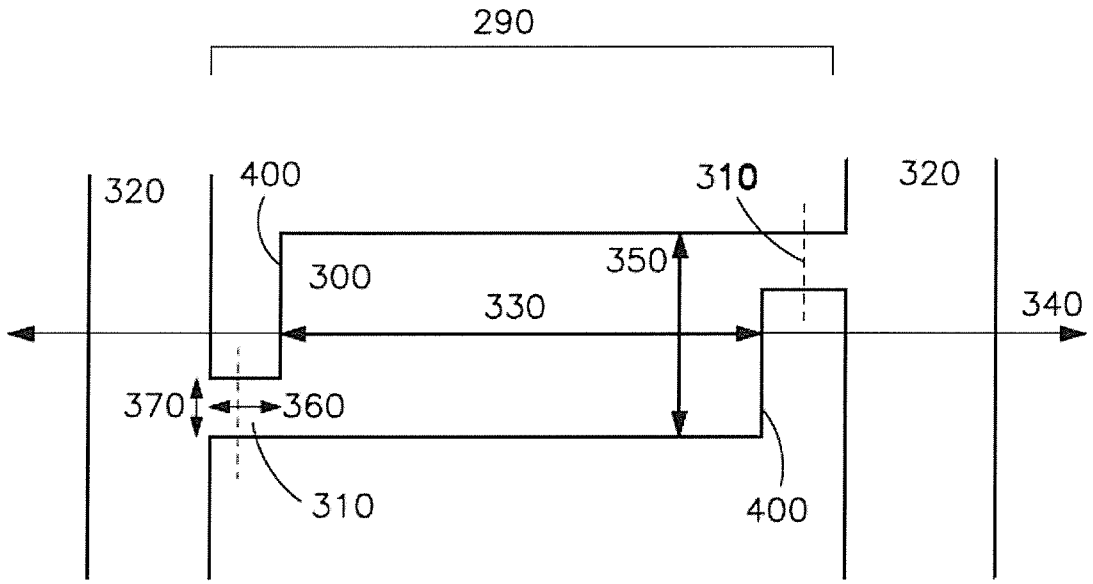

290
320
400
310
320
300
350
330
340
370
360
310
400

FIG. 2a

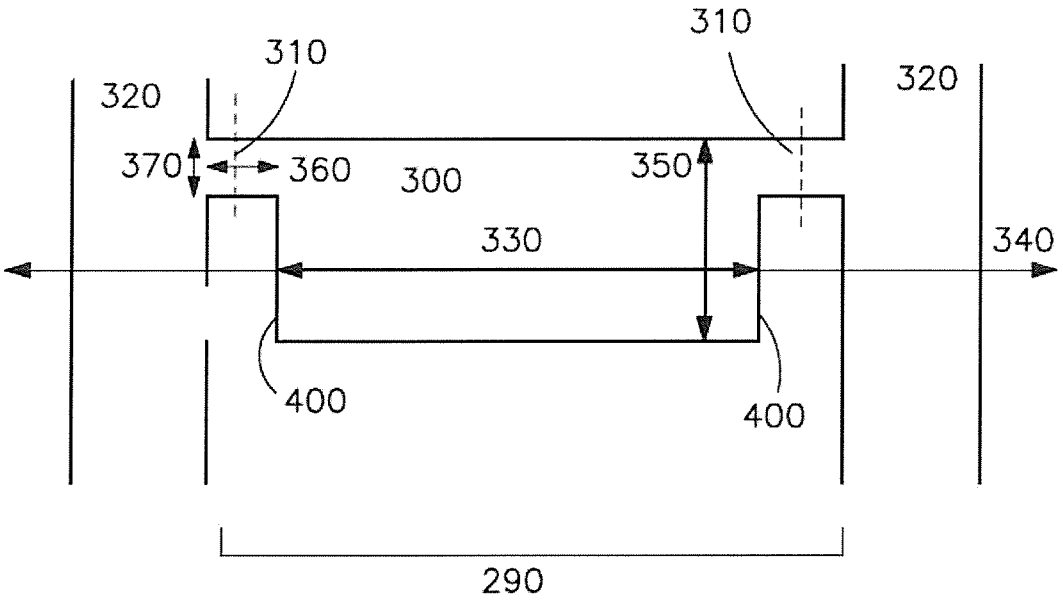

310
310
320
320
370
360
300
350
330
340
400
400
290

FIG. 2b

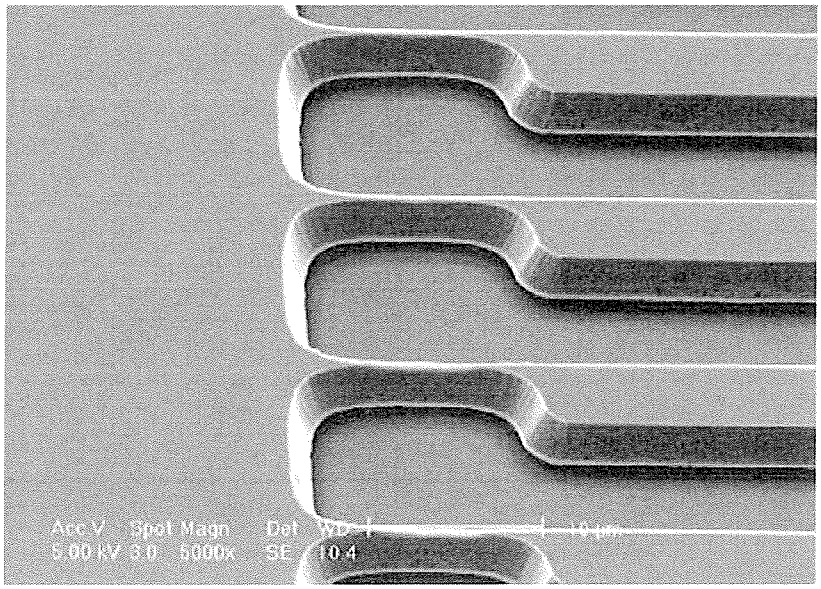

Acc.V Spot Magn Det WD
5.00 kV 3.0 5000x SE 10.4

FIG. 2c

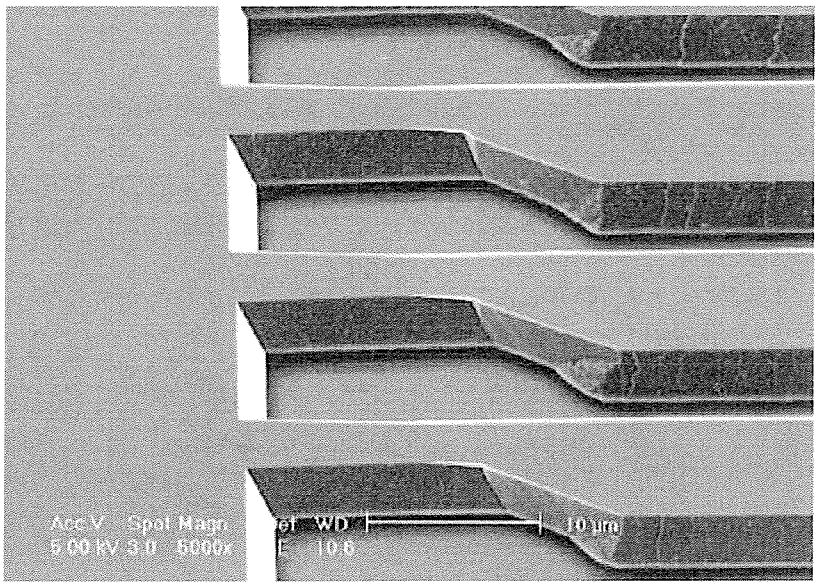

Acc.V Spot Magn
5.00 kV 3.0 5000x
WD
10.6
10 µm

FIG. 2d

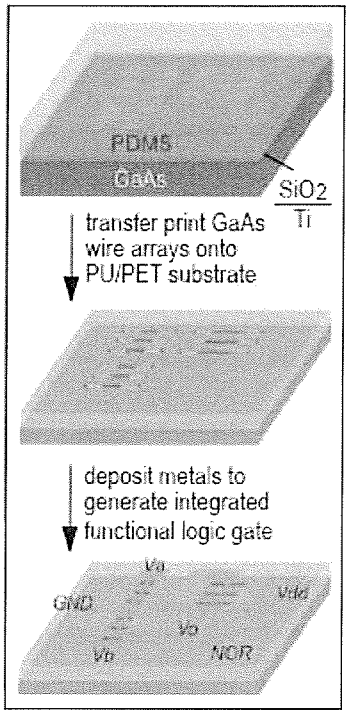


FIG. 3a

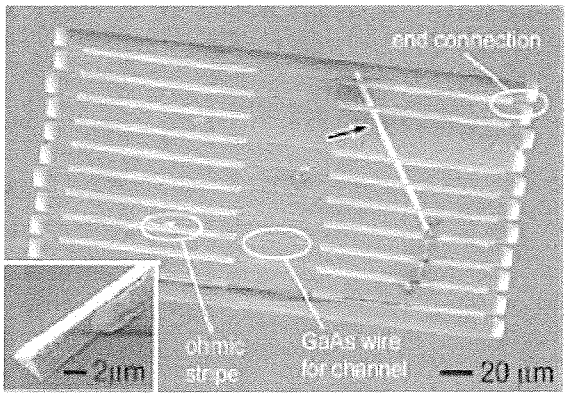


FIG. 3b

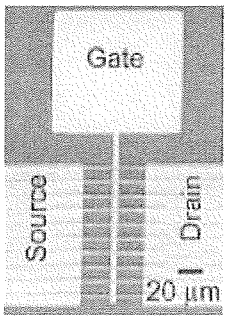


FIG. 3c

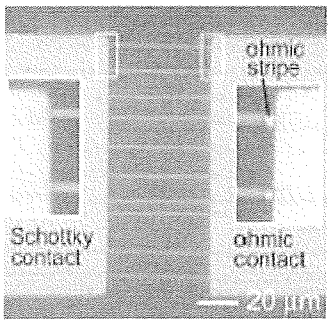


FIG. 3d

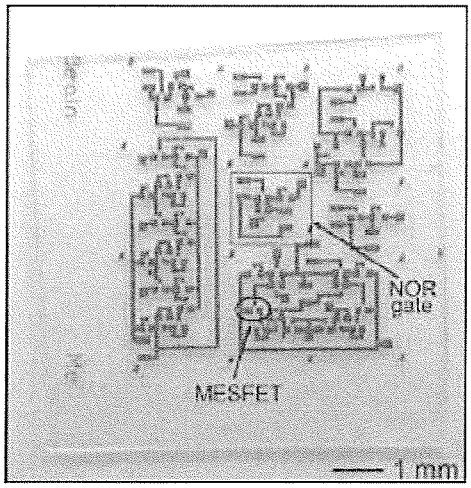


FIG. 3e

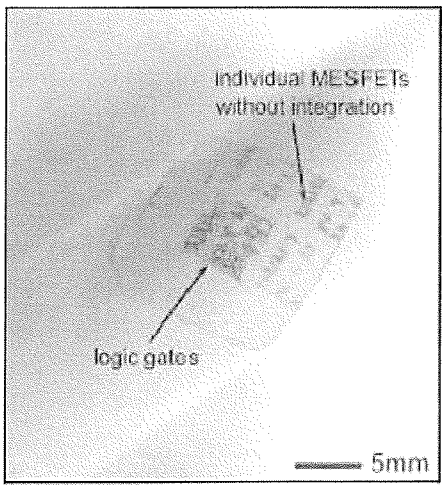


FIG. 3f

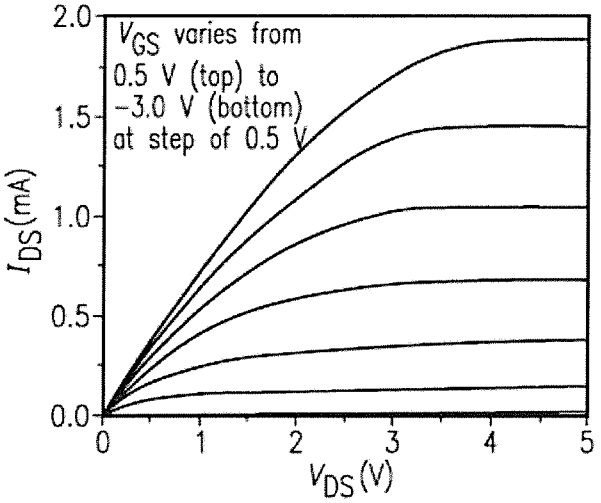


FIG. 4a

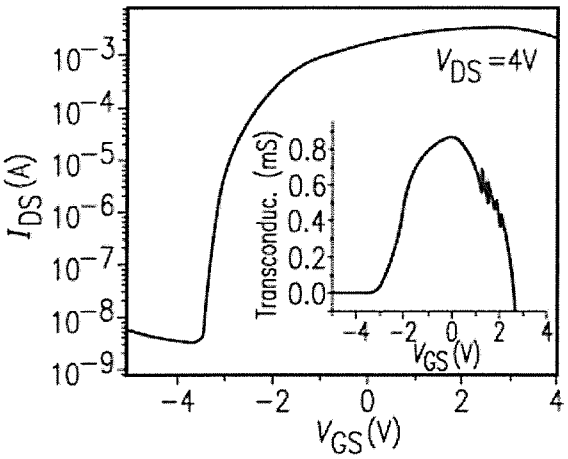


FIG. 4b

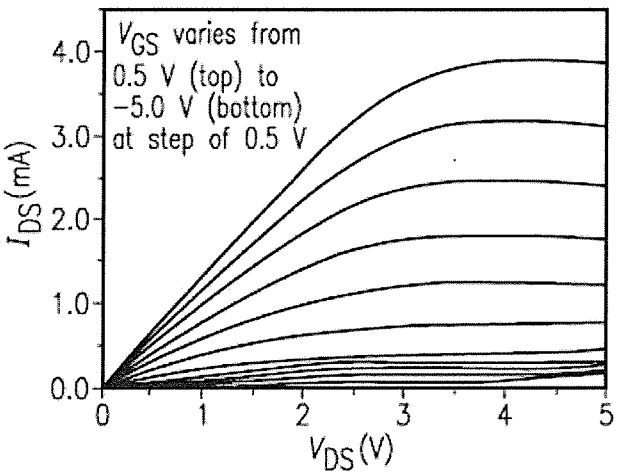


FIG. 4c

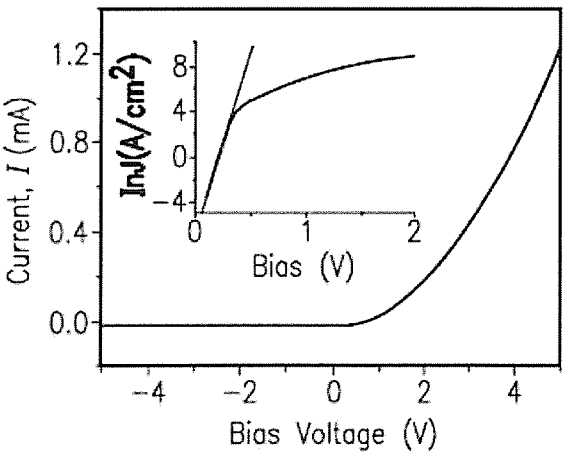


FIG. 4d

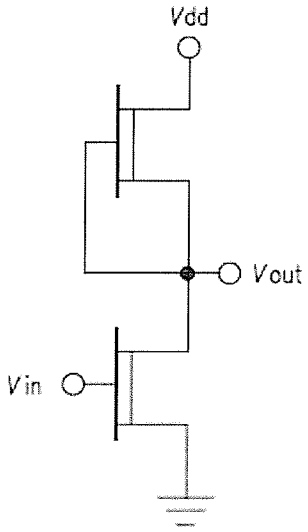


FIG. 5a

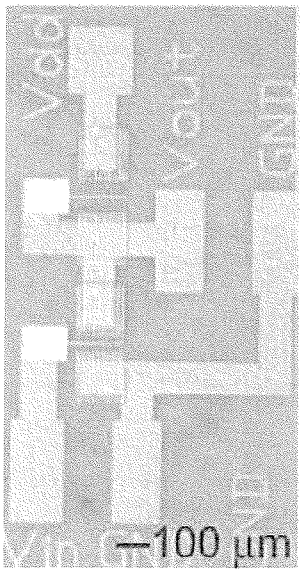


FIG. 5b

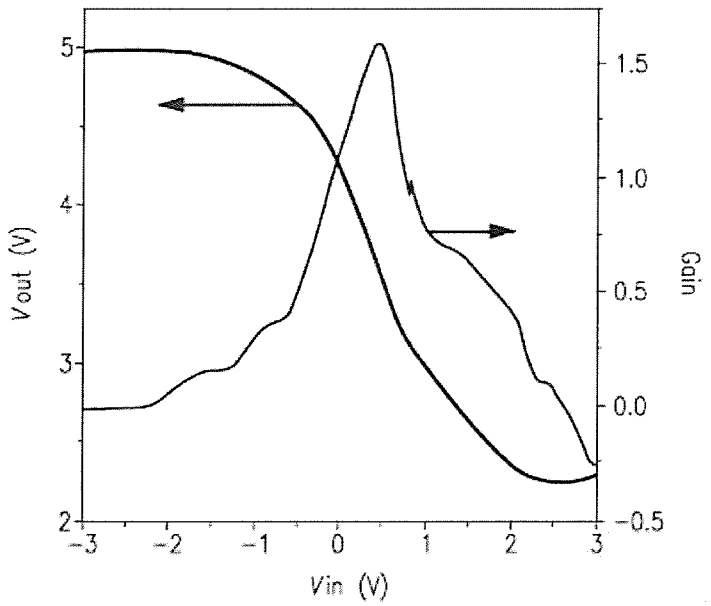


FIG. 5c

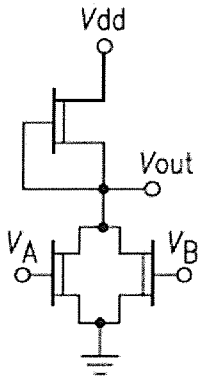


FIG. 6a

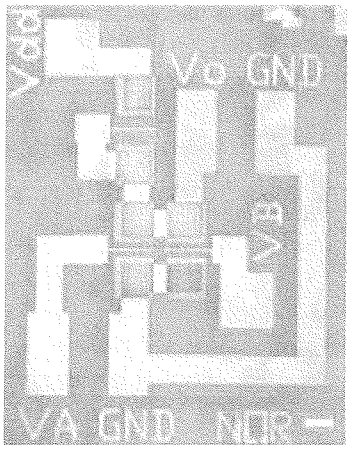


FIG. 6b

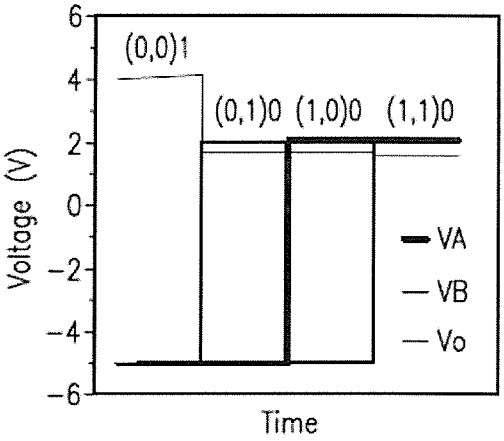


FIG. 6c

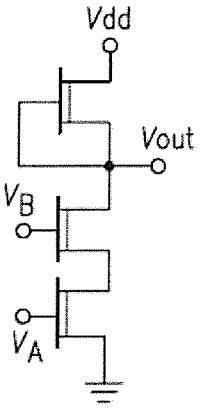


FIG. 6d

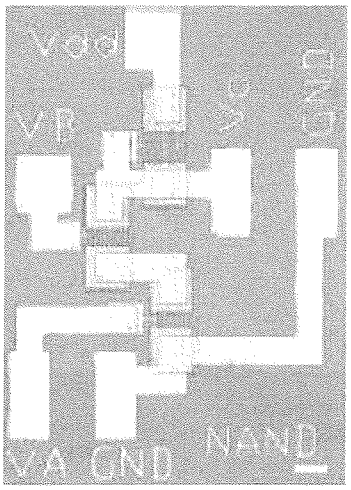


FIG. 6e

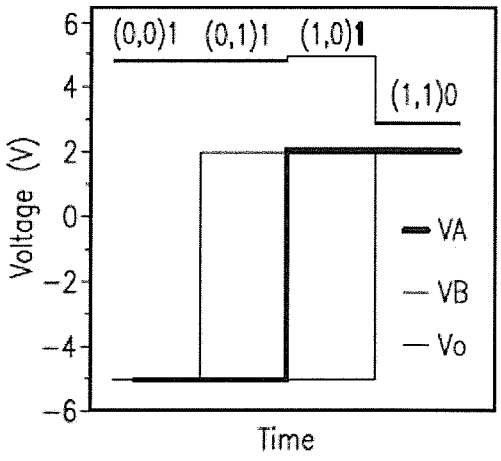


FIG. 6f

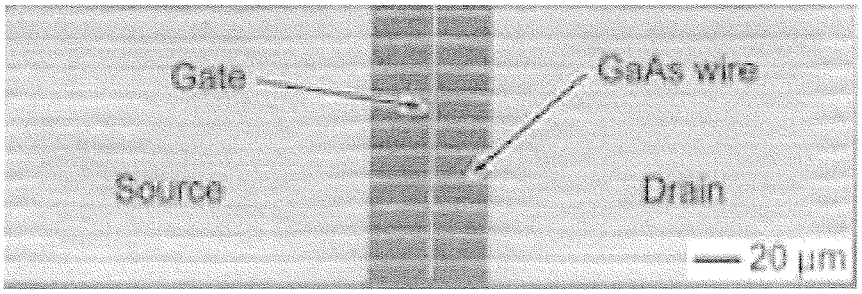

Gate
GaAs wire
Source
Drain
20 μm

FIG. 7a

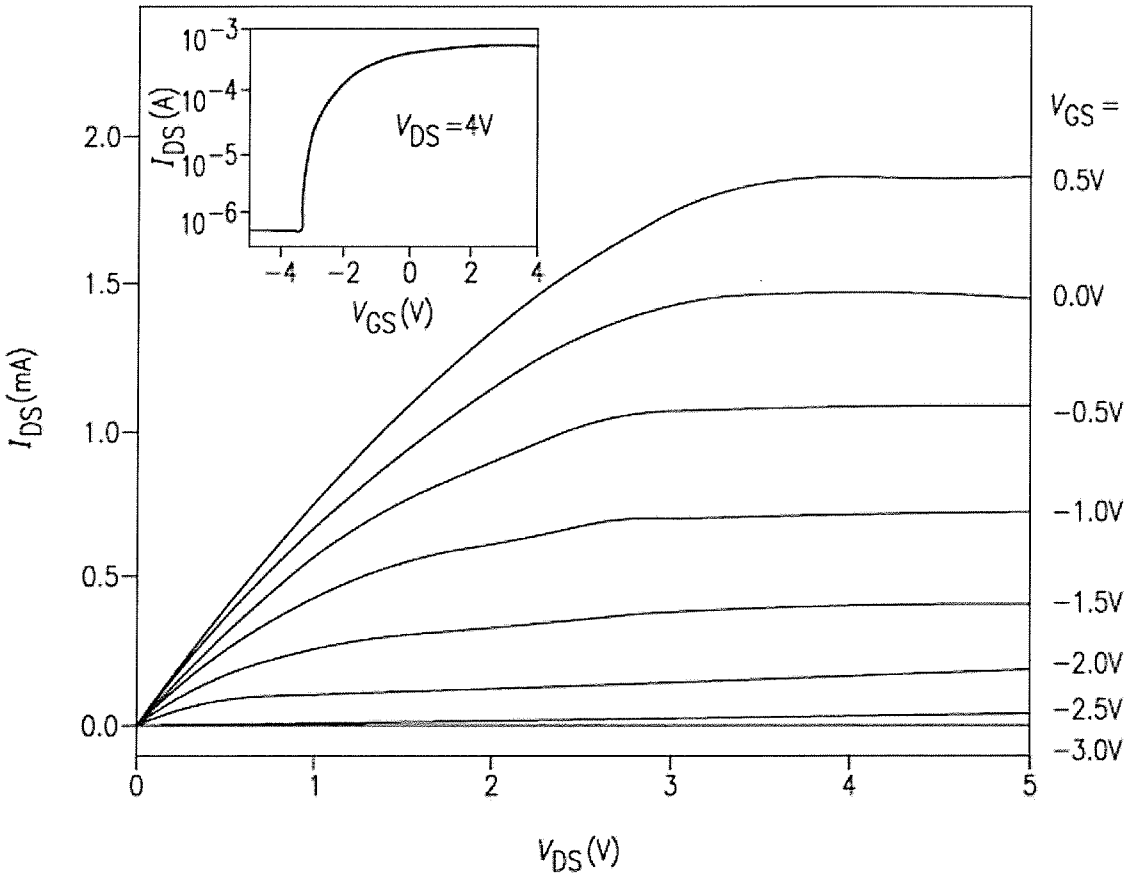

I_{DS} (mA)
2.0
1.5
1.0
0.5
0.0
0
1
2
3
4
5
V_{DS} (V)
V_{GS} =
0.5V
0.0V
−0.5V
−1.0V
−1.5V
−2.0V
−2.5V
−3.0V
I_{DS} (A)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
V_{DS} =4V
−4
−2
0
2
4
V_{GS} (V)

FIG. 7b

FIG. 8a

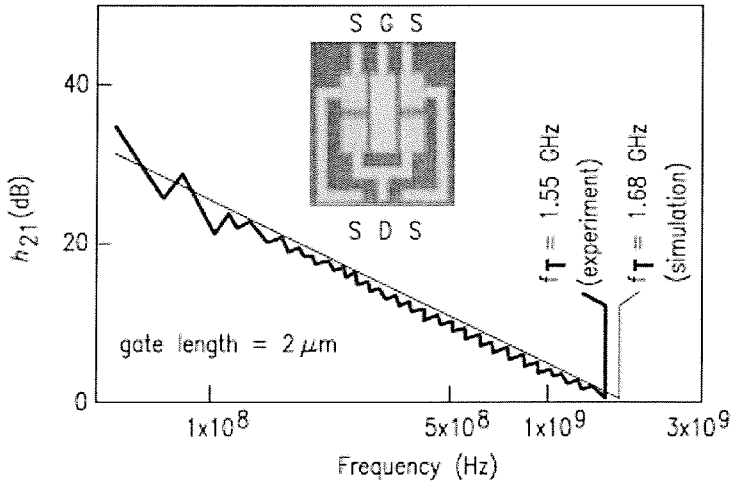


FIG. 8b

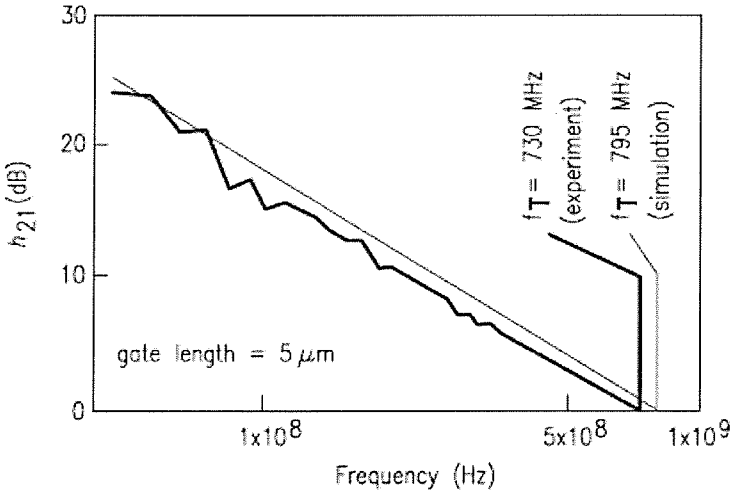


FIG. 8c

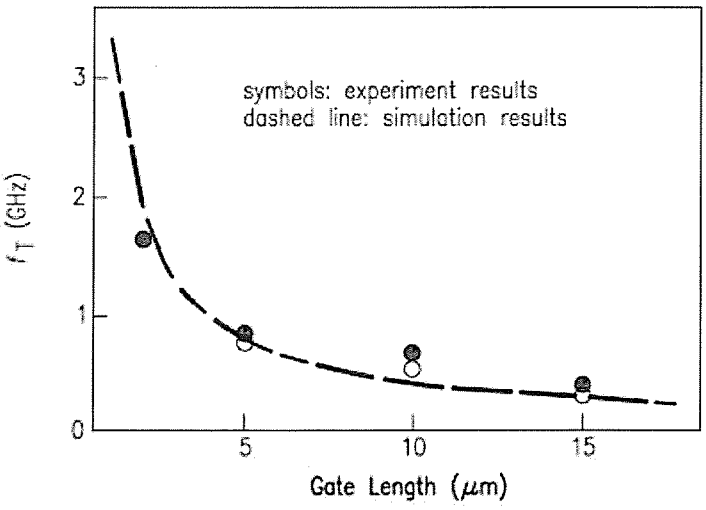


FIG. 9a

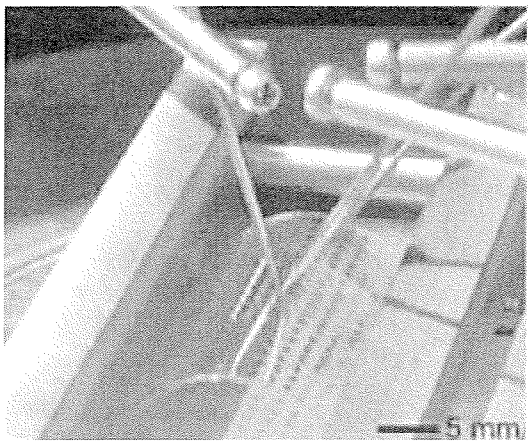


FIG. 9b

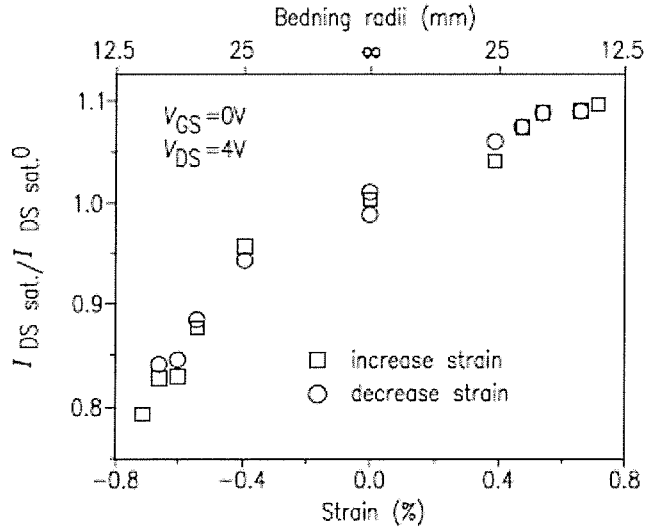


FIG. 9c

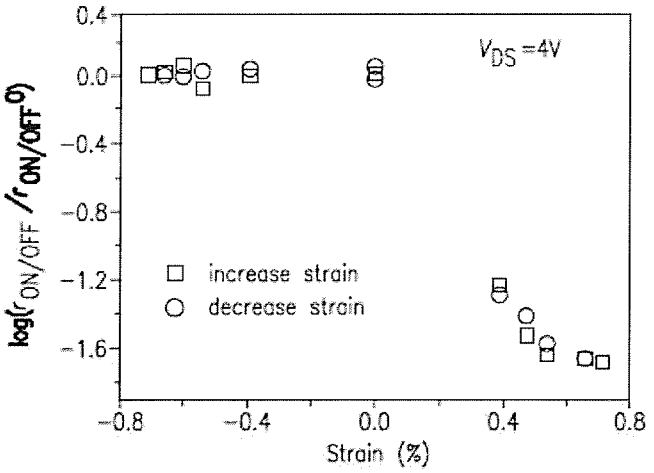


FIG. 10a

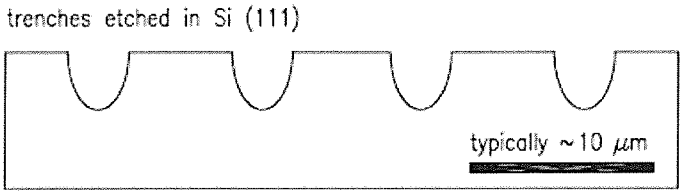


FIG. 10b

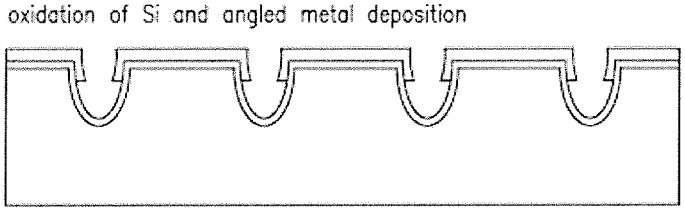


FIG. 10c

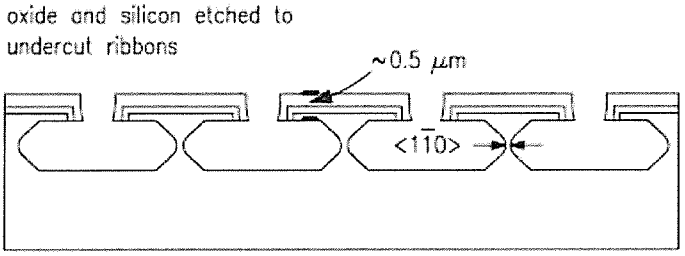


FIG. 10d

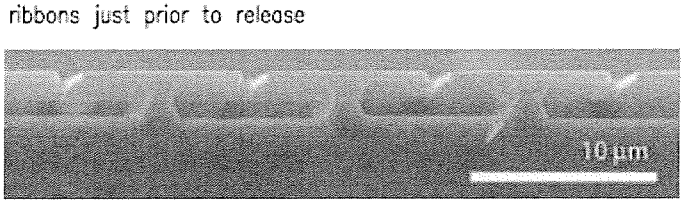
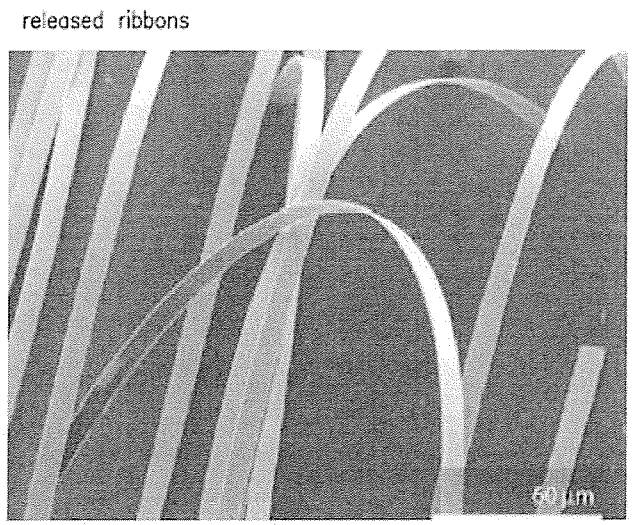


FIG. 10e



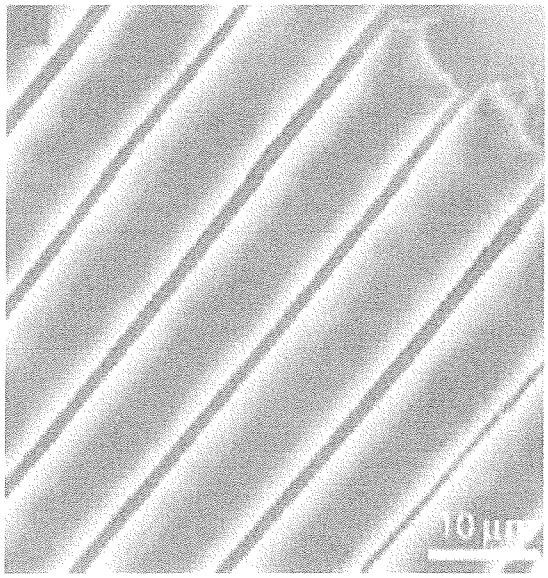


FIG. 11a

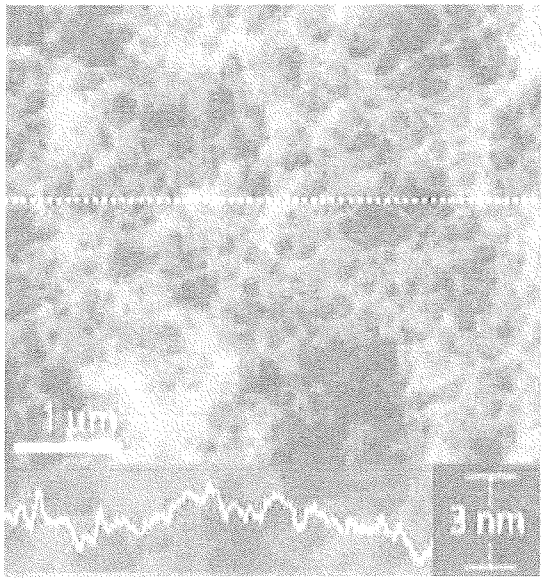


FIG. 11b

apply stamp to donor substrate

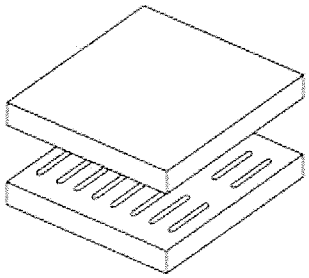


FIG. 12a

retrieve ribbons

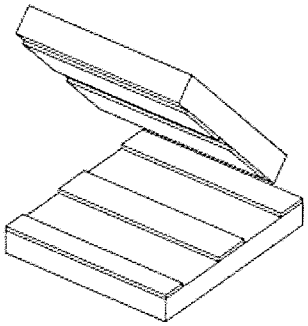


FIG. 12b

print ribbons onto plastic sheet

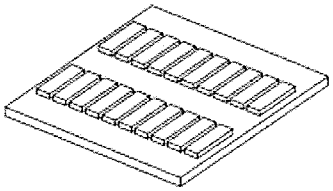


FIG. 12c

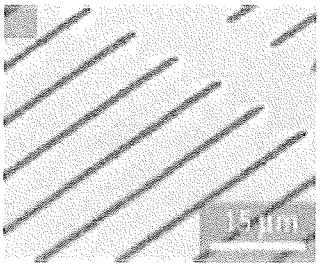


FIG. 12d

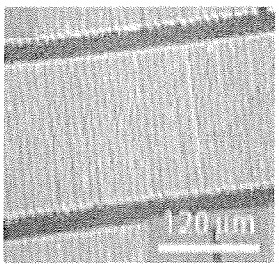


FIG. 12e

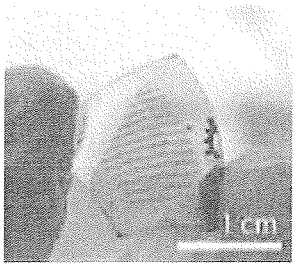


FIG. 12f

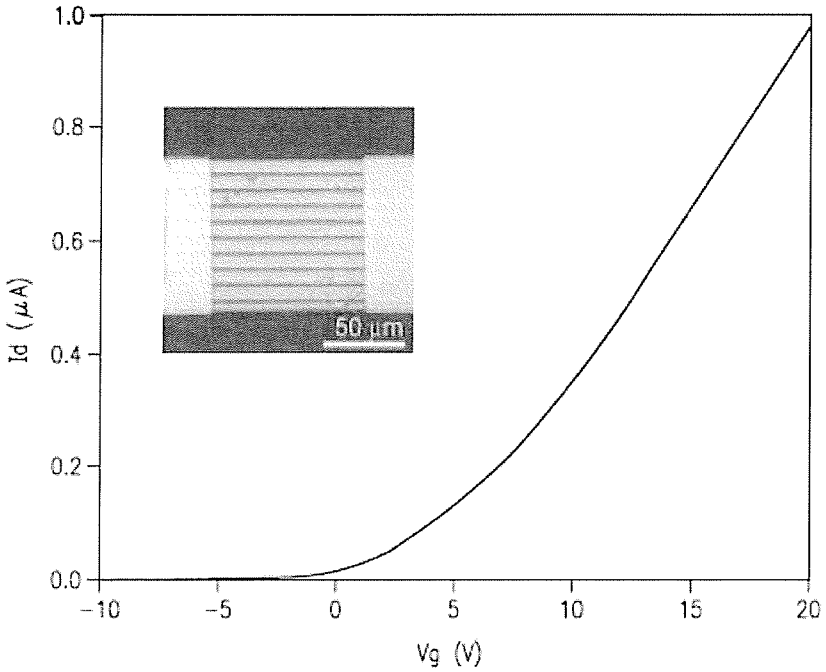


FIG. 13a

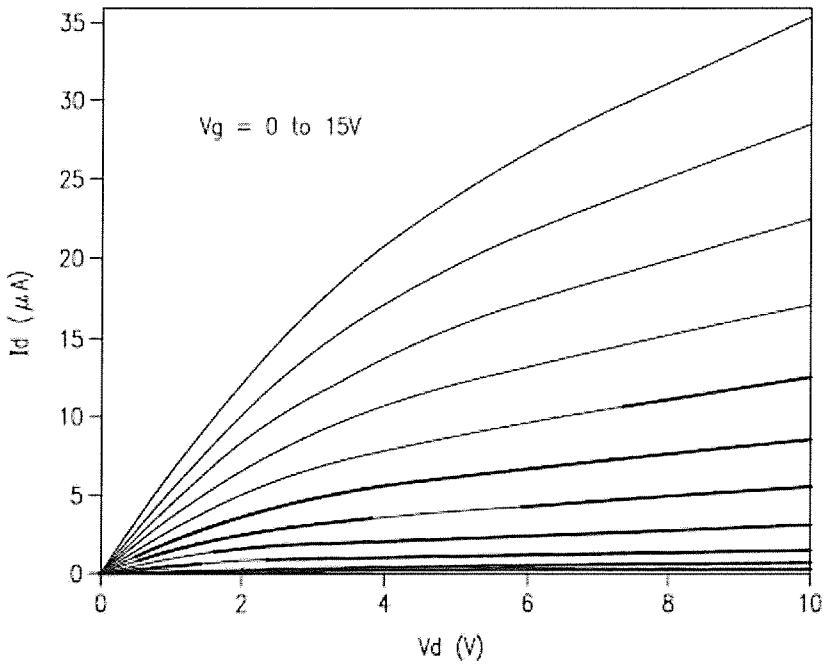


FIG. 13b

FIG. 14a

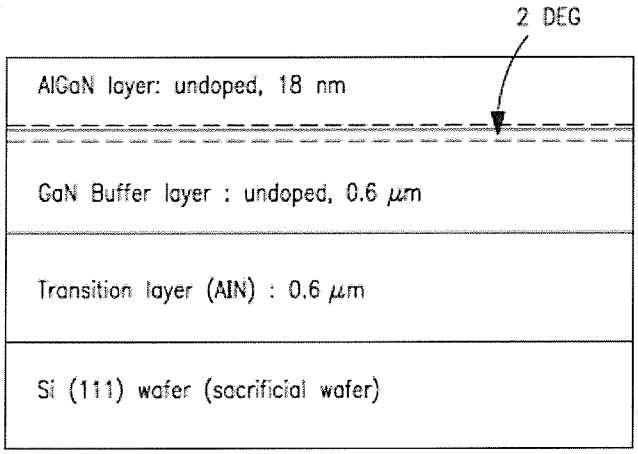


FIG. 14b

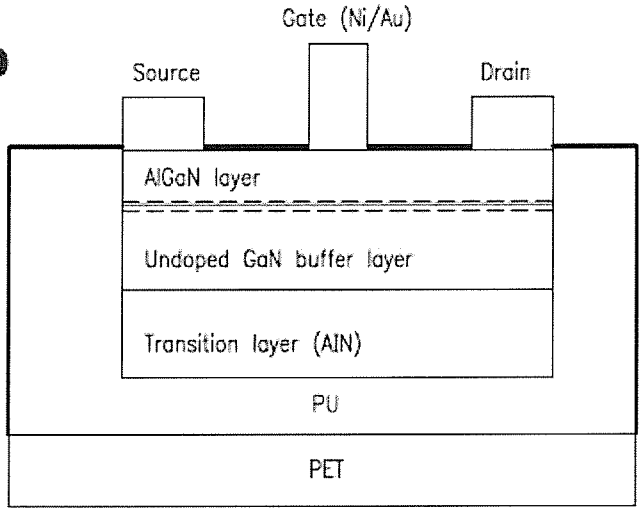
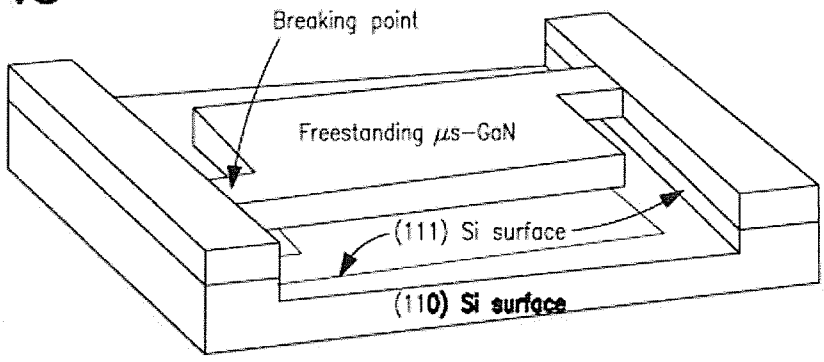


FIG. 14c



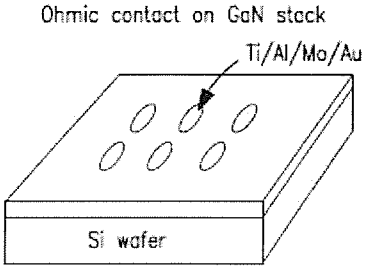


FIG. 15a

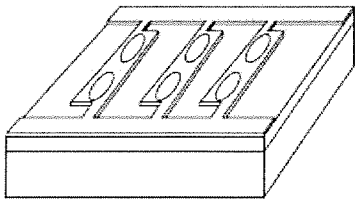


FIG. 15b

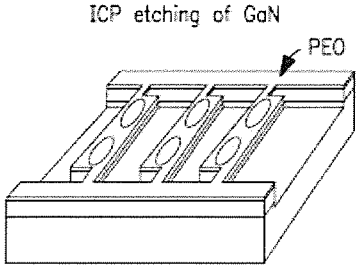


FIG. 15c

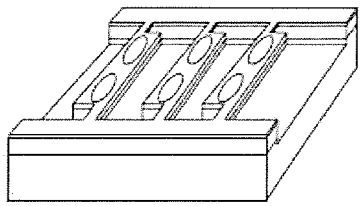


FIG. 15d

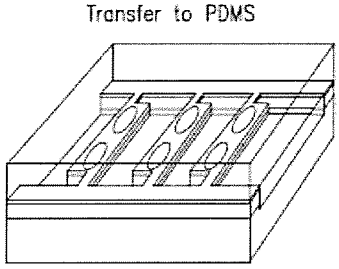


FIG. 15e

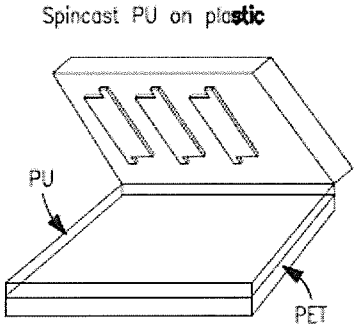


FIG. 15f

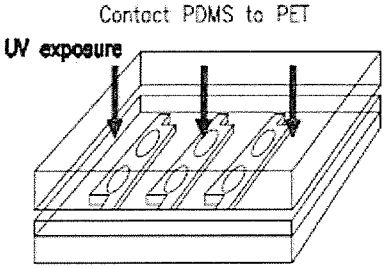


FIG. 15g

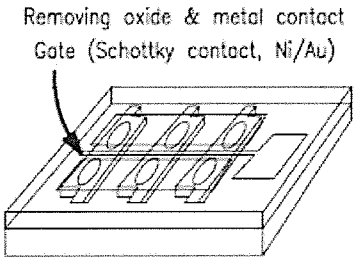


FIG. 15h

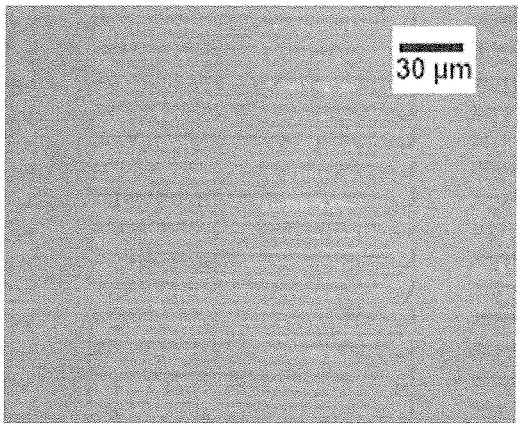


FIG. 16a

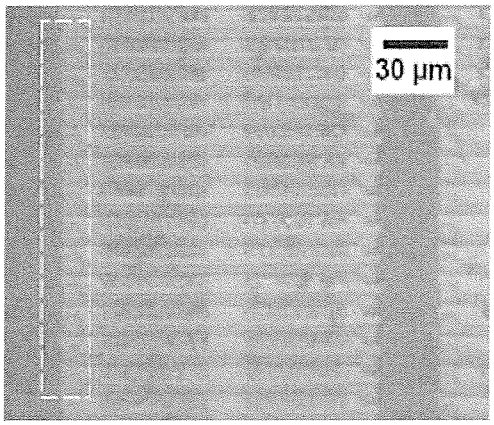


FIG. 16b

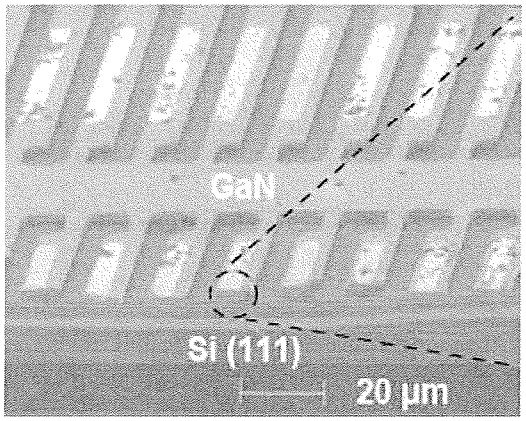


FIG. 16c

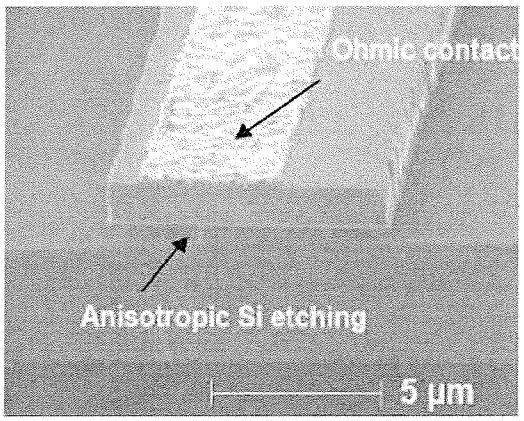


FIG. 16d

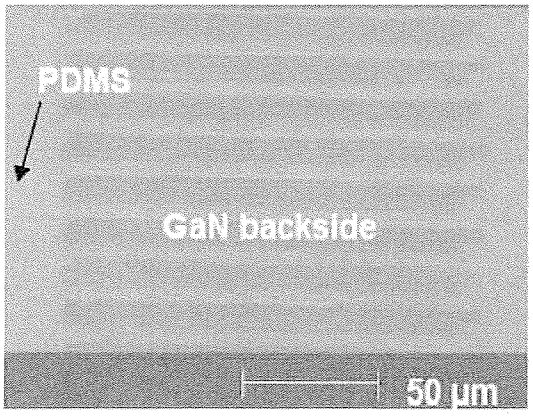


FIG. 16e

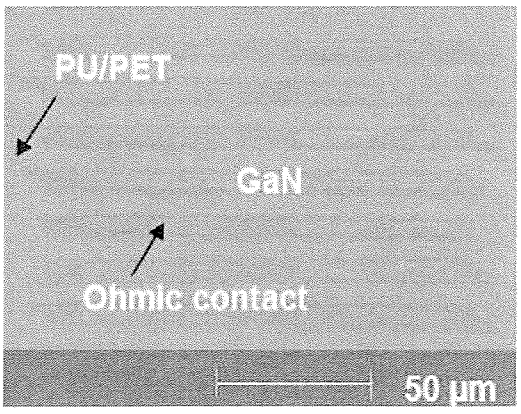


FIG. 16f

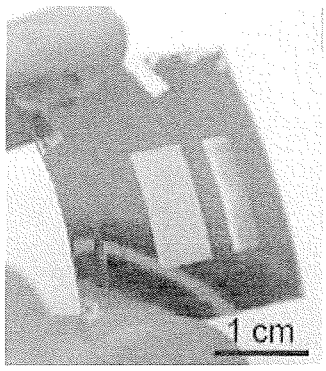


FIG. 17a

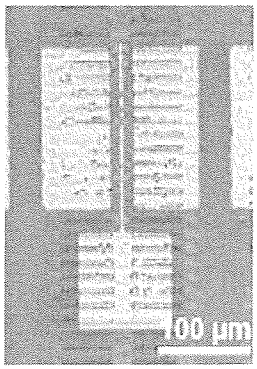


FIG. 17b

FIG. 17c

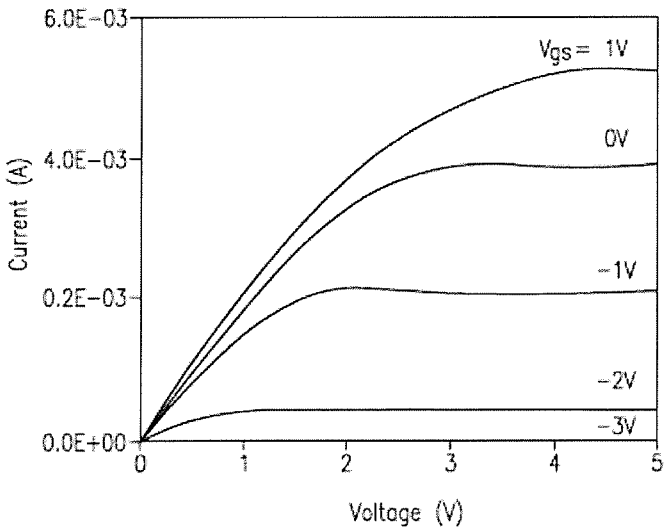


FIG. 17d

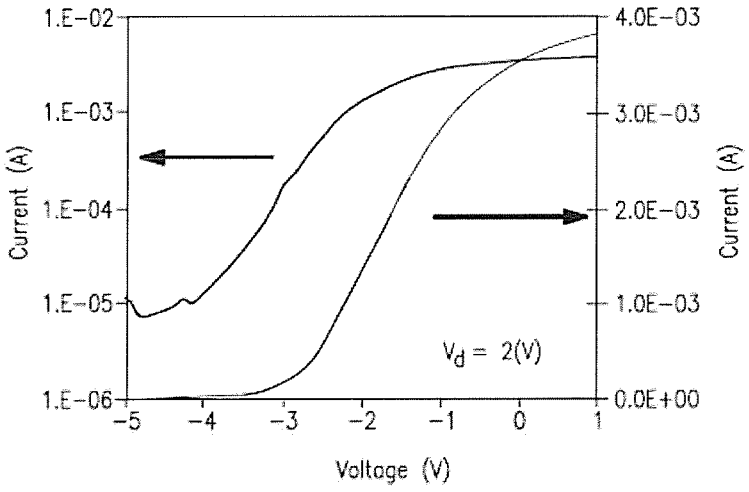


FIG. 18a

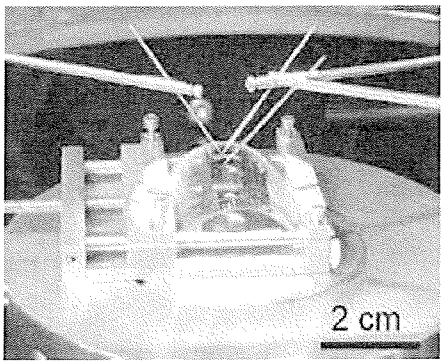


FIG. 18b

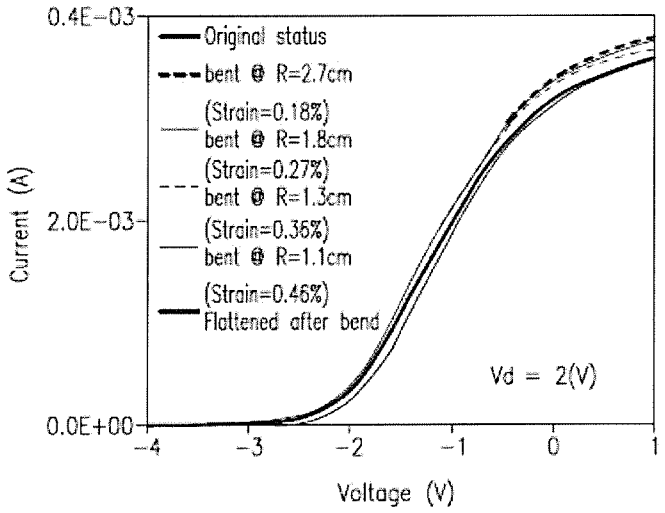
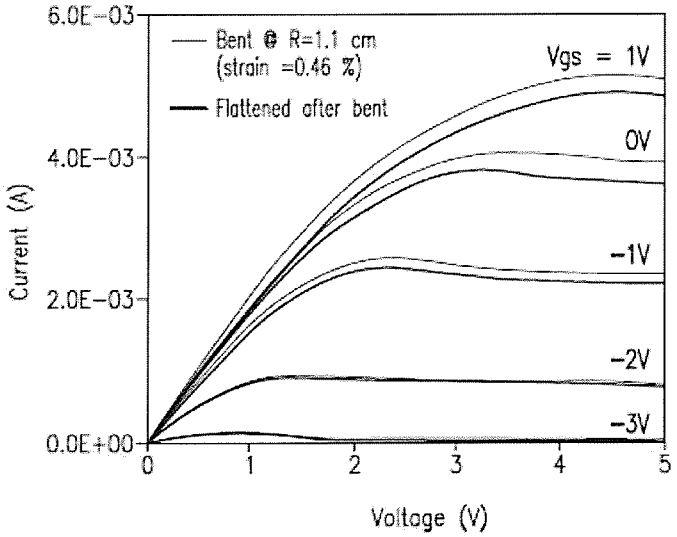


FIG. 18c



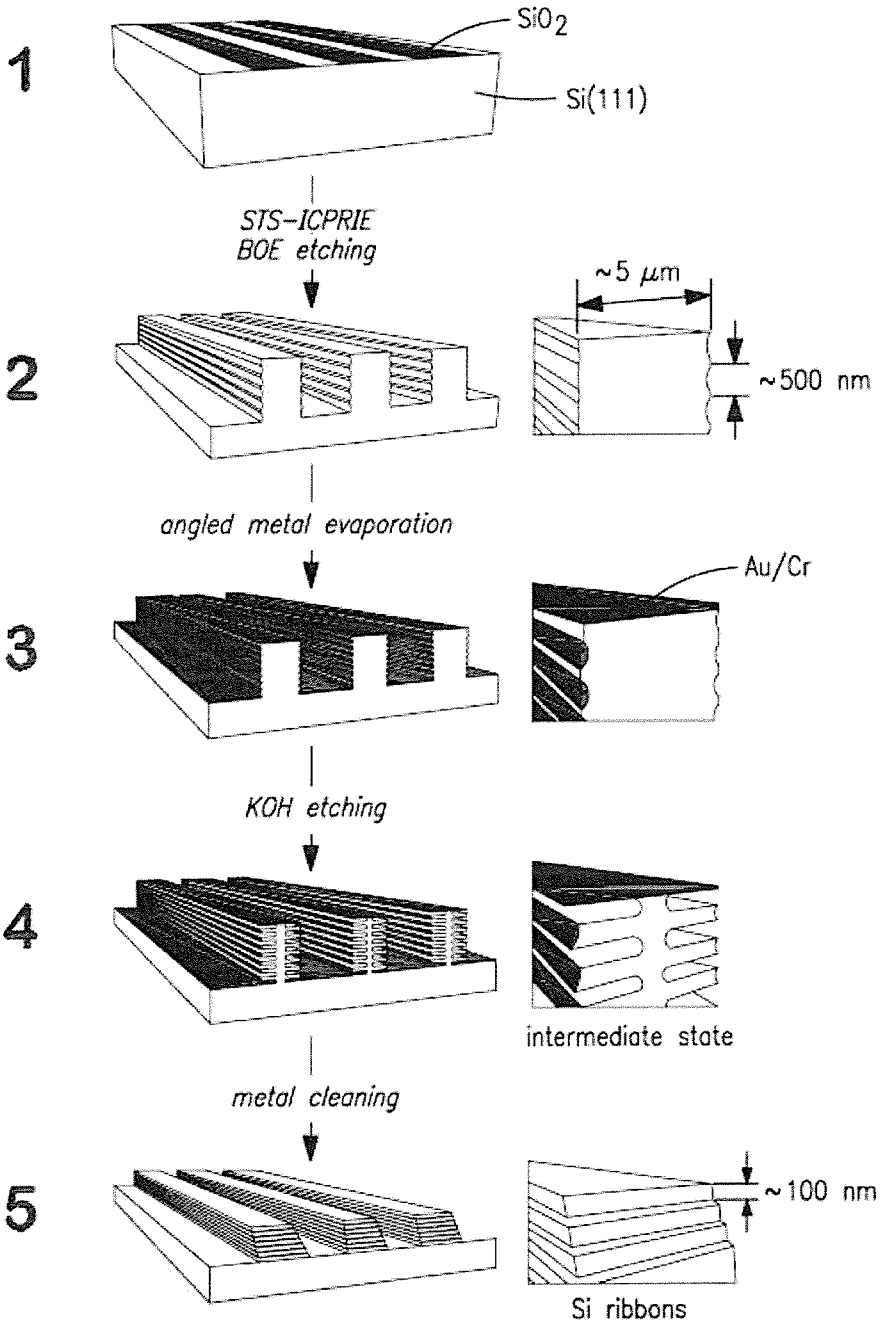

1
SiO_2
Si(111)
STS-ICPRIE
BOE etching
2
~5 μm
~500 nm
angled metal evaporation
3
Au/Cr
KOH etching
4
intermediate state
metal cleaning
5
~100 nm
Si ribbons

FIG. 19

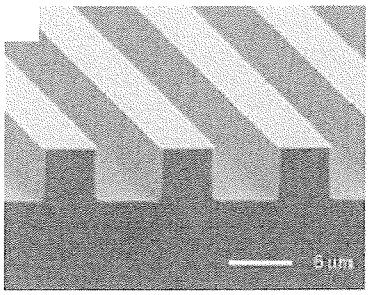


FIG. 20a

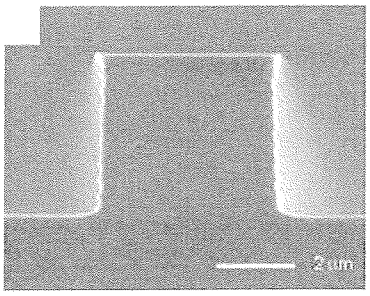


FIG. 20b

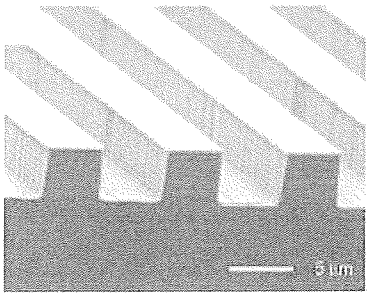


FIG. 20c

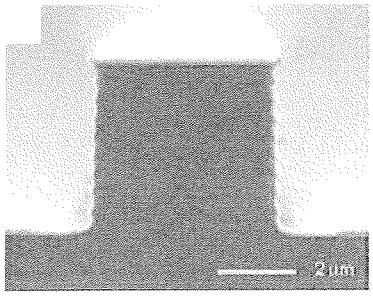


FIG. 20d

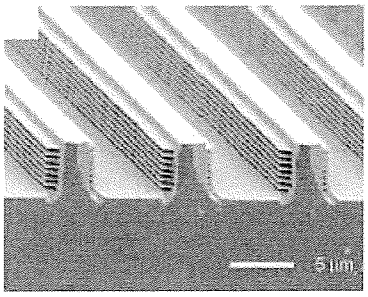


FIG. 20e

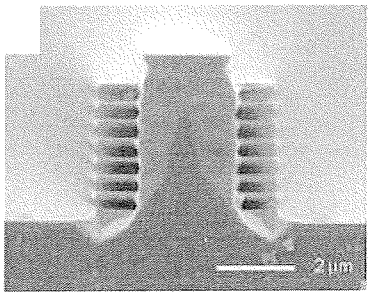


FIG. 20f

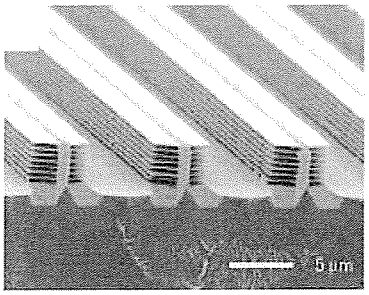


FIG. 20g

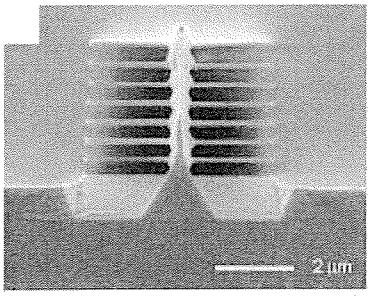


FIG. 20h

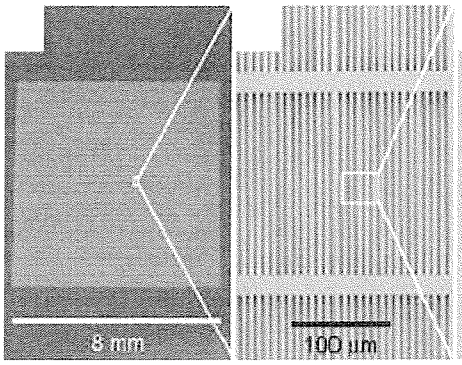


FIG. 21a

FIG. 21b

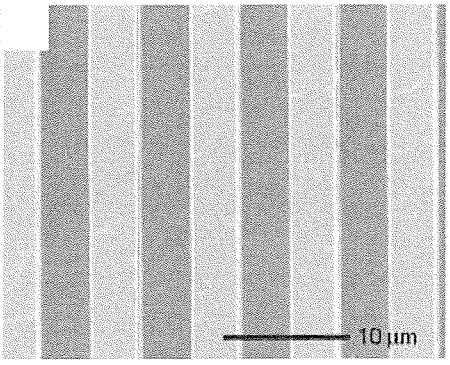


FIG. 21c

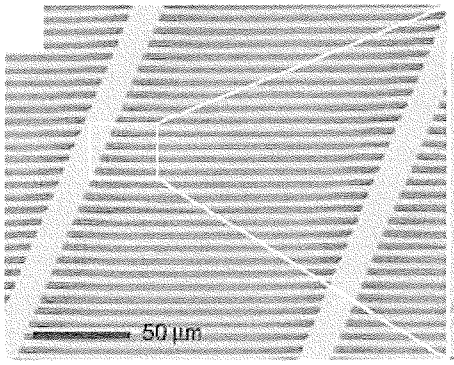


FIG. 21d

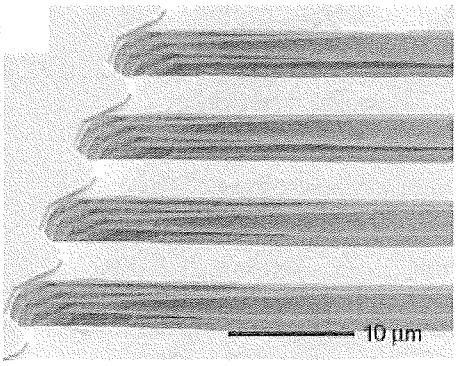


FIG. 21e

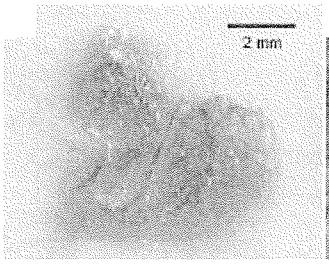


FIG. 22a

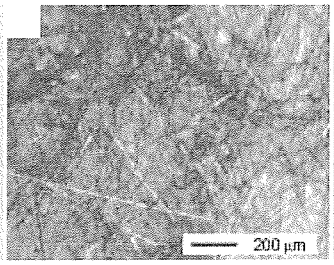


FIG. 22b

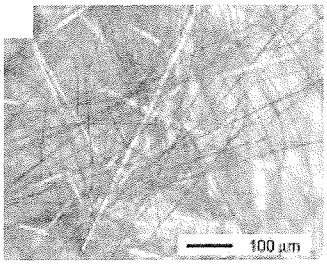


FIG. 22c

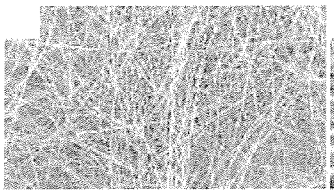


FIG. 22d

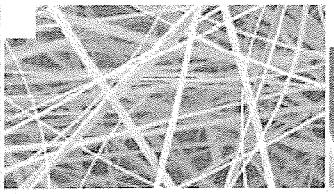


FIG. 22e

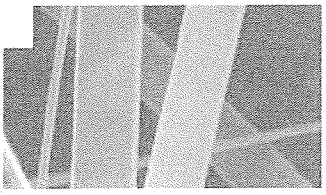


FIG. 22f

FIG. 23a

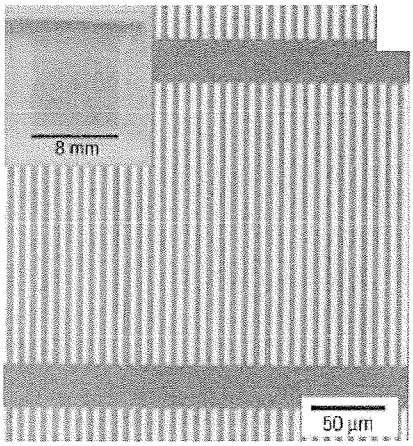


FIG. 23b

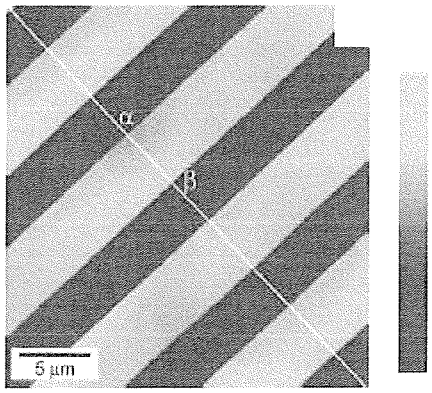


FIG. 23c

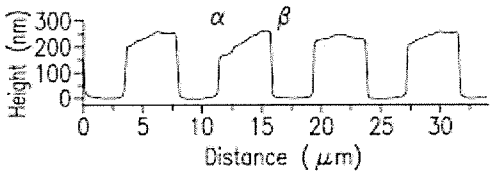


FIG. 23d

