



SILICON GERMANIUM BIPOLAR TRANSISTOR

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5 The present invention relates to bipolar transistors, and more particularly to a silicon germanium (SiGe) bipolar transistor which includes a lightly doped Si collector region and a SiGe base region that include carbon, C, continuously incorporated throughout the collector and SiGe base regions. A method of continuously incorporating C into the lightly doped Si collector region and SiGe base region of a SiGe bipolar transistor is also disclosed herein. The term SiGe is used herein to
10 denote silicon-germanium alloys, i.e., $\text{Si}_{1-x}\text{Ge}_x$.

15 Significant growth in both high-frequency wired and wireless markets has introduced new opportunities where compound semiconductors such as SiGe have unique advantages over bulk complementary metal oxide semiconductor (CMOS) technology. With the rapid advancement of epitaxial-layer pseudomorphic SiGe deposition processes, epitaxial-base SiGe heterojunction bipolar transistors have been integrated with mainstream advanced CMOS development for wide market acceptance, providing the advantages of SiGe technology for analog and RF circuitry while
20 maintaining the full utilization of the advanced CMOS technology base for digital logic circuitry.

25 SiGe heterojunction bipolar transistor devices are replacing silicon bipolar junction devices as the primary element in all analog applications. A typical prior art SiGe heterojunction bipolar transistor is shown in FIG 1. Specifically, the prior art heterojunction bipolar transistor includes an n+ subcollector layer 10 having a layer of n- Si collector (i.e., lightly doped) region 12 formed thereon. The transistor further includes p+ SiGe base region 14 formed on the lightly doped Si
30 collector region. One portion of base region 14 includes n+ Si emitter region 16 and other portions include base electrodes 18 which are separated from the emitter region by spaces 20. On top of emitter region 16 is an emitter electrode 22.

35 A major problem with bipolar SiGe transistors of the type illustrated in FIG 1 is the presence of dislocations between the collector and emitter regions. When these dislocations extend between the collector region and the emitter region, bipolar pipe, e.g., CE, shorts occur; Pipe shorts are a major yield detractor in SiGe bipolar technology.
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In the prior art, it is known to incorporate carbon into a bipolar structure so as to form a carbon layer over the base in the SiGe region only. Such a structure is shown in FIG 2 wherein reference numeral 24 denotes the grown carbon layer. This prior art technique which forms a C layer over the base in the SiGe region results in a narrow base width by hindering diffusion of the intrinsic base region. This result is shown, for example, in FIG 3.

Carbon incorporation is typically employed in the prior art to prevent the out-diffusion of boron into the base region. For example, it is known that the transient enhanced diffusion of boron is strongly suppressed in a carbon-rich silicon layer, See H.J. Osten, et al., "Carbon Doped SiGe Heterjunction Bipolar Transistors for High Frequency Applications", IEEE BTCM 7.1, 109. Boron diffusion in silicon occurs via an interstitial mechanism and is proportional to the concentration of silicon self-interstitials. Diffusion of carbon out of the carbon-rich regions causes an undersaturation of silicon self-interstitials. As a result, the diffusion of boron in these regions is suppressed. Despite being able to suppress the diffusion of boron, this prior art method which forms C over the base in the SiGe region only is not effective in reducing pipe shorts.

In view of the bipolar pipe shorts problem mentioned above, there is a continued need for the development of a new and improved method for fabricating SiGe bipolar transistors in which dislocations between the emitter and collector regions are substantially eliminated, without narrowing the base width as is the case with prior art methods.

One aspect of the present invention is to provide a method of fabricating a SiGe bipolar transistor in which the formation of dislocations between the emitter and collector regions have been substantially suppressed therefore avoiding the problem of bipolar pipe, e.g., CE, shorts.

Another aspect of the present invention is to provide a method of fabricating a SiGe bipolar structure in which the transistor yield of epitaxially grown silicon/SiGe region is enhanced.

A further aspect of the present invention is to provide a method of fabricating a bipolar SiGe transistor in which carbon can be incorporated into the structure without narrowing the base width.

A yet further aspect of the present invention is to provide a method of fabricating a bipolar SiGe transistor which is cost effective and that can be easily implemented with existing SiGe bipolar technology.

5 These and other aspects and advantages are achieved in the present invention by incorporating carbon into the lightly doped Si layer as well as the SiGe base region. In accordance with the present invention, the C incorporation occurs during the epitaxial growth of the SiGe layer by using a deposition process such as ultra-high vacuum chemical vapor
10 deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), molecular beam epitaxy (MBE), or plasma-enhanced chemical vapor deposition (PECVD), wherein a carbon source gas is employed. By employing the inventive method, carbon is continuously formed throughout the Si collector region and the SiGe base region. Moreover, applicants have
15 found that the inventive method provides enhanced yield of SiGe as well as suppressing dislocations which cause bipolar pipe shorts.

 In a first embodiment of the present invention there is provided, a method of fabricating a SiGe bipolar transistor which exhibits essentially
20 no pipe shorts. Specifically, the inventive method of fabricating the SiGe bipolar transistor includes the steps of:

(a) providing a structure which includes at least a bipolar device region, said bipolar device region including at least a collector region of a
25 first conductivity type formed in a semiconductor substrate;

(b) depositing a SiGe base region on said collector region, wherein during said depositing carbon is continuously grown through the collector region and the SiGe base region; and
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(c) forming a patterned emitter region over said SiGe base region.

 More suitably the collector is formed by the steps of epitaxially growing a Si layer on a surface of the semiconductor substrate; forming an
35 oxide layer on the epitaxially grown Si layer; implanting a dopant of the first conductivity type into the Si layer; and removing the oxide layer, and most suitably the oxide layer is removed by an HF etching process. The deposition process of step (b) may be selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD),
40 molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD), and plasma-enhanced chemical vapor deposition (PECVD), and is preferably a UHVCVD process, which is more preferably carried out a

temperature of about 650°C or less and at an operating pressure of about 250 milliTorr or less. The UHVCVD process is preferably carried out at a temperature of from about 500° to about 650°C and at an operation pressure of from about 0.1 to about 20 milliTorr, and also preferably includes a gas mixture comprising a Si source gas, a Ge source gas, a B source gas and a C source gas. The Si source gas is preferably a silane, the Ge source gas germane, the boron source gas B₂H₆, and the C source gas ethylene, methylsilane or methane. The source gases may be used undiluted or in conjunction with an inert gas, and the inert may be gas He, Ar, N₂ or H₂. The source gases may be premixed or introduced into an epi reactor as separate streams.

Aptly the step (c) above includes the steps of forming an insulator over the SiGe base region; opening an emitter window in the insulator; forming polysilicon in the emitter window; and etching the polysilicon.

Another embodiment of the present invention relates to a method of incorporating C into the collector region and the SiGe base region of a bipolar transistor. In accordance with this embodiment of the present invention, the method includes a step of depositing a SiGe base region on a lightly doped Si collector region, wherein during the depositing, carbon is continuously grown through the collector region and the SiGe base region. More suitably the depositing step includes a deposition process selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD), and plasma-enhanced chemical vapor deposition (PECVD), and most suitably the deposition process is a UHVCVD process. Preferably the UHVCVD process is carried out a temperature of about 650°C or less and at an operating pressure of about 250 milliTorr or less, and more preferably is carried out at a temperature of from about 500° to about 650°C and at an operation pressure of from about 0.1 to about 20 milliTorr. The UHVCVD process may include a gas mixture comprising a Si source gas, a Ge source gas, a B source gas and a C source gas, preferably wherein the Si source gas is a silane, the Ge source gas is germane, the boron source gas is B₂H₆, and the C source gas is ethylene, methylsilane or methane. The source gases may be used undiluted or in conjunction with an inert gas, and are preferably He, Ar, N₂ or H₂. The source gases may be premixed or introduced into an epi reactor as separate streams.

A further embodiment of the present invention relates to a SiGe bipolar transistor which includes substantially no dislocation defects present between the emitter and collector region, said structure comprising:

5 a collector region of a first conductivity type;
a SiGe base region; and

an emitter region of said first conductivity type formed over a portion of said base region, wherein said collector region and said base region include carbon continuously present in said collector and SiGe base regions and said SiGe base is further doped with B. Preferably C is
10 present in the SiGe base region in a concentration of from about 5×10^{17} to about $1 \times 10^{21} \text{ cm}^{-3}$, more suitably the C is present in the SiGe base region in a concentration of from about 1×10^{19} to about $1 \times 10^{20} \text{ cm}^{-3}$.

15 The SiGe bipolar transistor is most suitably one wherein the emitter is comprised of doped polysilicon.

The invention will be more particularly described by reference to the accompanying drawings, in which:

20 FIG 1 is pictorial representation of a fragment of a prior art SiGe bipolar transistor.

FIG 2 is a pictorial representation of a fragment of a prior art SiGe bipolar transistor including a C layer grown over the base in only the SiGe region.

FIG 3 is a plot of boron (B), germanium (Ge) and carbon (C) concentration versus depth ($\text{\AA}$) for prior art methods wherein C is
30 incorporated over the SiGe base region.

FIG 4 is a pictorial representation of a fragment of the inventive SiGe bipolar transistor including a C layer continuously grown in the collector and SiGe base regions.

35 FIGS 5-10 show the inventive SiGe bipolar transistor through the basic processing steps of the present invention.

FIGS 11-13 are plots of boron (B), germanium (Ge) and carbon (C) concentration versus depth ($\text{\AA}$) for the inventive method wherein C is
40 continuously incorporated into the collector region and the SiGe base region.

The present invention which is directed to a method of continuously incorporating C into the lightly doped Si collector region as well as the SiGe base layer and a SiGe bipolar structure produced therefrom will now be described in more detail by referring to the drawings that accompany the present invention.

Reference is first made to FIG 4 which is a cross-sectional illustration of a fragment of the inventive SiGe bipolar transistor. Specifically, the SiGe bipolar transistor shown in FIG 4 comprises a collector region 52 of a first conductivity type (n or p-type doped) which is formed on substrate 50. On top of a portion of collector region 52 is SiGe base region 54 which includes emitter region 56 and emitter diffusion 56d. Region 60 denote an insulator. The SiGe base region is characterized as being doped with B. It should be noted that the bipolar transistor shown in FIG 4 represents only a fragment of the bipolar transistor. For simplicity, the drawings have omitted other regions which are typically formed in a bipolar transistor structure.

In accordance with the present invention, the SiGe base region and the collector region, i.e., lightly doped Si, include C continuously distributed, i.e., grown, throughout these layers of the bipolar transistor. It is emphasized that the structure depicted in FIG 4 is unlike prior art SiGe bipolar transistors in which C is grown only above the SiGe base region, See FIG 2.

In accordance with the present invention, the concentration of C present within the SiGe base region and the collector region is from about 5×10^{17} to about 1×10^{19} atoms cm^{-3} , with a range of C concentration of from about 1×10^{19} to about 1×10^{20} atoms cm^{-3} being more highly preferred.

The method used in forming the inventive structure shown in FIG 4 will now be described in more detail by referring to FIGS 5-10 and the discussion that appears hereinbelow. Specifically, FIG 5 shows an initial structure that is employed in the present invention in forming the SiGe bipolar transistor. The structure of FIG 5 includes Si substrate 50 which includes collector region 52 of a first conductivity type formed on a surface of substrate 50. The structure shown in FIG 5 is formed utilizing conventional processes that are well known to those skilled in the art. For example, the collector region is formed on the surface of substrate 10 by epitaxially growing a Si layer (not shown) on the substrate. An oxide layer, not shown in the drawings, is then formed on the surface of the epi-Si layer and thereafter an n- or p-type dopant is implanted into the

epi-Si layer and the region is activated using a conventional activating annealing process. Following ion implantation and annealing, the oxide layer is removed from the surface of the structure prior to forming the SiGe layer thereon. The above processes result in the formation of the collector region in the substrate. A preferred means for removing the oxide layer is by employing a HF etching process. Another method which can be employed in the present invention in forming the subcollector region is by utilizing a conventional high-energy P-implant process.

Next, and as shown in FIG 6, SiGe layer 54 is formed on the collector region utilizing a suitable deposition process which is capable of epitaxially growing a SiGe base region while continuously growing C into the base and collector regions. The SiGe base region that is formed in the present invention typically has a thickness of from about 10 to about 200 nm. More preferably, the SiGe base region has a thickness of from about 50 to about 70 nm. It should be noted that in the present invention the SiGe base region includes C and B in the crystal lattice. That is, the SiGe base region is an alloyed SiGe region which includes SiGe, B and C therein.

In accordance with the present invention, the SiGe base layer may be formed by utilizing UHVCVD, MBE, RTCVD, PECVD or another like deposition process which is capable of epitaxially forming such a SiGe layer. Of these deposition processes, it is preferred to use a UHVCVD process.

The UHVCVD process used in the present invention in forming the SiGe base region is carried out in a low temperature epi (LTE) reactor which operates at temperatures of about 650°C or less and at operating pressures of about 250 milliTorrr or less. More preferably, the UHVCVD process is carried out in an epi reactor that operates at a temperature of from about 500° to about 650°C and at an operating pressure of from about 0.1 to about 20 milliTorrr. In the present invention, the UHVCVD process is carried out using a gas mixture which includes a Si source, a Ge source, a B source and a C source. Although a variety of Si, Ge, B and C sources can be employed in the present invention, it is preferred to utilize a gas mixture which includes a silane or other like Si-containing source gas as the Si source, germane, GeH_4 , as the Ge source, diborane, B_2H_6 , as the B source and ethylene, methylsilane or methane as the C source. Of the aforementioned C sources, it most preferred to employ ethylene as the C source gas.

The source gases may be used undiluted or the source gases may be used in conjunction with an inert gas such as helium, nitrogen, argon or hydrogen. For example, the Ge source gas may include germane in 5% inert gas and the C source gas may include one of the above mentioned C source gases (about 0.5 to about 2%) in an inert gas. Moreover, the source gases may be premixed prior to introduction into the epi reactor or the source gases may be introduced as separate streams.

The concentrations of Si and Ge employed in the present invention is not critical to the present invention as long as the Si and Ge concentrations are sufficient to form a SiGe base layer.

It is noted that the above-mentioned UHVCVD process (or related deposition processes) is capable of continuously growing C throughout the base region as well as the SiGe base region of the bipolar structure. Moreover, applicants have found that the above-mentioned UHVCVD process improves the yield of the SiGe base as well as suppressing the dislocations that cause bipolar pipe shorts. These findings are not reported in prior art processes wherein C is grown over the SiGe base region only. The present process thus represents an improved means of forming a SiGe bipolar transistor, wherein C essentially forms an intrinsic sink.

FIGS 11-13 illustrate the SiGe profile for the process in which C is incorporated in the UHVCVD deposited epitaxial grown SiGe base and in the Si collector region. The carbon is grown in discrete intervals separating the SiGe base region and the lightly doped Si layer (i.e., collector) in FIG 11 and is continuously formed throughout these regions in FIG 12. The low concentration of C in the lightly doped Si acts as an intrinsic sink reducing dislocation formation. Incorporation of C does restrict the Ge profile; therefore, as shown in FIGS 12-13, the Ge profile can be graded and is not fixed.

Referring back to the inventive process, insulator 60 is then formed of the surface of the SiGe film utilizing a conventional deposition process well known in the art, See FIG 7. Suitable deposition processes include, but are not limited to: CVD, plasma-enhanced CVD, sputtering, chemical solution deposition and other like deposition processes. Insulator 60 may comprise a single insulator material or it may include combinations of more than one insulator material, i.e., a dielectric stack. The insulator used in this step of the present invention may comprise an oxide, a nitride or a combination thereof.

FIG 8 shows the structure after emitter window opening 62 has been formed through insulator 60 exposing a surface of SiGe film. The emitter window opening is formed utilizing conventional lithography and etching such as reactive-ion etching (RIE).

FIG 9 shows the structure after a layer of intrinsic polysilicon 64 is formed in the emitter window opening as well as over the insulator layer. The intrinsic polysilicon which forms the emitter region of the bipolar SiGe transistor is formed by any conventional in-situ doping deposition process that is well known to those skilled in the art.

After forming the polysilicon layer in the structure, the polysilicon layer is patterned using conventional lithography and etching forming the structure shown in FIG 10. Selective etching processes that are capable of removing portions of the insulator and the SiGe layer are then performed so as to provide the structure shown in FIG 4. The inventive method can also apply to processes commonly known in the art as self-aligned bipolar processes.

While this invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

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CLAIMS

1. A method of fabricating a SiGe bipolar transistor including C in the collector region as well as the SiGe base region which comprises the steps of:

(a) providing a structure which includes at least a bipolar device region, the bipolar device region including at least a collector region of a first conductivity type formed in a semiconductor substrate;

(b) depositing a SiGe base region on the collector region, wherein during the depositing carbon is continuously grown through the collector region and the SiGe base region; and

(c) forming a patterned emitter region over the SiGe base region;

wherein the collector is formed by the steps of epitaxially growing a Si layer on a surface of the semiconductor substrate; forming an oxide layer on the epitaxially grown Si layer; implanting a dopant of the first conductivity type into the Si layer; and removing the oxide layer.

2. The method of Claim 1 wherein the oxide layer is removed by an HF etching process.

3. The method of Claim 1 wherein the deposition process of step (b) is selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD), and plasma-enhanced chemical vapor deposition (PECVD).

4. The method of Claim 3 wherein the deposition process is a UHVCVD process.

5. The method of Claim 4 wherein the UHVCVD process is carried out at a temperature of about 650°C or less and at an operating pressure of about 250 milliTorr or less.

6. The method of Claim 5 wherein the UHVCVD process is carried out at a temperature of from about 300° to about 650°C and at an operation pressure of from about 0.1 to about 20 milliTorr.

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7. The method of Claim 4 wherein the UHVCVD process includes a gas mixture comprising a Si source gas, a Ge source gas, a B source gas and a C source gas.
8. The method of Claim 7 wherein the Si source gas is a silane, the Ge source gas is germane, the boron source gas is B_2H_6 , and the C source gas is ethylene, methylsilane or methane.
9. The method of Claim 7 wherein the source gases are used undiluted or in conjunction with an inert gas.
10. The method of Claim 9 wherein the inert gas is He, Ar, N_2 or H_2 .
11. The method of Claim 7 wherein the source gases are premixed or introduced into an epi reactor as separate streams.
12. The method of Claim 1 wherein step (c) includes the steps of forming an insulator over the SiGe base region; opening an emitter window in the insulator; forming polysilicon in the emitter window; and etching the polysilicon.
13. A method of incorporating C into the collector region and the SiGe base region of a bipolar transistor, the method comprising depositing a SiGe base region on a Si collector region, wherein the collector is formed by the steps of epitaxially growing a Si layer on a surface of the semiconductor substrate; forming an oxide layer on the epitaxially grown Si layer; implanting a dopant of the first conductivity type into the Si layer; and removing the oxide layer, characterised in that during the depositing carbon is continuously grown through the collector region and the SiGe base region.
14. The method of Claim 13 wherein the depositing step includes a deposition process selected from the group consisting of ultra-high vacuum chemical vapor deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD), and plasma-enhanced chemical vapor deposition (PECVD).
15. The method of Claim 14 wherein the deposition process is a UHVCVD process.

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16. The method of Claim 15 wherein the UHVCVD process is carried out at a temperature of about 650°C or less and at an operating pressure of about 250 milliTorr or less.

17. The method of Claim 16 wherein the UHVCVD process is carried out at a temperature of from about 500° to about 650°C and at an operation pressure of from about 0.1 to about 20 milliTorr.

18. The method of Claim 15 wherein the UHVCVD process includes a gas mixture comprising a Si source gas, a Ge source gas, a B source gas and a C source gas.

19. The method of Claim 18 wherein the Si source gas is a silane, the Ge source gas is germane, the boron source gas is B_2H_6 , and the C source gas is ethylene, methylsilane or methane.

20. The method of Claim 18 wherein the source gases are used undiluted or in conjunction with an inert gas.

21. The method of Claim 20 wherein the inert gas is He, Ar, N_2 or H_2 .

22. The method of Claim 18 wherein the source gases are premixed or introduced into an spi reactor as separate streams