Claims:

1. A microelectronic assembly, comprising:

a first die comprising a first face and a second face; and

a second die, the second die comprising a first face and a second face, wherein the second die further comprises a plurality of first conductive contacts at the first face and a plurality of second conductive contacts at the second face, and the second die is between first-level interconnect contacts of the microelectronic assembly and the first die.

2. The microelectronic assembly of Claim 1, wherein the first die further comprises:

a plurality of first conductive contacts at the first face of the first die interconnected with the first-level interconnect contacts of the microelectronic assembly; and

a plurality of second conductive contacts at the first face of the first die interconnected with the second die.

3. The microelectronic assembly of Claim 2, wherein a set of the plurality of the second conductive contacts at the first face of the first die have a same pitch and are interconnected to the second die.

4. The microelectronic assembly of Claim 2, wherein a first set of the plurality of the second conductive contacts at the first face of the first die have a first pitch, a second set of the plurality of the second conductive contacts of the first die have a second pitch, the first set and the second set are interconnected to the second die, and the first pitch and second pitch are different.

5. The microelectronic assembly of Claim 1, wherein the microelectronic assembly further comprises:

a redistribution layer (RDL), wherein the RDL comprises one or more interconnect structures and the second die is between the first die and at least a portion of the RDL.

6. The microelectronic assembly of Claim 5, wherein at least one of:

one interconnect structure of the RDL includes a conductive pathway between at least one first conductive contact of the first die and at least one first-level interconnect contact of the microelectronic assembly;

one interconnect structure of the RDL includes a conductive pathway between at least one second conductive contact of the second die and at least one first-level interconnect contact of the microelectronic assembly;

one interconnect structure of the RDL includes a conductive pathway between at least one first conductive contact of the first die and at least one second conductive contact of the second die; and

one interconnect structure of the RDL includes a conductive pathway between at least two second conductive contacts the second die.

7. The microelectronic assembly of Claim 1, wherein the second die includes a die substrate, a metallization stack, and a device layer between the die substrate and the metallization stack, and wherein the die substrate is between a package substrate and the device layer.

8. The microelectronic assembly of Claim 1, wherein the second die includes a die substrate, a metallization stack, and a device layer between the die substrate and the metallization stack, and wherein the device layer is between a package substrate and the die substrate.

9. The microelectronic assembly of Claim 1, wherein the second die includes a first metallization stack, a second metallization stack, and a device layer between the first metallization stack and the second metallization stack.

10. The microelectronic assembly of any of Claims 1-9, wherein the second die is an individual one of a plurality of second dies.

11. The microelectronic assembly of Claim 10, wherein at least one second die has a first thickness and at least one other second die has a second thickness that is different than the first thickness of the at least one second die.

12. The microelectronic assembly of Claim 9, further comprising an insulating layer between the plurality of second dies and the first die.

13. The microelectronic assembly of Claim 12, wherein at least two of the plurality of second dies are interconnected via interconnect structures of the insulating layer.

14. The microelectronic assembly of Claim 12, wherein the insulating layer is a first insulating layer, and the microelectronic assembly further comprises a second insulating layer between at least one second die of the plurality of second dies and the first insulating layer.

15. A computing device, comprising:

a composite die, the composite die comprising:

a first die ; and

a second die interconnected to the first die between first-level interconnect contacts of the composite die and the first die, wherein the second die further comprises conductive contacts at a first face and a second face.

16. The computing device of Claim 15, wherein the second die is an individual one of a plurality of second dies.

17. The computing device of Claim 15, wherein at least one of:

at least one second die of the plurality of second dies has a solder interconnection with the first die;

at least one second die of the plurality of second dies has a non-solder interconnection with the first die;

at least one second die of the plurality of second dies has an interconnection with the first die on a first layer having a first thickness; and

at least one second die of the plurality of second dies has an interconnection with the first die on a first layer having a first thickness and at least one other second die of the plurality of second dies has an interconnection with the first die on a second layer having a second thickness, wherein the first layer and the second layer comprise one or more dielectric materials.

18. The computing device of any of Claims 15-17, wherein at least one second die of the plurality of second dies has a thickness between 10 microns and 30 microns.

19. The computing device of any of Claims 15-17, wherein at least two second dies of the plurality of second dies are different types of devices.

20. The computing device of any of Claims 15-17, wherein individual ones of the plurality of second dies have a X-Y area that is smaller than an X-Y area of the first die.

21. A method of manufacturing a microelectronic assembly, comprising:

interconnecting a second die to a first die, the first die comprising a first face and a second face and the second die comprising a first face and a second face, the second die further comprising a plurality of first conductive contacts at the first face and a plurality of second conductive contacts at the second face; and

forming a redistribution layer, the redistribution layer comprising a plurality of conductive structures, wherein the second die is between at least a portion of the redistribution layer and the first die.

22. The method of manufacturing the microelectronic assembly of Claim 21, wherein the second die is one of a plurality of second dies.

23. The method of manufacturing the microelectronic assembly of Claim 22, further comprising:

forming a first layer extending from the first face of the first die, the first layer comprising an insulating material and a plurality of first interconnect structures in electrical contact with a plurality of conductive contacts at the first face of the first die, wherein the plurality of second dies are interconnected to the first die via the first layer.

24. The method of manufacturing the microelectronic assembly of Claim 23, wherein at least one second die has a first thickness and at least one other second die has a second thickness that is different than the first thickness of the at least one second die.

25. The method of manufacturing the microelectronic assembly of any of Claims 23-24, further comprising:

forming a second layer extending from the first layer and from the second face of the plurality of second dies, the second layer comprising another insulating material and a plurality of other interconnect structures.