

The present invention relates to a device for irreversibly blocking access to an integrated circuit which can be used in all fields where it is necessary, at a given time, to prevent in an irreversible manner access to certain zones or functions of the integrated circuit.

This device is particularly useful for limiting the internal accessibility of an integrated circuit after testing at the end of manufacture. In practice, after manufacture, an integrated circuit should be tested to an extent which it is incessantly sought to improve. In particular it is necessary for the internal accessibility of the integrated circuit to be maximised during the testing. However, this accessibility should then be restricted because a user of the circuit should only have access, after these tests, to what is called an applications layer. It is therefore necessary to block certain access routes.

Furthermore, a user of a programmable integrated circuit must be able to customize the said integrated circuit by programming an application. It may then be particularly important to prevent any modifications or even the reading from outside of data contained in specific memory zones. It may also be important to guard against possible external disturbances which could affect the memory zones. Blocking devices make such protection possible. Such devices are required for example in protected integrated circuits such as circuits in banking cards.

In the present state of the art, at the end of manufacture these blocking devices are in an unlocked condition and are equivalent to closed switches. The said devices can be programmed only once in an irreversible manner. Once programmed, after the tests, they are equivalent to open switches. These devices are also integrated into the circuit so that there is no possibility of short-circuiting them again. Their states are taken into account in the logic equations for access to the memory zones or the operations which they control. A blocking device is known from the document WO-A-88/00372 which comprises a control circuit for cells to make them unerasable.

Blocking devices comprising programmable fuses are also known. Each fuse, formed for example by a very thin layer of polycrystalline silicon is supplied with current by a transistor. When a current passes for a specified time, localized heating occurs which is caused by the very thin cross-section of the fuse. This heating suffices to vaporize the metal: the fuse is said to be blown. In fact it can occur that the fuse does not blow. In practice therefore a device comprising fuses is not very reliable.

Consequently an aim of the invention is to provide a blocking device which does not have this disadvantage. It employs the known characteristics of EEPROM cells which it is opportune to recall.

An EEPROM cell is an electrically erasable and programmable cell. It includes a floating gate transistor. The floating gate positioned between a control gate of the transistor and a conduction channel region of the transistor can receive electrical charges. These charges may impose a conductive state of the transistor independent of a command applied on the control gate. In an EEPROM cell the electrical charges are injected into the floating gate by the application of a powerful electrical field. A cell of this kind has the feature of having a zero threshold at the end of manufacture. It is in an initial state. It will be recalled that the threshold voltage is the minimum voltage, as an absolute value, which must be applied to the control gate for a conduction channel to be formed in the channel region. An EEPROM cell having an N type channel, has a positive threshold voltage of about 5 volts if the cell is erased. If the cell is programmed its threshold voltage is negative and is about -2 volts.

The read circuits of memory cells comprise a selection circuit which applies a control pulse on the control gate of the transistors of the memory cells of each line. With a conventional gate voltage value, of about 1.5 volts, the EEPROM cell described above conducts a current when it is programmed, because a voltage is applied to its gate which is greater than its threshold voltage. The EEPROM cell does not conduct a current when it is erased.

In the invention advantage has been taken of the fact that the EEPROM cell in its initial state behaves as if it was programmed. Moreover, in the invention, it is arranged that programming of the EEPROM cell is prevented. Under these conditions it only conducts current if it is in its initial state. Once it is erased it no longer conducts. Because it can no longer be programmed it remains in this state: the blocking device desired has been obtained.

Consequently an object of the invention is a device for blocking access to all or part of an integrated circuit comprising an EEPROM cell which is never programmable, with a device for blocking access to all or part of an integrated circuit, the EEPROM cell which is never programmable including a floating gate transistor equipped with a voltage limiter on its drain region and/or on its source region.

The characteristics of an EEPROM cell in accordance with the invention are given in the following description with reference to the attached Figures. This description and the said Figures are given only by way of non-limiting illustration of the invention. In the Figures:

- Figure 1 shows an example of a blocking device equipped with an EEPROM cell in accordance with the invention,
- Figure 2.a shows a circuit diagram equivalent to an EEPROM cell in accordance with the invention,
- Figure 2.b is a schematic cross-sectional view of a cell in accordance with Figure 2.a.

Figure 1 shows a blocking device in accordance with the invention. An EEPROM cell 1 has a source region 4 connected to ground. A drain region 3 is supplied by a polarizing current generator controlled by a circuit for selecting the cell. In a dual technology the respective roles of the source and drain regions will be reversed. A read voltage V_1 controlled by a selection circuit which is not shown is applied to the control gate 2 of the EEPROM cell. The cell is selected for example by the decoding of a base address of a memory zone which it protects. A read voltage of about 1.5 volts is then applied to the gate 2. Before the

selection a bit line 30, to which the cell is connected, is supplied by means of a generator 31 with a voltage of about 5 volts. A read circuit 20 (sensing circuit, in English publications), centred on a threshold voltage set between 0 and 5 volts, and in general the mean value 2.5 volts is taken, detects a "1" if the cell is in its initial state and a "0" if the cell is erased. In practice, if the the cell is in its initial state its threshold voltage is equal to zero volts. It behaves, at the time of selection, like a closed circuit. Under these conditions the voltage on the bit line 30 falls. This fall is detected in the circuit 20. On the other hand if the cell 1 has been erased it behaves like an open circuit whatever the command applied may be. A drop in voltage is then no longer detected. It is the data at the output of the detector 20 which validates or not the decoding of the memory zone.

It is thus possible to have a non-programmable EEPROM memory assembly in an integrated circuit, each cell blocking a specific function.

Figures 2.a and 2.b show a EEPROM cell which is never programmable in accordance with the invention. The EEPROM cell 1 is controlled on its control gate 2 by a voltage V_1 . Between the drain region 3 and the ground there is a voltage limiter 5 which limits the voltage between the drain and the ground to 5 volts. Between the source region 4 and the ground there is another voltage limiter 6 which plays the same role. In Figure 2.b the drain region 3 and source region 4 are regions of a given type of doping, N for example, in a substrate of the opposite type, P for example. The voltage limiter 5 or 6, respectively, is a Zener diode, preferably formed (Figure 2.b) by joining to the drain region 3 or source region 4, respectively, a region of opposite doping 7 or 8, respectively, outside the channel region 9. The regions of opposite doping 7 or 8 are connected to ground. The regions 7 and 8 have a doping of the same type as that of the substrate 11. If the cell is formed in an island, the regions 7 and 8 are doped with the same type of impurity as that in the island in which the cell is formed. Furthermore it is necessary that the regions should be more highly doped than the substrate, or the island if this is applicable.

In the example shown in Figure 2b the regions 7 and 8 have a P type doping.

In order to explain the physical effects employed it is necessary to recall the principles of erasure and programming of an EEPROM cell.

An EEPROM cell comprising an N type channel will be considered, for example. The said cell 1 is erased by bringing its control gate 2 to a very positive potential, of about 15 volts or more, and its drain region 3 to ground. Electrons are stored on the floating gate 10 as a result of the powerful electrical field thus created. They induce a potential barrier which opposes the formation of a conduction channel in the channel region 9. The threshold voltage of the cell is increased. Typically the threshold voltage reaches a value of about 5 volts.

In order to program an erased EEPROM cell the electrons are caused to leave the floating gate 10. In order to achieve this the control gate is brought to ground potential and the drain region is brought to a very positive potential, of about 15 volts or more. The electrons stored in the floating gate are then removed. The threshold voltage of the cell is decreased. Typically the threshold voltage then has a value of about -2 volts. This negative threshold voltage is produced because, in order to be sure that the cell has been properly programmed, the programming operation is continued for a time longer than that necessary to cause the departure of the electrons previously stored. In doing this, free electrons which contribute to the electrical neutrality of the material of the floating gate are also removed. In a way holes are formed in this manner.

In fact it is the difference in potential which is important because it establishes the direction of the electric field and thus the direction of movement of electrons. For programming it would therefore be possible to set the control gate at a very negative potential and the drain region at ground potential: the potential difference would be unchanged. However, in practice it is not possible to set the control

gate at a negative potential. because the control logic of the cells which is connected to the integrated circuit will always oppose this.

In certain cases it is possible to erase and to program the cell in the same manner by using the source region 4 instead of the drain region 3 because these two regions are not differentiated. This is the reason why, in the invention, a voltage limiter is put on each source region and drain region.

It should also be noted that it is possible to program the cell by exposing it to ultraviolet radiation. This is only possible if its floating gate is not protected by an optical mask. This optical mask may be formed for example by a metal layer 12 positioned above the integrated circuit.

If a voltage limiter 5 or 6 is located on the drain region 3 and the source region 4, respectively, electrical programming is prevented because it is no longer possible to apply a very positive potential on these regions, and it is not possible to apply a very negative potential on the control gate as has been shown above. If in addition a metal layer 12 is put on the control gate, programming by ultraviolet radiation is prevented. An EEPROM cell which can never be programmed is obtained.

The description and reasoning which has just been presented for an EEPROM cell having an N type channel region is similarly applicable to an EEPROM cell having a P type channel region, by reversing the polarities and the types of charges.

The voltage limiters 5 and 6, respectively, are for example Zener diodes formed as has already been shown above by joining the drain region 3 and the source region 4, respectively, to a region of opposite doping 7 and 8, respectively, outside the channel region 9. The regions of opposite doping 7 and 8 are connected to ground. A reverse polarized junction PN is obtained which can be shown to be a Zener diode characterized by a Zener voltage having a value of between 5 and 6

volts. In order to form the Zener diodes in practice, during the implantation of the doping, a slight covering may be allowed of the subsequently doped region (7 or 8) in the adjacent region (3 or 4) previously doped with an opposite type.



CLAIMS

1. A device for blocking access to all or part of an integrated circuit comprising an EEPROM cell (1) comprising a floating gate transistor (10), characterized in that the transistor is equipped with a voltage limiter (5, 6) on its drain region (3) and/or on its source region (4) and in that the EEPROM cell is never programmable.
2. A device as claimed in claim 1, characterized in that the voltage limiter on each source and/or drain region of the EEPROM cell is a Zener diode formed simply by joining to each source and drain region a region of opposite doping (7, 8) connected to ground and located outside the channel region (9) of the EEPROM cell.
3. A device as claimed in either one of claims 1 and 2, characterized in that it comprises a metal layer (12) on the control gate of the EEPROM cell to prevent programming of this EEPROM cell by the application of an ultraviolet radiation.
4. A device as claimed in claim 3, characterized in that it is integrated in the integrated circuit (11) the access to which it controls.