CLAIMS

1. A method of fabricating a semiconductor device, the method comprising:

etching high-aspect-ratio channels in a multi-layer stack disposed on a semiconductor substrate, the multi-layer stack comprising sets of oxide and non-oxide layers;

filling each of the high-aspect-ratio channels with an oxide using a thermal atomic layer deposition (ALD) process;

recess etching the oxide using a wet chemical etch to form recess-etched channels;

capping the recess-etched channels to refill an etched portion of the recess-etched channels with a conductive material,

wherein filling each of the high-aspect-ratio channels with an oxide includes:

depositing a silicon (Si) oxide in multiple blocks that each contains multiple growth cycles followed by a passivation operation, each of the growth cycles including: introduction of an inhibitor into a chamber in which the semiconductor substrate is disposed during an inhibition operation, followed by multiple thermal ALD deposition cycles, and

injecting H_2, O_2, Ar, and N_2 gasses and an aminosilane precursor during each ALD deposition cycle to deposit a sub-angstrom thickness of oxide per ALD deposition cycle.

2. The method of claim 1, wherein the inhibitor includes multiple gasses that each act as an inhibitor and the inhibition operation is maintained for less than 1s.

3. The method of claim 1, wherein recess etching the oxide includes etching the oxide using a dilute HF (DHF) etch of 100:1 HF: H_2O, the oxide having a relatively constant etch rate along a width and depth of each of the high-aspect-ratio channels.

4. The method of claim 1, further comprising maintaining, during the growth cycle, a temperature of a pedestal on which the semiconductor substrate is disposed of 550–650°C and a pressure in the chamber of 10-20 Torr.

5. The method of claim 1, further comprising injecting H_2, O_2, Ar, and N_2 gasses during each passivation operation to remove residual inhibitor and passivate an exposed surface of the Si oxide in each of the high-aspect-ratio channels, the passivation operation maintained for up to two minutes.

6. The method of claim 1, further comprising purging the chamber of gasses used in each growth cycle:

after the inhibition operation,

before and after the thermal ALD deposition cycles associated with the inhibition operation, and

after the passivation operation.

7. The method of claim 1, wherein filling each of the high-aspect-ratio channels with an oxide includes:

depositing a first thermal Si oxide ALD liner layer within each of the high aspect-ratio-channels to form a liner layer prior to depositing the Si oxide in a first of the blocks; and

depositing a second thermal Si oxide ALD liner layer after depositing the Si oxide within each of the high-aspect-ratio channels after a last of the blocks.

8. The method of claim 1, further comprising, for filling each of the high-aspect-ratio channels with the Si oxide:

determining a number of blocks, a number of growth cycles within each block and a number of thermal ALD deposition cycles within each growth cycle, at least one of which depends on critical dimensions of each of the high-aspect-ratio channels as well as a quality of a structure in which the Si oxide is to be deposited.

9. The method of claim 1, further comprising depositing alternating SiO_2 and SiN layers as the multi-layer stack.

10. The method of claim 1, wherein capping the recess-etched channels includes depositing polycrystalline Si (poly-Si) in the recess-etched channels using plasma-enhanced chemical vapor deposition.

11. The method of claim 10, further comprising:

growing a field oxide on the multi-layer stack prior to forming the high-aspect-ratio channels; and

planarizing the poly-Si to expose the field oxide, a top surface of the field oxide and a top surface of the poly-Si in each of the high-aspect-ratio channels lying in a plane after planarization of the poly-Si.

12. The method of claim 11, further comprising:

depositing an amount of the oxide sufficient to cover the field oxide; and

planarizing the oxide prior to recess etching the oxide such that a top surface of the field oxide and a top surface of the oxide in each of the high-aspect ratio-channels lie in a plane after planarization of the oxide.

13. A method of fabricating a semiconductor device, the method comprising:

etching high-aspect-ratio channels in a multi-layer stack disposed on a semiconductor substrate, the multi-layer stack comprising sets of silicon (Si) oxide and non-Si oxide layers;

depositing, in the high-aspect-ratio channels until each of the high-aspect-ratio channels is filled, a channel oxide in multiple blocks that each contains multiple growth cycles followed by a passivation operation, each of the growth cycles comprising:

introducing an inhibitor into a chamber in which the semiconductor substrate is disposed during an inhibition operation;

multiple thermal atomic layer deposition (ALD) deposition cycles, and

injecting H_2, O_2, Ar, and N_2 gasses and an aminosilane precursor during each ALD deposition cycle to deposit a sub-angstrom thickness of oxide per ALD deposition cycle;

recess etching the channel oxide to form recess-etched channels; and

capping each of the recess-etched channels with a cap to refill an etched portion of the recess-etched channels with a conductive material.

14. The method of claim 13, further comprising:

depositing a first thermal Si oxide ALD liner layer within each of the high aspect-ratio-channels to form a liner layer prior to depositing the Si oxide in a first of the blocks; and

depositing a second thermal Si oxide ALD liner layer after depositing the Si oxide within each of the high-aspect-ratio channels after a last of the blocks.

15. The method of claim 13, further comprising:

growing a field oxide on the multi-layer stack prior to forming the high-aspect-ratio channels; and

planarizing the cap to expose the field oxide, a top surface of the field oxide and a top surface of the cap in each of the high-aspect-ratio channels lying in a plane after the planarization.