

SOLID-STATE IMAGE PICKUP ELEMENT, SOLID-STATE IMAGE PICKUP DEVICE AND PRODUCTION METHOD THEREFOR

5

DESCRIPTION

TECHNICAL FIELD

[0001]

The present invention relates to a solid-state image pickup element, a solid-state image
10 pickup device and a production method therefor, and more particularly to a CCD solid-state
image pickup element, a CCD solid-state image pickup device and a production method therefor

BACKGROUND ART

[0002]

15 In a conventional solid-state image pickup device (solid-state image sensor) for use in a
video camera and others, a plurality of photodetection elements are arranged in a matrix array,
and a vertical charge-coupled device (VCCD) is provided between adjacent columns of the
photodetection elements to read signal charges generated in an associated one of the adjacent
columns of photodetection elements.

20 [0003]

A structure of the conventional solid-state image pickup device will be described below (see,
for example, the following Patent Document 1). FIG. 1 is a sectional view showing a unit pixel
of the conventional solid-state image pickup device. A photodiode (PD) in each unit pixel is
comprised of an n-type photoelectric conversion region 13 formed in a p-type well region 12
25 formed in an upper region of an n-type semiconductor substrate 11, to serve as a charge storage
layer, and a p⁺-type region 14 formed on the n-type photoelectric conversion region 13.

[0004]

An n-type CCD channel region 16 is also formed in the p-type well region 12 in the form of
an n-type impurity-doped region. A portion of the p-type well region 12 between the n-type

CCD channel region 16 and the photodiode from which signal charges are read out to the n-type
CCD channel region 16 is formed as a p-type impurity-doped region to provide a read channel.
Thus, signal charges generated in the photodiode are temporarily stored in the n-type
photoelectric conversion region 13, and then read out to the n-type CCD channel region 16 via
5 the read channel.

[0005]

Further, a p+-type element isolation region 15 is provided between the n-type CCD channel
region 16 and another adjacent photodiode. Based on the p+-type element isolation region 15,
the n-type CCD channel region 16 is electrically isolated from the adjacent photodiode, and the
10 n-type CCD channel region 16 are isolated from another adjacent n-type CCD channel region.

[0006]

A transfer electrode 18 is formed on a surface of the semiconductor substrate through a Si
oxide film 17 to extend in a horizontal direction and pass through between the photodiode and
the adjacent photodiode. Thus, in the solid-state image pickup device, when a read signal is
15 applied to a selected one of the transfer electrodes 18, the read channel located just below the
selected transfer electrode 18 is effected to allow signal charges generated in the photodiode
associated with the read channel to be read out to the corresponding n-type CCD channel region
16 therethrough.

[0007]

20 A metal shield film 20 is formed on the surface of the semiconductor substrate having the
transfer electrodes 18. The metal shielding film 20 has a plurality of metal-shield-film
openings 24 each provided as a light transmission portion on a photodiode-by-photodiode basis
to transmit therethrough light to be received by the p+-type region 14 serving as a light-receiving
section.

25 [0008]

[Patent Document 1] JP 2000-101056A

DISCLOSER OF THE INVENTION

[PROBLEM TO BE SOLVED BY THE INVENTION]

[0009]

As above, in the conventional solid-state image pickup element, the photodiode (PD), the read channel, the n-type CCD channel region and the p+-type element isolation region are formed in one plane, and thereby there is a limit to an increase in ratio of a surface area of a light-receiving section (photodiode) to the overall surface area of one pixel. It is therefore an object of the present invention to provide a solid-state image pickup element capable of reducing an area of a read channel to increase a ratio of a surface area of a light-receiving section (photodiode) to the overall surface area of one pixel.

[MEANS FOR SOLVING THE PROBLEM]

[0010]

In order to achieve the above object, according to a first object of the present invention, there is provided a solid-state image pickup element which comprises: a second-conductive type planar semiconductor layer; a first-conductive type planar semiconductor layer formed on the second-conductive type planar semiconductor layer; a hole portion formed in the first-conductive type planar semiconductor layer to define a hole therein; a first-conductive type high-concentration impurity region formed in a bottom wall of the hole portion of the first-conductive type planar semiconductor layer; a first-conductive type high-concentration impurity-doped element isolation region formed in a part of a sidewall of the hole portion of the first-conductive type planar semiconductor layer, and connected to the first-conductive type high-concentration impurity region; a second-conductive type photoelectric conversion region formed in a portion of the first-conductive type planar semiconductor layer located beneath the first-conductive type high-concentration impurity region and in a part of a lower region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer, and adapted to undergo a change in charge amount upon receiving light; a transfer electrode formed on the sidewall of the hole portion of the first-conductive type planar semiconductor layer through a gate dielectric film; a second-conductive type CCD channel region formed in a top surface of the first-conductive type planar semiconductor layer and in a part of an upper region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer; and a read channel formed in a region of the

first-conductive type planar semiconductor layer sandwiched between the second-conductive type photoelectric conversion region and the second-conductive type CCD channel region.

[0011]

According a second aspect of the present invention, there is provided a solid-state image pickup device which comprises a plurality of the above solid-state image pickup elements, wherein the solid-state image pickup elements are arranged in a matrix array.

[0012]

Preferably, the solid-state image pickup device according to the second aspect of the present invention includes: a plurality of the second-conductive type CCD channel regions made up of a plurality of second-conductive type impurity regions each extending in a column direction at least in a region between adjacent ones of a plurality of columns of the hole portions formed in the first-conductive type planar semiconductor layer; and a plurality of the first-conductive type high-concentration impurity-doped element isolation regions each arranged to prevent contact between adjacent ones of the second-conductive type CCD channel regions.

[0013]

Preferably, the above solid-state image pickup device includes a plurality of the transfer electrodes each formed to extend in a row direction in a region between adjacent ones of a plurality of rows of the hole portions formed in the first-conductive type planar semiconductor layer, and arranged along and in spaced-apart relation to the associated second-conductive type CCD channel region by a given distance to transfer therethrough signal charges generated in the associated solid-state image pickup element.

[0014]

According to a third aspect of the present invention, there is provided a solid-state image pickup device which comprises a plurality of element line groups each consisting of a first solid-state image pickup element line and a second solid-state image pickup element line, wherein the first solid-state image pickup element line consists of a plurality of the above solid-state image pickup elements which are arranged in a first direction at intervals of a first distance, and the second solid-state image pickup element line consists of a plurality of the above solid-state image pickup elements which are arranged in the first direction at intervals of the first

distance and in displaced relation to the first solid-state image pickup element line in the first direction by a given distance, and wherein the first and second solid-state image pickup element lines in each of the element line groups are arranged in a second direction perpendicular to the first direction at intervals of a second distance, and the element line groups are arranged in the second direction at interval of the second distance and in displaced relation to each other in the first direction.

[0015]

Preferably, the solid-state image pickup device according to the third aspect of the present invention includes: a plurality of the second-conductive type CCD channel regions made up of a plurality of second-conductive type impurity regions each extending in a column direction at least in a region between adjacent ones of a plurality of columns of the hole portions formed in the first-conductive type planar semiconductor layer, while passing through the respective hole portions in the adjacent columns; and a plurality of the first-conductive type high-concentration impurity-doped element isolation regions arranged to prevent contact between adjacent ones of the second-conductive type CCD channel regions.

[0016]

Preferably, the above solid-state image pickup device includes a plurality of the transfer electrodes each formed to extend in a row direction in a region between adjacent ones of a plurality of rows of the hole portions formed in the first-conductive type planar semiconductor layer, while passing through the respective hole portions in the adjacent rows, wherein the transfer electrodes are arranged in spaced-apart relation to each other by a given distance to allow signal charges generated in each of the solid-state image pickup elements, to be transferred along an associated one of the second-conductive type CCD channel regions.

[0017]

According to a fourth aspect of the present invention, there is provided a method of producing a solid-state image pickup element, comprising the steps of: forming a hole portion defining a hole therein, in a first-conductive type planar semiconductor layer formed on a second-conductive type planar semiconductor layer; forming a first-conductive type high-concentration impurity region in a bottom wall of the hole portion of the first-conductive

type planar semiconductor layer; forming a first-conductive type high-concentration impurity-doped element isolation region in a part of a sidewall of the hole portion of the first-conductive type planar semiconductor layer; forming a second-conductive type photoelectric conversion region adapted to undergo a change in charge amount upon receiving
5 light, in a portion of the first-conductive type planar semiconductor layer located beneath the first-conductive type high-concentration impurity region and in a part of a lower region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer; forming a transfer electrode on the sidewall of the hole portion of the first-conductive type planar semiconductor layer through a gate dielectric film; forming a
10 second-conductive type CCD channel region in an top surface of the first-conductive type planar semiconductor layer and in a part of an upper region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer; and forming a read channel in a region of the first-conductive type planar semiconductor layer sandwiched between the second-conductive type photoelectric conversion region and the second-conductive type CCD
15 channel region.

[0018]

Preferably, in the method of the present invention, the step of forming a hole portion includes forming a mask on the first-conductive type planar semiconductor layer formed on the second-conductive type planar semiconductor layer, and etching the first-conductive type planar
20 semiconductor layer to form the hole portion therein.

[0019]

Preferably, in the above method, the step of forming a second-conductive type photoelectric conversion region includes the sub-steps of: forming a masking material on the sidewall of the hole portion of the first-conductive type planar semiconductor layer; and forming the
25 second-conductive type photoelectric conversion region by an ion-implantation process.

[0020]

Preferably, in the above method, the step of forming a first-conductive type high-concentration impurity region is performed after the sub-step of forming the second-conductive type photoelectric conversion region by an ion-implantation process.

[0021]

Preferably, the above method further comprises the step of, after the sub-step of forming the second-conductive type photoelectric conversion region by an ion-implantation process, removing a part of the masking material formed on the sidewall of the hole portion of the first-conductive type planar semiconductor layer, wherein each of the step of forming a first-conductive type high-concentration impurity region and the step of forming a first-conductive type high-concentration impurity-doped element isolation region is performed by an ion-implantation process after the step of removing a part of the masking material.

[0022]

Preferably, in the method of the present invention, the step of forming a second-conductive type CCD channel region includes the sub-steps of: forming a masking material on the hole portion of the first-conductive type planar semiconductor layer; and forming the second-conductive type CCD channel region by an ion-implantation process.

[0023]

Preferably, in the above method, the step of forming a first-conductive type high-concentration impurity-doped element isolation region includes the sub-steps of: forming a masking material in such a manner as to allow the first-conductive type high-concentration impurity-doped element isolation region to be formed in connected relation to the first-conductive type high-concentration impurity-doped element isolation region (first-conductive type high-concentration impurity region) by an ion-implantation process; and forming the first-conductive type high-concentration impurity-doped element isolation region by the ion-implantation process.

[0024]

Preferably, in the method of the present invention, the step of forming a transfer electrode including the sub-steps of: forming the gate dielectric film on a surface of the first-conductive type planar semiconductor layer; depositing a gate electrode material on the gate dielectric film; flattening the gate electrode material; and etching the flattened gate electrode material to form the transfer electrode.

[EFFECT OF THE INVENTION]

[0025]

In the conventional CCD solid-state image pickup element, the photodiode (PD), the read channel, the n-type CCD channel region and the p+-type element isolation region are formed in one plane, and thereby there is a limit to an increase in ratio of a surface area of a light-receiving section (photodiode) to the overall surface area of one pixel, as mentioned above. In the present invention, a read channel can be arranged in a non-horizontal direction to provide a solid-state image pickup element capable of drastically reducing an occupancy area of the read channel to increase a ratio of a surface area of a light-receiving section (photodiode) to the overall surface area of one pixel.

BEST MODE FOR CARRYING OUT THE INVENTION

[0026]

With reference to the accompanying drawings, the present invention will now be specifically described based on an embodiment thereof.

[0027]

(FIRST EMBODIMENT)

FIGS. 2 and 3 are, respectively, a top plan view and a bird's-eye view showing a solid-state image pickup device comprising a plurality of CCD solid-state image pickup elements according to a first embodiment of the present invention which are arranged in an one-row $\times$ two column array. FIGS. 4 and 5 are a sectional view taken along the line X₁-X₁' in FIG. 2 and a sectional view taken along the line Y₁-Y₁' in FIG. 2, respectively.

[0028]

In the solid-state image pickup device, a p-type well region 114 is formed in an upper region of an n-type substrate 115, and a silicon hole portion 203 is formed in the p-type well region 114 to define a hole therein. A p+-type region 104 is formed in a bottom wall of the silicon hole portion 203, and a p+-type element isolation region 101 is formed in a part of a sidewall of the silicon hole portion 203 in connected relation to the p+-type region 104. An n-type photoelectric conversion region 110 is formed in a portion of the p-type well region 114 located beneath the p+-type region 104 and in a part of a lower portion of the sidewall of the

silicon hole portion 203, and two transfer electrodes 106, 107 are formed on the sidewall of the silicon hole portion 203 through a gate dielectric film 117. An n-type CCD channel region 103 is formed in a top surface of the p-type well region 114 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 203, and a read channel 112 is formed in a region of the p-type well region 114 sandwiched between the n-type photoelectric conversion region 110 and the n-type CCD channel region 103.

Further, a silicon hole portion 204 is formed in the p-type well region 114 to define a hole therein. A p+-type region 105 is formed in a bottom wall of the silicon hole portion 204, and a p+-type element isolation region 102 is formed in a part of a sidewall of the silicon hole portion 204 in connected relation to the p+-type region 105. An n-type photoelectric conversion region 111 is formed in a portion of the p-type well region 114 located beneath the p+-type region 105 and in a part of a lower portion of the sidewall of the silicon hole portion 204, and the transfer electrodes 106, 107 are also formed on the sidewall of the silicon hole portion 204 through the gate dielectric film 117. An n-type CCD channel region 109 is formed in a top surface of the p-type well region 114 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 204, and a read channel 113 is formed in a region of the p-type well region 114 sandwiched between the n-type photoelectric conversion region 111 and the n-type CCD channel region 109.

[0029]

The p+-type element isolation region 101 is formed between the n-type CCD channel regions 108, 103 to prevent contact therebetween. The p+-type element isolation region 102 is also formed between the n-type CCD channel regions 103, 108 to prevent contact therebetween.

[0030]

A metal shield film 116 is formed above the transfer electrodes 106, 107 and on the sidewalls of the silicon hole portions 203, 204, through a dielectric film 119.

[0031]

In the above solid-state image pickup device, when a read signal is applied to the transfer electrode 106 (or 107), signal charges stored in the n-type photoelectric conversion region 110 (or 111) serving as a charge storage layer are read out to the n-type CCD channel region 103 (or

108) via the read channel 112 (or 113). The readout signal charges are transferred in a vertical (Y_1 - Y_1') direction through the transfer electrode 106 (or 107).

[0032]

(SECOND EMBODIMENT)

5 FIGS. 26 and 27 are, respectively, a fragmentary top plan view and a fragmentary bird's-eye view showing a solid-state image pickup device according to a second embodiment of the present invention, wherein a plurality of CCD solid-state image pickup elements each having fundamentally the same structure as that of the CCD solid-state image pickup element according to the first embodiment are arranged in a matrix array. FIGS. 28 and 29 are a sectional view
10 taken along the line X_3 - X_3' in FIG. 26 and a sectional view taken along the line Y_3 - Y_3' in FIG. 26, respectively. The solid-state image pickup device according to the second embodiment generally has a symmetrical arrangement. Thus, the following description will be made primarily about only an area illustrated in FIGS. 26 and 27.

[0033]

15 As shown in FIGS. 26 and 27, a solid-state image pickup element having a p+-type region 501 and a solid-state image pickup element having a p+-type region 502 are arranged on a semiconductor substrate in a vertical (Y_3 - Y_3') direction (column direction) at given intervals (vertical pixel pitches VP) to form a first solid-state image pickup element column. Further, a
20 solid-state image pickup element having a p+-type region 503 and a solid-state image pickup element having a p+-type region 504 are arranged on the semiconductor substrate in the vertical direction at the same intervals (same vertical pixel pitches VP) as those in the first solid-state image pickup element column, in adjacent relation to and at the same vertical (column-wise) positions as corresponding ones of the solid-state image pickup elements in the first solid-state image pickup element column, to form a second solid-state image pickup element column. The
25 first solid-state image pickup element column and the second solid-state image pickup element column are arranged in spaced-apart relation to each other in a row direction by the same distance (horizontal pixel pitch HP) as the vertical pixel pitch VP. In this manner, the solid-state image pickup elements having the p+-type regions 501, 502, 503, 504 are arranged in a so-called matrix array.

[0034]

An n-type CCD channel region 508 is provided between corresponding ones of two silicon hole portions 530, 532 in the first solid-state image pickup element column and two silicon hole portions 531, 533 in the second solid-state image pickup element column arranged adjacent to the first solid-state image pickup element column, to read signal charges generated in a photodiode having the p+-type region 501 and a photodiode having the p+-type region 502, and transfer the readout signal charges in the vertical direction. In the same manner, two n-type CCD channel regions 507, 509 are provided to transfer signal charges generated in other photodiodes in the vertical direction.

Each of the n-type CCD channel regions is formed to extend between the silicon hole portions arranged in a matrix array, in the vertical direction. Two p+-type element isolation regions 505, 506 are provided to isolate adjacent ones of the n-type CCD channel regions from each other without contact therebetween.

The p+-type element isolation region 505 is also formed in a part of sidewalls of the silicon hole portions 530, 532 in connected relation to the p+-type regions 501, 502 to apply a voltage to the p+-type regions 501, 502.

The p+-type element isolation region 506 is also formed in a part of sidewalls of the silicon hole portions 531, 533 in connected relation to the p+-type regions 503, 504 to apply a voltage to the p+-type regions 503, 504.

In the second embodiment, each of the p+-type element isolation regions 505, 506 is provided along an axis of an associated one of the first and second solid-state image pickup element columns and a part of outer peripheries of associated ones of the silicon hole portions. Alternatively, as long as each of the p+-type element isolation regions is provided to prevent contact between adjacent ones of the n-type CCD channel regions, and formed as a part of the sidewalls of associated ones of the silicon hole portions in connected relation to associated ones of the p+-type regions, it may be arranged at any suitable position other than that in FIG. 25, such as a position displaced from that in FIG. 25 in an X₃ direction.

[0035]

Three transfer electrodes 512, 513, 514 are provided between each of the silicon hole

portions 530, 531 in a first solid-state image pickup element row where the solid-state image pickup element having the p⁺-type region 501 and the solid-state image pickup element having the p⁺-type region 503 are arranged in a horizontal (X_2 - X_2') direction (row direction), and a corresponding one of the silicon hole portions 532, 533 in a second solid-state image pickup element row where the solid-state image pickup element having the p⁺-type region 502 and the solid-state image pickup element having the p⁺-type region 504 are arranged in the horizontal direction, to transfer signal charges read out from associated ones of the photodiodes to the n-type CCD channel regions 507, 508, 509, in the vertical direction.

Further, four transfer electrodes 510, 511, 515, 516 are provided to transfer signal charges read out from other photodiodes to the n-type CCD channel regions 507, 508, 509, in the vertical direction. When a read signal is selectively applied, for example, to the transfer electrode 514, signal charges stored in the photodiodes having the p⁺-type regions 502, 504 are read out to the n-type CCD channel regions 508, 509 via respective associated read channels. Each of the transfer electrodes is formed to extend in the horizontal direction and between the silicon hole portions arranged in the matrix array.

[0036]

In the solid-state image pickup element having the p⁺-type region 501, a p-type well region 525 is formed in an upper region of an n-type substrate 526, and the silicon hole portion 530 is formed in the p-type well region 525 to define a hole therein. The p⁺-type region 501 is formed in a bottom wall of the silicon hole portion 530, and the p⁺-type element isolation region 505 is formed in a part of the sidewall of the silicon hole portion 530 in connected relation to the p⁺-type region 501. An n-type photoelectric conversion region 517 is formed in a portion of the p-type well region 523 located beneath the p⁺-type region 501 and in a part of a lower portion of the sidewall of the silicon hole portion 530, and the transfer electrodes 511, 512 are formed on the sidewall of the silicon hole portion 530 through a gate dielectric film 527. The n-type CCD channel region 508 is formed in a top surface of the p-type well region 525 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 530, and the read channel 521 is formed in a region of the p-type well region 525 sandwiched between the n-type photoelectric conversion region 517 and the n-type CCD channel region 508.

In the solid-state image pickup element having the p+-type region 502, the silicon hole portion 532 is formed in the p-type well region 525 to define a hole therein. The p+-type region 502 is formed in a bottom wall of the silicon hole portion 532, and the p+-type element isolation region 505 is formed in a part of a sidewall of the silicon hole portion 532 in connected relation to the p+-type region 502. An n-type photoelectric conversion region 518 is formed in a portion of the p-type well region 525 located beneath the p+-type region 502 and in a part of a lower portion of the sidewall of the silicon hole portion 532, and the transfer electrodes 514, 515 are also formed on the sidewall of the silicon hole portion 532 through the gate dielectric film 527. The n-type CCD channel region 508 is formed in a top surface of the p-type well region 525 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 532, and the read channel 522 is formed in a region of the p-type well region 525 sandwiched between the n-type photoelectric conversion region 518 and the n-type CCD channel region 508.

In the solid-state image pickup element having the p+-type region 503, the silicon hole portion 531 is formed in the p-type well region 525 to define a hole therein. The p+-type region 503 is formed in a bottom wall of the silicon hole portion 531, and the p+-type element isolation region 506 is formed in a part of a sidewall of the silicon hole portion 531 in connected relation to the p+-type region 503. An n-type photoelectric conversion region 519 is formed in a portion of the p-type well region 525 located beneath the p+-type region 503 and in a part of a lower portion of the sidewall of the silicon hole portion 531, and the transfer electrodes 511, 512 are also formed on the sidewall of the silicon hole portion 531 through the gate dielectric film 527. The n-type CCD channel region 509 is formed in a top surface of the p-type well region 525 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 531, and the read channel 523 is formed in a region of the p-type well region 525 sandwiched between the n-type photoelectric conversion region 519 and the n-type CCD channel region 509.

In the solid-state image pickup element having the p+-type region 504, the silicon hole portion 533 is formed in the p-type well region 525 to define a hole therein. The p+-type region 504 is formed in a bottom wall of the silicon hole portion 533, and the p+-type element isolation

region 506 is formed in a part of a sidewall of the silicon hole portion 533 in connected relation to the p+-type region 504. An n-type photoelectric conversion region 520 is formed in a portion of the p-type well region 525 located beneath the p+-type region 504 and in a part of a lower portion of the sidewall of the silicon hole portion 533, and the transfer electrodes 514, 515 are also formed on the sidewall of the silicon hole portion 533 through the gate dielectric film 527. The n-type CCD channel region 509 is formed in a top surface of the p-type well region 525 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 533, and the read channel 524 is formed in a region of the p-type well region 525 sandwiched between the n-type photoelectric conversion region 520 and the n-type CCD channel region 509.

[0037]

A metal shield film 529 is formed above the transfer electrodes 510, 511, 512, 513, 514, 515, 516 and on the sidewalls of the silicon hole portions 501, 502, 503, 504 through a dielectric film 528.

[0038]

As above, each of the transfer electrode 510, 511, 512, 513, 514, 515, 516 is formed to extend in the row direction in a region between the silicon hole portions in adjacent ones of the solid-state image pickup element rows, while passing through the respective silicon hole portions in the adjacent solid-state image pickup element rows, wherein the transfer electrode are arranged in spaced-apart relation to each other by a given distance. Each of the transfer electrodes 511, 512, 514, 515 located adjacent to associated ones of the silicon hole portions is formed on the sidewall of the associated silicon wall through the gate dielectric film. In cooperation with the n-type CCD channel regions, the transfer electrode 510, 511, 512, 513, 514, 515, 516 make up a vertical charge transfer device (VCCD) for transferring signal charges generated in the photodiodes in the vertical direction. The VCCD is configured as a three-phase driven type ($\phi 1$ to $\phi 3$) in which three transfer electrodes are provided in each of the photodiodes, and adapted to be driven in respective different phases so as to transfer signal charges generated in the photodiode, in the vertical direction. Although the VCCD in the second embodiment is a three-phase driven type, it is apparent to those skilled in the art that the

VCCD may be configured to be driven in any other suitable number of phases.

[0039]

(THIRD EMBODIMENT)

In the second embodiment, a solid-state image pickup device comprising a plurality of CCD
5 image pickup elements arranged in a matrix array has been shown and described. Alternatively,
as shown in FIGS. 22, 23, 24 and 25, the solid-state image pickup elements may be arranged in a
honeycomb array. In this connection, as a third embodiment of the present invention, a
solid-state image pickup device will be described in which a plurality of CCD image pickup
elements each having fundamentally the same structure as that of the CCD solid-state image
10 pickup element according to the first embodiment are arranged in a honeycomb array. FIGS. 22
and 23 are, respectively, a fragmentary top plan view and a fragmentary bird's-eye view showing
a solid-state image pickup device comprising a plurality of CCD image pickup elements
arranged in a honeycomb array. FIGS. 24 and 25 are a sectional view taken along the line
 X_2-X_2' in FIG. 22 and a sectional view taken along the line Y_2-Y_2' in FIG. 22, respectively. The
15 solid-state image pickup device according to the third embodiment generally has a symmetrical
arrangement. Thus, the following description will be made primarily about only an area
illustrated in FIGS. 22 and 23.

[0040]

As shown in FIGS. 22 and 23, a solid-state image pickup element having a p+-type region
20 301 and a solid-state image pickup element having a p+-type region 302 are arranged on a
semiconductor substrate in a vertical (Y_2-Y_2') direction (column direction) at given intervals
(vertical pixel pitches VP) to form a first solid-state image pickup element column.

Further, a solid-state image pickup element having a p+-type region 303 and a solid-state
image pickup element having 304 are arranged on the semiconductor substrate in the vertical
25 direction at the same intervals (same vertical pixel pitches VP) as those in the first solid-state
image pickup element column, in spaced-apart relation to the first solid-state image pickup
element column in a direction perpendicular to the vertical direction (i.e., horizontal direction)
by $1/2$ of a horizontal pixel pitch HP equal to the vertical pixel pitch and in displaced relation to
the first solid-state image pickup element column in the vertical direction by $1/2$ of the vertical

pixel pitch, to form a second solid-state image pickup element column.

Further, a solid-state image pickup element having a p+-type region 305 and a solid-state image pickup element having 306 are arranged on the semiconductor substrate in the vertical direction at the same intervals (same vertical pixel pitches VP) as those in the first solid-state image pickup element column, in spaced-apart relation to the second solid-state image pickup element column in the horizontal direction by $1/2$ of a horizontal pixel pitch HP equal to the vertical pixel pitch and in displaced relation to the second solid-state image pickup element column in the vertical direction by $1/2$ of the vertical pixel pitch, to form a third solid-state image pickup element column.

In this manner, the solid-state image pickup elements having the p+-type regions 301, 302, 303, 304, 305, 306 are arranged in a honeycomb array.

[0041]

An n-type CCD channel region 331 is provided between corresponding ones of two silicon hole portions 339, 331 in the first solid-state image pickup element column and two silicon hole portions 334, 333 in the second solid-state image pickup element column arranged adjacent to the first solid-state image pickup element column, to read signal charges generated in a photodiode having the p+-type region 301 and a photodiode having the p+-type region 302, and transfer the readout signal charges in the vertical direction.

In the same manner, an n-type CCD channel region 312 is provided between corresponding ones of two silicon hole portions 334, 333 in the second solid-state image pickup element column and two silicon hole portions 305, 306 in the third solid-state image pickup element column to read signal charges generated in a photodiodes having the p+-type region 303 and a photodiodes having the p+-type region 304, and transfer the readout signal charges in the vertical direction.

Further, an n-type CCD channel region 313 is provided to read signal charges generated in a photodiode having the p+-type region 305 and a photodiode having the p+-type region 306, and transfer the readout signal charges in the vertical direction.

An n-type CCD channel region 310 is provided to read signal charges generated in other photodiodes and transfer the readout signal charges in the vertical direction.

Each of the n-type CCD channel regions is formed to extend between the silicon hole portions arranged in a honeycomb array, in the vertical direction in a meandering pattern. Further, three p+-type element isolation regions 307, 308, 309 are provided to isolate adjacent ones of the n-type CCD channel regions from each other without contact therebetween.

5 The p+-type element isolation region 307 is also formed in a part of sidewalls of the silicon hole portions 339, 331 in connected relation to the p+-type regions 301, 302 to apply a voltage to the p+-type regions 301, 302.

 The p+-type element isolation region 308 is also formed in a part of sidewalls of the silicon hole portions 334, 333 in connected relation to the p+-type regions 303, 304 to apply a voltage to
10 the p+-type regions 303, 304.

 The p+-type element isolation region 309 is also formed in a part of sidewalls of the silicon hole portions 343, 332 in connected relation to the p+-type regions 305, 306 to apply a voltage to the p+-type regions 305, 305.

 In the third embodiment, each of the p+-type element isolation regions 307, 308, 309 is
15 provided along an axis of an associated one of the first to third solid-state image pickup element columns and a part of outer peripheries of associated ones of the silicon hole portions. Alternatively, as long as each of the p+-type element isolation regions is provided to prevent contact between adjacent ones of the n-type CCD channel regions, and formed as a part of the sidewalls of associated ones of the silicon hole portions in connected relation to associated ones
20 of the p+-type regions, it may be arranged at any suitable position other than that in FIG. 21, such as a position displaced from that in FIG. 21 in an X_2 direction.

[0042]

 Two transfer electrodes 314, 315 are provided between each of the silicon hole portions 339, 343 in a first solid-state image pickup element row where the solid-state image pickup element
25 having the p+-type region 301 and the solid-state image pickup element having the p+-type region 303 are arranged in a horizontal (X_2 - X_2') direction (row direction), and the silicon hole portion 334 in a second solid-state image pickup element row where the solid-state image pickup element having the p+-type region 303 and other solid-state image pickup element having a p+-type regions (not shown) are arranged in the horizontal direction.

Further, two transfer electrodes 316, 317 are provided between the silicon hole portion 334 in the second solid-state image pickup element row, and each of the silicon hole portions 331, 332 in a third solid-state image pickup element row where the solid-state image pickup element having the p+-type region 302 and the solid-state image pickup element having the p+-type region 306 are arranged in the horizontal direction, and two transfer electrodes 318, 319 are provided between each of the silicon hole portions 331, 332 in the third solid-state image pickup element row, and the silicon hole portion 333 in a fourth solid-state image pickup element row where the solid-state image pickup element having the p+-type region 304 and other solid-state image pickup element having a p+-type regions (not shown) are arranged in the horizontal direction. Each of the transfer electrodes is formed to extend in the horizontal direction and between the silicon hole portions arranged in the honeycomb array, in a meandering pattern.

[0043]

In the solid-state image pickup element having the p+-type region 301, a p-type well region 320 is formed in an upper region of an n-type substrate 321, and the silicon hole portion 339 is formed in the p-type well region 320 to define a hole therein. The p+-type region 301 is formed in a bottom wall of the silicon hole portion 339, and the p+-type element isolation region 307 is formed in a part of the sidewall of the silicon hole portion 339 in connected relation to the p+-type region 301. An n-type photoelectric conversion region 322 is formed in a portion of the p-type well region 320 located beneath the p+-type region 301 and in a part of a lower portion of the sidewall of the silicon hole portion 339, and the transfer electrode 314 is formed on the sidewall of the silicon hole portion 339 through a gate dielectric film 328. The n-type CCD channel region 311 is formed in a top surface of the p-type well region 320 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 339, and the read channel 304 is formed in a region of the p-type well region 320 sandwiched between the n-type photoelectric conversion region 322 and the n-type CCD channel region 311.

In the solid-state image pickup element having the p+-type region 302, the silicon hole portion 331 is formed in the p-type well region 320 to define a hole therein. The p+-type region 302 is formed in a bottom wall of the silicon hole portion 331, and the p+-type element isolation region 307 is formed in a part of a sidewall of the silicon hole portion 331 in connected relation

to the p⁺-type region 302. An n-type photoelectric conversion region 323 is formed in a portion of the p-type well region 320 located beneath the p⁺-type region 302 and in a part of a lower portion of the sidewall of the silicon hole portion 331, and the transfer electrodes 317, 318 are also formed on the sidewall of the silicon hole portion 331 through the gate dielectric film 328. The n-type CCD channel region 311 is formed in a top surface of the p-type well region 320 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 331, and the read channel 335 is formed in a region of the p-type well region 320 sandwiched between the n-type photoelectric conversion region 323 and the n-type CCD channel region 311.

In the solid-state image pickup element having the p⁺-type region 303, the silicon hole portion 334 is formed in the p-type well region 320 to define a hole therein. The p⁺-type region 303 is formed in a bottom wall of the silicon hole portion 334, and the p⁺-type element isolation region 308 is formed in a part of a sidewall of the silicon hole portion 334 in connected relation to the p⁺-type region 303. An n-type photoelectric conversion region 324 is formed in a portion of the p-type well region 320 located beneath the p⁺-type region 303 and in a part of a lower portion of the sidewall of the silicon hole portion 334, and the transfer electrodes 315, 316 are also formed on the sidewall of the silicon hole portion 334 through the gate dielectric film 328. The n-type CCD channel region 312 is formed in a top surface of the p-type well region 320 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 334, and the read channel 338 is formed in a region of the p-type well region 320 sandwiched between the n-type photoelectric conversion region 324 and the n-type CCD channel region 312.

In the solid-state image pickup element having the p⁺-type region 304, the silicon hole portion 333 is formed in the p-type well region 320 to define a hole therein. The p⁺-type region 304 is formed in a bottom wall of the silicon hole portion 333, and the p⁺-type element isolation region 308 is formed in a part of a sidewall of the silicon hole portion 333 in connected relation to the p⁺-type region 304. An n-type photoelectric conversion region 325 is formed in a portion of the p-type well region 320 located beneath the p⁺-type region 304 and in a part of a lower portion of the sidewall of the silicon hole portion 333, and the transfer electrode 319 is

also formed on the sidewall of the silicon hole portion 333 through the gate dielectric film 328. The n-type CCD channel region 312 is formed in a top surface of the p-type well region 320 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 333, and the read channel 337 is formed in a region of the p-type well region 320 sandwiched
5 between the n-type photoelectric conversion region 325 and the n-type CCD channel region 312.

In the solid-state image pickup element having the p+-type region 305, the silicon hole portion 343 is formed in the p-type well region 320 to define a hole therein. The p+-type region 305 is formed in a bottom wall of the silicon hole portion 343, and the p+-type element isolation region 309 is formed in a part of a sidewall of the silicon hole portion 343 in connected relation
10 to the p+-type region 305. An n-type photoelectric conversion region 326 is formed in a portion of the p-type well region 320 located beneath the p+-type region 305 and in a part of a lower portion of the sidewall of the silicon hole portion 343, and the transfer electrode 314 is also formed on the sidewall of the silicon hole portion 343 through the gate dielectric film 328. The n-type CCD channel region 313 is formed in a top surface of the p-type well region 320 and
15 in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 343, and the read channel 341 is formed in a region of the p-type well region 320 sandwiched between the n-type photoelectric conversion region 326 and the n-type CCD channel region 313.

In the solid-state image pickup element having the p+-type region 306, the silicon hole portion 332 is formed in the p-type well region 320 to define a hole therein. The p+-type region
20 306 is formed in a bottom wall of the silicon hole portion 332, and the p+-type element isolation region 309 is formed in a part of a sidewall of the silicon hole portion 332 in connected relation to the p+-type region 306. An n-type photoelectric conversion region 327 is formed in a portion of the p-type well region 320 located beneath the p+-type region 306 and in a part of a lower portion of the sidewall of the silicon hole portion 332, and the transfer electrodes 317, 318
25 are also formed on the sidewall of the silicon hole portion 332 through the gate dielectric film 328. The n-type CCD channel region 313 is formed in a top surface of the p-type well region 320 and in a part of an upper region of the remaining part of the sidewall of the silicon hole portion 332, and the read channel 336 is formed in a region of the p-type well region 320 sandwiched between the n-type photoelectric conversion region 327 and the n-type CCD channel

region 313.

[0044]

A metal shield film 330 is formed above the transfer electrodes 314, 315, 316, 317, 318, 319 and on the sidewalls of the silicon hole portions 339, 331, 334, 333, 332 through a dielectric film 329.

[0045]

As above, each of the transfer electrode 314, 315, 316, 317, 318, 319 is formed to extend in the row direction in a region between the silicon hole portions in adjacent ones of the solid-state image pickup element rows, while passing through the respective silicon hole portions in the adjacent solid-state image pickup element rows. Each of the transfer electrodes 314, 315, 316, 317, 318, 319 is formed on the sidewall of the associated silicon wall through the gate dielectric film, and the transfer electrodes 314, 315, 316, 317, 318, 319 are arranged in spaced apart relation to each other by a given distance. In cooperation with the n-type CCD channel regions, the transfer electrode 314, 315, 316, 317, 318, 319 make up a vertical charge transfer device (VCCD) for transferring signal charges generated in the photodiodes in the vertical direction. The VCCD is configured as a four-phase driven type ($\phi 1$ to $\phi 4$) in which four transfer electrodes are provided in each of the photodiodes, and adapted to be driven in respective different phases so as to transfer signal charges generated in the photodiode, in the vertical direction. Although the VCCD in the third embodiment is a four-phase driven type, it is apparent to those skilled in the art that the VCCD may be configured to be driven in any other suitable number of phases.

[0046]

Although not illustrated, as with conventional CCD image sensors, a color filter, a microlens and others are formed on the metal shield film 330 through a protective film and a flattened film.

[0047]

With reference to FIGS. 6(a) to 21(b), one example of a process of producing the solid-state image pickup element (the solid-state image pickup device) according to the above embodiments will be described below.

[0048]

In FIGS. 6(a) to 21(b), each figure suffixed by (a) and each figure suffixed by (b) corresponds to a cross-section taken along the line X₁-X₁' in FIG. 2 and a cross-section taken along the line Y₁-Y₁' in FIG. 2, respectively.

[0049]

5 A p-type well region 114 is formed in an upper region of an n-type silicon substrate 115, and an oxide film 201 is formed on the p-type well region 114 (FIGS. 6(a) and 6(b)).

[0050]

The oxide film is etched to form an oxide-film mask 202 (FIGS. 7(a) and 7(b)).

[0051]

10 The p-type well region 114 is etched to form a silicon hole portion (203, 204) (FIGS. 8(a) and 8(b)).

[0052]

The resulting product is subjected to an oxidation treatment to form an oxide film (205, 206) thereon in order to prevent the occurrence of ion channeling during an ion-implantation process. Then, polysilicon is deposited thereon, and etched to form a sidewall-shaped polysilicon film (207, 208) as a mask for use in the ion-implantation process (FIGS. 9(a) and 9(b)).

[0053]

20 Phosphorus (P) or arsenic (As) is implanted, and the resulting product is subjected to annealing to form an n-type photoelectric conversion region (110, 111) (FIGS. 10(a) and 10(b)).

[0054]

A resist (209, 210) is formed, and then a portion of the polysilicon film corresponding to a p⁺-type element isolation region to be formed in a sidewall of the silicon hole portion is etched (FIGS. 11(a) and 11(b)).

25 [0055]

The resist is removed, and then boron is implanted to form a p⁺-type region (104, 105) (FIGS. 12(a) and 12(b)).

[0056]

The remaining polysilicon film and the oxide film are removed (FIGS. 13(a) and 13(b)).

[0057]

An oxide film is deposited, and, after being flattened, etched to form a mask for use in an ion-plantation process (FIGS. 14(a) and 14(b)).

[0058]

5 An oxide film 213 is deposited to prevent the occurrence of ion channeling during the ion-implantation process (FIGS. 15(a) and 15(b)).

[0059]

Phosphorus (P) or arsenic (As) is implanted to form an n-type CCD channel region (103, 108, 109) (FIGS. 16(a) and 16(b)).

10 [0060]

A resist (214, 215, 216) is formed, and then boron is implanted to form a p⁺-type element isolation region (101, 102) (FIGS. 17(a) and 17(b)).

[0061]

The resist and the oxide film are removed (FIGS. 18(a) and 18(b)).

15 [0062]

A gate dielectric film 117 is formed, and then polysilicon is deposited and flattened (FIGS. 19(a) and 19(b)).

[0063]

The polysilicon is etched to form a transfer electrode (106, 107) (FIGS. 20(a) and 20(b)).

20 [0064]

A dielectric film 119 and a metal shield film 116 are deposited, and then the metal shield film 116 is etched (FIGS. 21(a) and 21(b)).

[0065]

In the above example, the transfer electrode may be made of an electrode material
25 commonly used in semiconductor processes or solid-state devices. For example, the electrode material includes low-resistance polysilicon, tungsten (W), molybdenum (Mo), tungsten silicide (WSi), molybdenum silicide (MoSi), titanium silicide (TiSi), tantalum silicide (TaSi) and copper silicide (CuSi). The transfer electrode may be formed in a multilayer structure using such a material without interposing a dielectric film therebetween.

[0066]

For example, the metal shield film may be formed as a metal film made of one selected from the group consisting of aluminum (Al), chromium (Cr), tungsten (W), titanium (Ti), molybdenum (Mo), an alloy layer made of a combination of two or more thereof, or a multilayer metal film formed of a combination of two or more selected from the group consisting of one or more types of the metal films and one or more types of the alloy layers.

[0067]

Although the present invention has been described in term of specific exemplary embodiments, it is apparent to those skilled in the art that various changes and modifications may be made therein without departing from the spirit and scope of the invention as set forth in appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0068]

FIG. 1 is a sectional view showing a unit pixel of a conventional solid-state image pickup element.

FIG. 2 is a top plan view of a CCD solid-state image pickup element according to one embodiment of the present invention.

FIG. 3 is a bird's-eye view of the CCD solid-state image pickup element according to the embodiment.

FIG. 4 is a sectional view taken along the line $X_1-X'_1$ in FIG. 2.

FIG. 5 is a sectional view taken along the line $Y_1-Y'_1$ in FIG. 2.

FIG. 6(a) is a sectional view ($X_1-X'_1$ section) showing a step of one example of a production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 6(b) is a sectional view ($Y_1-Y'_1$ section) showing the step in FIG. 6(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 7(a) is a sectional view ($X_1-X'_1$ section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 7(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 7(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

5 FIG. 8(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 8(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 8(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

10 FIG. 9(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 9(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 9(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

15 FIG. 10(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 10(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 10(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

20 FIG. 11(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 11(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 11(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

25 FIG. 12(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 12(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 12(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 13(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the

production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 13(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 13(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

5 FIG. 14(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 14(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 14(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

10 FIG. 15(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 15(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 15(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

15 FIG. 16(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 16(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 16(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

20 FIG. 17(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 17(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 17(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

25 FIG. 18(a) is a sectional view (X_1 - X'_1 section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 18(b) is a sectional view (Y_1 - Y'_1 section) showing the step in FIG. 18(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 19(a) is a sectional view ($X_1-X'_1$ section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 19(b) is a sectional view ($Y_1-Y'_1$ section) showing the step in FIG. 19(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 20(a) is a sectional view ($X_1-X'_1$ section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 20(b) is a sectional view ($Y_1-Y'_1$ section) showing the step in FIG. 20(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 21(a) is a sectional view ($X_1-X'_1$ section) showing a step of the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 21(b) is a sectional view ($Y_1-Y'_1$ section) showing the step in FIG. 21(a), in the example of the production process for the CCD solid-state image pickup element according to the embodiment.

FIG. 22 is a fragmentary top plan view of a solid-state image pickup device comprising a plurality of CCD solid-state image pickup elements arranged in a honeycomb array, according to another embodiment of the present invention.

FIG. 23 is a fragmentary bird's-eye view of the solid-state image pickup device according to the embodiment.

FIG. 24 is a sectional view taken along the line $X_2-X'_2$ in FIG. 22.

FIG. 25 is a sectional view taken along the line $Y_2-Y'_2$ in FIG. 22.

FIG. 26 is a fragmentary top plan view of a solid-state image pickup device comprising a plurality of CCD solid-state image pickup elements arranged in a matrix array, according to yet another embodiment of the present invention.

FIG. 27 is a fragmentary bird's-eye view of the solid-state image pickup device according to the embodiment.

FIG. 28 is a sectional view taken along the line $X_3-X'_3$ in FIG. 26.

FIG. 29 is a sectional view taken along the line $Y_3-Y'_3$ in FIG. 26.

EXPLANATION OF CODES

[0069]

- 11: n-type substrate
- 5 12: p-type well region
- 13: n-type photoelectric conversion region
- 14: p+-type region
- 15: p+-type element isolation region
- 16: n-type CCD channel region
- 10 17: Si oxide film
- 18: transfer electrode
- 20: metal shield film
- 24: metal-shield film opening
- 101: p+-type element isolation region
- 15 102: p+-type element isolation region
- 103: n-type CCD channel region
- 104: p+-type region
- 105: p+-type region
- 106: transfer electrode
- 20 107: transfer electrode
- 108: n-type CCD channel region
- 109: n-type CCD channel region
- 110: n-type photoelectric conversion region
- 111: n-type photoelectric conversion region
- 25 112: read channel
- 113: read channel
- 114: p+-type region
- 115: n-type substrate
- 116: metal shield film

- 117: gate dielectric film
- 119: dielectric film
- 201: oxide film
- 202: oxide-film mask
- 5 203: silicon hole portion
- 204: silicon hole portion
- 205: oxide film
- 206: oxide film
- 207: polysilicon sidewall
- 10 208: polysilicon sidewall
- 209: resist
- 210: resist
- 211: oxide film
- 212: oxide film
- 15 213: oxide film
- 214: resist
- 215: resist
- 216: resist
- 217: polysilicon
- 20 301: p+-type region
- 302: p+-type region
- 303: p+-type region
- 304: p+-type region
- 305: p+-type region
- 25 306: p+-type region
- 307: p+-type element isolation region
- 308: p+-type element isolation region
- 309: p+-type element isolation region
- 310: n-type CCD channel region

- 311: n-type CCD channel region
- 312: n-type CCD channel region
- 313: n-type CCD channel region
- 314: transfer electrode
- 5 315: transfer electrode
- 316: transfer electrode
- 317: transfer electrode
- 318: transfer electrode
- 319: transfer electrode
- 10 320: p-type well region
- 321: n-type substrate
- 322: n-type photoelectric conversion region
- 322: n-type photoelectric conversion region
- 324: n-type photoelectric conversion region
- 15 325: n-type photoelectric conversion region
- 326: n-type photoelectric conversion region
- 327: n-type photoelectric conversion region
- 328: gate dielectric film
- 329: dielectric film
- 20 330: metal shield film
- 331: silicon hole portion
- 332: silicon hole portion
- 333: silicon hole portion
- 334: silicon hole portion
- 25 335: read channel
- 336: read channel
- 337: read channel
- 338: read channel
- 339: silicon hole portion

- 340: read channel
- 341: read channel
- 343: silicon hole portion
- 501: p⁺-type region
- 5 502: p⁺-type region
- 503: p⁺-type region
- 504: p⁺-type region
- 505: p⁺-type element isolation region
- 506: p⁺-type element isolation region
- 10 507: n-type CCD channel region
- 508: n-type CCD channel region
- 509: n-type CCD channel region
- 510: transfer electrode
- 511: transfer electrode
- 15 512: transfer electrode
- 513: transfer electrode
- 514: transfer electrode
- 515: transfer electrode
- 516: transfer electrode
- 20 517: n-type photoelectric conversion region
- 518: n-type photoelectric conversion region
- 519: n-type photoelectric conversion region
- 520: n-type photoelectric conversion region
- 521: read channel
- 25 522: read channel
- 523: read channel
- 524: read channel
- 525: p-type well region
- 526: n-type substrate

524: gate dielectric film

528: dielectric film

529: metal shield film

530: silicon hole portion

5 531: silicon hole portion

532: silicon hole portion

533: silicon hole portion

What is claimed is:

1. A solid-state image pickup element comprising:
 - a second-conductive type planar semiconductor layer;
 - 5 a first-conductive type planar semiconductor layer formed on the second-conductive type planar semiconductor layer;
 - a hole portion formed in the first-conductive type planar semiconductor layer to define a hole therein;
 - a first-conductive type high-concentration impurity region formed in a bottom wall of the
 - 10 hole portion of the first-conductive type planar semiconductor layer;
 - a first-conductive type high-concentration impurity-doped element isolation region formed in a part of a sidewall of the hole portion of the first-conductive type planar semiconductor layer, and connected to the first-conductive type high-concentration impurity region;
 - a second-conductive type photoelectric conversion region formed in a portion of the
 - 15 first-conductive type planar semiconductor layer located beneath the first-conductive type high-concentration impurity region and in a part of a lower region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer, and adapted to undergo a change in charge amount upon receiving light;
 - a transfer electrode formed on the sidewall of the hole portion of the first-conductive type
 - 20 planar semiconductor layer through a gate dielectric film;
 - a second-conductive type CCD channel region formed in a top surface of the first-conductive type planar semiconductor layer and in a part of an upper region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer; and
 - 25 a read channel formed in a region of the first-conductive type planar semiconductor layer sandwiched between the second-conductive type photoelectric conversion region and the second-conductive type CCD channel region.
2. A solid-state image pickup device comprising a plurality of the solid-state image pickup

elements as defined in claim 1, wherein the solid-state image pickup elements are arranged in a matrix array.

3. The solid-state image pickup device as defined in claim 2, which includes:

5 a plurality of the second-conductive type CCD channel regions made up of a plurality of second-conductive type impurity regions each extending in a column direction at least in a region between adjacent ones of a plurality of columns of the hole portions formed in the first-conductive type planar semiconductor layer; and

10 a plurality of the first-conductive type high-concentration impurity-doped element isolation regions each arranged to prevent contact between adjacent ones of the second-conductive type CCD channel regions.

4. The solid-state image pickup device as defined in claim 3, which includes a plurality of the transfer electrodes each formed to extend in a row direction in a region between adjacent ones of
15 a plurality of rows of the hole portions formed in the first-conductive type planar semiconductor layer, and arranged along and in spaced-apart relation to the associated second-conductive type CCD channel region by a given distance to transfer therethrough signal charges generated in the associated solid-state image pickup element.

20 5. A solid-state image pickup device comprising a plurality of element line groups each consisting of a first solid-state image pickup element line and a second solid-state image pickup element line, wherein the first solid-state image pickup element line consists of a plurality of the solid-state image pickup elements as defined in claim 1 which are arranged in a first direction at intervals of a first distance, and the second solid-state image pickup element line consists of a
25 plurality of the solid-state image pickup elements as defined in claim 1 which are arranged in the first direction at intervals of the first distance and in displaced relation to the first solid-state image pickup element line in the first direction by a given distance, and wherein the first and second solid-state image pickup element lines in each of the element line groups are arranged in a second direction perpendicular to the first direction at interval of a second distance, and the

element line groups are arranged in the second direction at intervals of the second distance and in displaced relation to each other in the first direction.

6. The solid-state image pickup device as defined in claim 5, which includes:

5 a plurality of the second-conductive type CCD channel regions made up of a plurality of second-conductive type impurity regions each extending in a column direction at least in a region between adjacent ones of a plurality of columns of the hole portions formed in the first-conductive type planar semiconductor layer, while passing through the respective hole portions in the adjacent columns; and

10 a plurality of the first-conductive type high-concentration impurity-doped element isolation regions arranged to prevent contact between adjacent ones of the second-conductive type CCD channel regions.

7. The solid-state image pickup device as defined in claim 6, which includes a plurality of the
15 transfer electrodes each formed to extend in a row direction in a region between adjacent ones of a plurality of rows of the hole portions formed in the first-conductive type planar semiconductor layer, while passing through the respective hole portions in the adjacent rows, wherein the transfer electrodes are arranged in spaced-apart relation to each other by a given distance to allow signal charges generated in each of the solid-state image pickup elements, to be transferred
20 along respective an associated one of the second-conductive type CCD channel regions.

8. A method of producing a solid-state image pickup element, comprising the steps of:

forming a hole portion defining a hole therein, in a first-conductive type planar semiconductor layer formed on a second-conductive type planar semiconductor layer;

25 forming a first-conductive type high-concentration impurity region in a bottom wall of the hole portion of the first-conductive type planar semiconductor layer;

forming a first-conductive type high-concentration impurity-doped element isolation region in a part of a sidewall of the hole portion of the first-conductive type planar semiconductor layer;

forming a second-conductive type photoelectric conversion region adapted to undergo a

change in charge amount upon receiving light, in a portion of the first-conductive type planar semiconductor layer located beneath the first-conductive type high-concentration impurity region and in a part of a lower region of the remaining part of the sidewall of the hole portion of the first-conductive type planar semiconductor layer;

5 forming a transfer electrode on the sidewall of the hole portion of the first-conductive type planar semiconductor layer through a gate dielectric film;

 forming a second-conductive type CCD channel region in an top surface of the first-conductive type planar semiconductor layer and in a part of an upper region of the remaining part of the sidewall of the hole portion of the first-conductive type planar
10 semiconductor layer; and

 forming a read channel in a region of the first-conductive type planar semiconductor layer sandwiched between the second-conductive type photoelectric conversion region and the second-conductive type CCD channel region.

15 9. The method as defined in claim 8, wherein the step of forming a hole portion includes forming a mask on the first-conductive type planar semiconductor layer formed on the second-conductive type planar semiconductor layer, and etching the first-conductive type planar semiconductor layer to form the hole portion therein.

20 10. The method as defined in claim 9, wherein the step of forming a second-conductive type photoelectric conversion region includes the sub-steps of: forming a masking material on the sidewall of the hole portion of the first-conductive type planar semiconductor layer; and forming the second-conductive type photoelectric conversion region by an ion-implantation process.

25 11. The method as defined in claim 10, wherein the step of forming a first-conductive type high-concentration impurity region is performed after the sub-step of forming the second-conductive type photoelectric conversion region by an ion-implantation process.

12. The method as defined in claim 11, which further comprises the step of, after the sub-step of

forming the second-conductive type photoelectric conversion region by an ion-implantation process, removing a part of the masking material formed on the sidewall of the hole portion of the first-conductive type planar semiconductor layer, wherein each of the step of forming a first-conductive type high-concentration impurity region and the step of forming a first-conductive type high-concentration impurity-doped element isolation region is performed by an ion-implantation process after the step of removing a part of the masking material.

13. The method as defined in any one of claims 9 to 12, wherein the step of forming a second-conductive type CCD channel region includes the sub-steps of: forming a masking material on the hole portion of the first-conductive type planar semiconductor layer; and forming the second-conductive type CCD channel region by an ion-implantation process.

14. The method as defined in claim 13, wherein the step of forming a first-conductive type high-concentration impurity-doped element isolation region includes the sub-steps of: forming a masking material in such a manner as to allow the first-conductive type high-concentration impurity-doped element isolation region to be formed in connected relation to the first-conductive type high-concentration impurity-doped element isolation region (first-conductive type high-concentration impurity region) by an ion-implantation process; and forming the first-conductive type high-concentration impurity-doped element isolation region by the ion-implantation process.

15. The method as defined in any one of claims 9 to 14, wherein the step of forming a transfer electrode including the sub-steps of: forming the gate dielectric film on a surface of the first-conductive type planar semiconductor layer; depositing a gate electrode material on the gate dielectric film; flattening the gate electrode material; and etching the flattened gate electrode material to form the transfer electrode.