

tors T.1 to T.N+1. The arrangement further comprises correction means 4 comprising a correction circuit 5 having a reference-current-source 6, for supplying the control signal to one of the control inputs 3.1 to 3.N+1, and having a switching network 7, for coupling each time one of the transistor configurations 2.1 to 2.N+1 to the correction circuit 5 and for coupling the other transistor configurations to the outputs 1 ... N in accordance with a cyclic pattern.

In the present arrangement N transistor configurations supply the output currents to the outputs 1 to N in every period of a cycle, the remaining transistor configuration being coupled to the correction circuit 4. In this circuit the current from the relevant transistor configuration is compared with the reference-current from the source 6 and, by means of a control signal applied to the control input 3 of the transistor configuration by the correction circuit 5 the control voltage of the control transistor 2 is adjusted in such a way that the current from the transistor configuration is equal to the reference-current. In the next period of the cycle the corrected transistor configuration 2 is exchanged with an "uncorrected" transistor configuration 2 by means of the switching network 7. Thus, the current from all the transistor configurations 2.1 to 2.N+1 are corrected successively and continually. As a result of this, the currents available at the outputs 1 to N are highly equal to the reference-current. Since a transistor configuration to be corrected is switched out of the actual current-source arrangement the correction circuit 5 will not disturb the correct operation of the current-source arrangement. Since the correction circuit does not require a higher supply voltage than during normal operation of the arrangement the current-source arrangement is suitable for operation with low supply voltages.

Fig. 2 shows a first embodiment of a current-source arrangement in accordance with the invention. The arrangement comprises four transistor configurations comprising control transistors T1 to T4 with capacitors C1 to C4 arranged between their gate and source electrodes. By means of switches S1.1 to S4.1, S1.2 to S4.2 and S1.3 to S3.3 each time three of the four transistors T1 to T4 can be coupled to the outputs 1, 2 and 3, the remaining transistor being coupled to the inputs 10 and 11 of the correction circuit 5. These switches are controlled in accordance with a cyclic pattern, in the present example by means of a shift register 14 which is controlled by a clock 15.

The Figure illustrates the situation in which the currents I1, I3 and I4 from the transistors T1, T3 and T4 are applied to the outputs 1, 2 and 3, while the current I2 from the transistor T2 is applied to the input 11 of the correction circuit 5. The switch-

es S1.1, S3.1 and S4.1 are open and the switch S2.1 is closed, so that the gate electrode of the transistor T2 is coupled to the input 10. In the present example the correction circuit comprises a reference-current-source 6, which supplies a current Iref to the interconnected inputs 10 and 11.

As a result of this direct connection between the inputs 10 and 11 the drain electrode of the transistor T2 is connected to its gate electrode. The current-source 6 now controls the voltage on the capacitor C2 in such a way that the current I2 becomes accurately equal to the reference-current Iref. In the next clock period the transistor T2 is connected to the output 2 by means of the switches S2.2 and S2.3, and at the same time the switch S2.1 is opened. The voltage on the capacitor C2 therefore remains available, so that the transistor T2 continues to supply a current I2 which is accurately equal to the current Iref. In the same clock period one of the other three transistors, for example the transistor T3, is connected to the inputs 10 and 11 of the correction circuit and the control voltage on the capacitor C3 is adjusted in such a way that the current I3 becomes accurately equal to the current Iref. Thus, the currents I1 to I4 of the transistors T1 to T4 are successively and continually made equal to the current Iref. This results in accurately equal currents being available on the outputs 1, 2 and 3.

Fig. 3 shows a second embodiment of a current-source arrangement in accordance with the invention, in which for simplicity only the correction circuit and the transistor to be corrected are shown. The correction circuit comprises a current-source 6, which supplies a reference-current Iref, which is converted into a reference voltage Vref across a resistor R1. The input 11 is connected to the positive power-supply terminal via a resistor R2. The resistors R1 and R2 are connected to the inverting input and the non-inverting input of an amplifier 16, whose output is connected to the input 10. Again the gate and the drain electrode of the transistor T2 are connected to the inputs 10 and 11. The current I2 from the transistor T2 is converted into a proportional voltage across the resistor R2. The amplifier 16 now controls the voltage across the capacitor C2 in such a way that the voltage across the resistor R2 is equal to the reference voltage Vref across the resistor R1. When R1 and R2 have equal resistance values the current I2 will be accurately equal to the current Iref. By selecting a specific ratio for the resistance values of the resistors R1 and R2 it is possible to define the ratio between the currents Iref. and I2.

Fig. 4 shows a third embodiment of a current-source arrangement in accordance with the invention, in which identical parts bear the same reference numerals as in Fig. 2. The transistor configurations now comprise control transistors T1 to T4

and capacitors C1 to C4, with which current-sources B1 to B4 are arranged in parallel. The current supplied by a transistor configuration is equal to the sum of the currents from a control transistor and a current-source. The currents from the current sources B1 to B4 are therefore smaller than the reference current from the current source 6. By means of switches S1.1 to S4.1, S1.2 to S4.2, S1.4 to S4.4, and S1.3 to S3.3 each time three of the four currents of the transistor configurations T1, B1 to T4, B4 can be applied to the outputs 1, 2 and 3, while the currents from the control transistor and the current-source of the remaining transistor configuration are applied to inputs 11 and 13 of the correction circuit 5.

The Figure illustrates the situation in which the currents from the transistor configurations T1, B1, T3, B3 and T4, B4 are applied to the outputs 1, 3 and 2 and the transistor configuration T2, B2 is connected to the correction circuit 5. The switches S1.1, S3.1 and S4.1 are then open and the switch S2.1 is connected to the input 10 of the correction circuit 5. The correction circuit 5 again comprises a current-source 6 for supplying a reference-current Iref, which current source has its output connected to the inputs 10, 11 and 13.

The difference ΔI_2 between the currents Iref and I2 is applied to the drain electrode of the transistor T2. The current-source 6 now controls the voltage on the capacitor C2 in such a way that the sum of the currents I2 and ΔI_2 is equal to the current Iref. For the remainder the arrangement operates in the same way as that shown in Fig. 2. Since the correction circuit only corrects a small difference current via the voltage on the capacitor C2 the susceptibility of the output current to small variations in the gate-source voltage of transistor T2 is reduced substantially.

Fig. 5 shows a fourth embodiment, in which for simplicity only the correction circuit in the transistor to be corrected are shown. Identical parts bear the same reference numerals as in Fig. 4. Again the correction circuit comprises a current-source 6, which carries a reference-current Iref. The current I2 of the current-source B2 is derived from this current at the input 13. The difference between the currents Iref and I2 is applied to a transistor T5, whose drain electrode is connected to the gate electrode. The gate electrode is coupled to the input 10. The input 11 is coupled to a point carrying a direct voltage Vc. Again the gate and the drain electrode of the transistor T2 are connected to the inputs 10 and 11. The transistor T5 in conjunction with the transistor T2 constitutes a current-mirror circuit, to which the current ΔI_2 is applied. This current controls the voltage on the capacitor C2 in such a way that the current of the transistor T5 is accurately equal to the current ΔI_2 .

Since the same control voltage appears between the gate and the source electrode of the transistor T2 the current of the transistor T2 will also be accurately equal to ΔI_2 . For the remainder the arrangement operates in the same way as that in Fig. 4.

Fig. 6 shows a fifth embodiment in which only the correction circuit and the transistor to be corrected are shown. Identical parts bear the same reference numerals as in Fig. 3. The arrangement operates in the same way as that shown in Fig. 3, the difference being that now the sum of the current ΔI_2 from the transistor T2 and the current I2 from the current-source B2 is applied to the resistor R2.

Fig. 7 shows a sixth embodiment, and again shows only the correction circuit and the transistor to be corrected. Identical parts bear the same reference numerals as in Fig. 2. Again the correction circuit comprises a current-source 6, which now supplies a current Iref + Ib and a transistor T6, whose source electrode is coupled to the current-source 6, whose gate electrode is at a voltage Vref, and whose drain electrode is connected to the negative power-supply terminal via a bias-current-source 20 which carries a current Ib. Again the gate and the drain electrode of the transistor T2 are connected to the inputs 10 and 11 of the correction circuit. The difference current Iref between the currents from the current-sources 6 and 20 again controls the voltage on the capacitor C2 in such a way, via the transistor T6, that the current I2 from the transistor T2 becomes accurately equal to the current Iref. The reference voltage Vref is selected in such a way that the voltage on the drain electrode of the transistor T2 is equal to the drain voltage of the transistor T2 when this transistor is switched into the actual current-source arrangement or D/A converter. This is to ensure that as a result of another drain-source voltage the transistor T2 in the actual arrangement cannot carry another current than in the correction circuit.

It will be evident that this correction circuit may also be employed in the embodiment shown in Fig. 4, in which case the current-source B2 should again be connected to the input 13 of the correction circuit, as is shown in broken lines in Fig. 7. The difference current $\Delta I_2 = I_{ref} - I_2$ then controls the voltage across the capacitor C2 via the transistor T6 in such a way that the current through the transistor T2 becomes accurately equal to the current ΔI_2 .

In the embodiments shown the switches suitably comprise transistors. By way of illustration Fig. 8a shows a transistor T2 with a capacitor C2 and a switch S2.1 comprising a transistor T7. Fig. 8b shows a modification to this, a transistor T8 being arranged in series with the transistor T7 and having

Description

The invention relates to a current source arrangement for supplying a required number of currents comprising:

- a plurality of transistor configurations for generating a plurality of substantially equal currents,
- each transistor configuration comprising a control transistor whose control voltage is adjustable to supply an adjustable first current, and
- correction means for reducing the mutual deviation in the currents from the transistor configurations.

The invention also relates to a digital-to-analog converter comprising such an arrangement.

Such an arrangement is known from EP-A-0,115,897. In this arrangement the correction means comprise a precision-current-mirror circuit in which the current from one transistor configuration is applied to the input as a reference-current and the current from another transistor configuration is applied to the at least one output in accordance with a cyclic pattern. The difference between the reference-current and the current from the other transistor configuration then appears on this output, said difference being used to correct the last mentioned current in such a way that it is better in compliance with the reference-current.

A disadvantage of this arrangement is that the precision-current-mirror circuit must be arranged in series with the transistor configuration and its load, so that the known current-source arrangement requires a comparatively high supply voltage.

Therefore it is an object of the invention to provide a current-source arrangement with correction means, which is constructed to operate on comparatively low supply voltages.

In accordance with the invention a current-source arrangement of the type defined in the opening paragraph is characterized in that:

- the number of transistor configurations is at least one larger than the required number of currents and
- the correction means are adapted to make the current from each transistor configuration equal to a reference-current in accordance with a cyclic pattern by adjusting the control voltage of the control transistor of the relevant transistor configuration.

Since in the arrangement in accordance with the invention the number of transistor configurations is one larger than actually required this means that in every cycle period it is possible to use one transistor configuration of the current-source arrangement for the purpose of correction and to switch the transistor configuration corrected

in the preceding cycle period back into the current-source arrangement. Since during correction a transistor configuration is no longer connected in series with the load of the current-source arrangement the arrangement can be operated with comparatively low supply voltages.

Another advantage of the current-source arrangement in accordance with the invention is that the operation of the actual current-source arrangement is not disturbed by the correction means.

Embodiments of a current-source arrangement according to the invention are defined in the appended subsidiary claims.

The invention will now be described in more detail, by way of example with reference to the accompanying drawings in which:

Fig. 1 shows the basic circuit diagram of a current-source arrangement in accordance with the invention,

Fig. 2 shows a first embodiment of a current-source arrangement in accordance with the invention,

Fig. 3 shows a second embodiment of a current-source arrangement in accordance with the invention,

Fig. 4 shows a third embodiment of a current-source arrangement in accordance with the invention,

Fig. 5 shows a fourth embodiment of a current-source arrangement in accordance with the invention,

Fig. 6 shows a fifth embodiment of a current-source arrangement in accordance with the invention,

Fig. 7 shows a sixth embodiment of a current-source arrangement in accordance with the invention,

Fig. 8 shows two examples of switches for use in a current-source arrangement in accordance with the invention,

Fig. 9 shows a first embodiment of a digital-to-analog converter comprising current-source arrangements in accordance with the invention, and

Fig. 10 shows a second embodiment of a digital-to-analog converter in accordance with the invention.

Fig. 1 is a basic diagram of a current-source arrangement in accordance with the invention. The arrangement is constructed to supply N substantially equal currents to outputs 1 to N, to which loads, which are not shown for the sake of simplicity, can be connected. The arrangement comprises N+1 transistor configurations 2.1 to 2.N+1, with respective control transistors T1 to T.N+1. The transistor configurations further comprise control inputs 3.1 to 3.N+1 for adjusting the control voltage and hence the currents of the control transis-

its drain connected to the source electrode. A signal which is the inverse of the signal applied to the gate of the transistor T7 is applied to the gate of the transistor T8. Transistor T8 thereby prevents the charge present in the transistor T7 from being drained to the capacitor C2 during turning off.

The capacitors C1 to C4 in the embodiment shown herein may be separate capacitors but may also be constituted in a suitable manner by the gate-source capacitances of the transistors.

Fig. 9 shows a first embodiment of a D/A converter comprising current-source arrangements in accordance with the invention. The present example is a 16-bit D/A converter. It comprises a current-source arrangement 50, shown diagrammatically, comprising 18 transistor configurations, whose currents are made substantially equal to the reference-current I_{ref} from a current-source 52 by means of a correction circuit 51 in a manner as described above. One current I_{ref} of the seventeen output currents is employed as the reference-current for the correction circuit 61 of a second current-source arrangement 60 comprising seventeen transistor configurations, whose currents are made equal to the current I_{ref} in a manner as described above. One of the currents I_{ref} in the arrangement 60 is applied to a binary current divider 63 which in the present example supplies the currents for the eight least significant bits. The other currents of the arrangement are combined so as to obtain a binary-weighted series of currents I_{ref} , $2I_{ref}$... $8I_{ref}$. The sixteen other currents in the current-source arrangement 50 are combined to obtain a current $16I_{ref}$, which is applied as a reference-current to the correction circuit 71 of a third current-source arrangement 70 comprising sixteen transistor configurations, whose currents are made equal to the current $16I_{ref}$ in a manner as described above. The fifteen currents in the current-source arrangement 70 are combined so as to obtain the binary-weighted series $16I_{ref}$, $32I_{ref}$... $128I_{ref}$. The output currents of the current-source arrangements 60 and 70 and the current divider 63 are used in known manner to convert a digital input code into an analog output signal.

Fig. 10 shows a second embodiment of a 16-bit D/A converter comprising a current-source arrangement in accordance with the invention. It comprises a current-source 90, shown diagrammatically, for generating 64 substantially equal currents which are successively and continually made equal to a reference-current by means of a correction circuit 95 in a manner as described above. By means of a switching network 100, comprising 63 two-way switches, which are not shown for simplicity, 63 currents are applied either to the summing point 125 or to a positive power-supply terminal depending on the 6 most significant bits of the

digital input code. One of the 64 currents is applied to the current-dividing circuit 115, which is shown diagrammatically. The current-dividing circuit 115 supplies the currents for the 10 least significant bits, which currents by means of a switching network 120 comprising two-way switches, which are not shown for simplicity, are applied either to the summing point 125 or to the positive power-supply terminal depending on the digital input code. The total output current I_{out} appearing on the summing point 125 can be converted into an output voltage V_{out} by means of a current-voltage converter 130, shown diagrammatically.

In the present embodiment the 16-bit digital input word is applied serially to an input 111 of a data register 110. The 10 least significant bits directly control the switches of the switching network 120. The 6 most significant bits are first applied to a decoding device 105, which derives the switching signals for the 63 switches of the switching network 100 from these bits.

In the D/A converters comprising current-source arrangements in accordance with the invention the frequency with which the correction network is connected to the successive transistor configurations is preferably selected in such a way that the frequency with which the digital input code is applied is equal to a multiple ($N \geq 1$) of said switching frequency. This results in switching transients, which may be caused by the correction and switching network, being smoothed by the customary deglitching network arranged at the output of a D/A converter in order to smooth switching transients produced by the actual D/A converter.

Claims

1. A current source arrangement for supplying a required number of currents (1, 2,...,N) comprising:
 - a plurality of transistor configurations (2.1,...,2.N + 1) for generating a plurality of substantially equal currents,
 - each transistor configuration comprising a control transistor (T1,...,TN + 1) whose control voltage is adjustable to supply an adjustable first current, and
 - correction means (4) for reducing the mutual deviation in the currents in the transistor configurations (2.1,...,2.N + 1), characterized in that
 - the number of transistor configurations (2.1,...,2.N + 1) is at least one larger than the required number of currents, and
 - the correction means (4) are adapted to make the current from each transistor configuration (2.1,...,2.N + 1) equal to a reference-current (6) in accordance with



its drain connected to the source electrode. A signal which is the inverse of the signal applied to the gate of the transistor T7 is applied to the gate of the transistor T8. Transistor T8 thereby prevents the charge present in the transistor T7 from being drained to the capacitor C2 during turning off.

The capacitors C1 to C4 in the embodiment shown herein may be separate capacitors but may also be constituted in a suitable manner by the gate-source capacitances of the transistors.

Fig. 9 shows a first embodiment of a D/A converter comprising current-source arrangements in accordance with the invention. The present example is a 16-bit D/A converter. It comprises a current-source arrangement 50, shown diagrammatically, comprising 18 transistor configurations, whose currents are made substantially equal to the reference-current I_{ref} from a current-source 52 by means of a correction circuit 51 in a manner as described above. One current I_{ref} of the seventeen output currents is employed as the reference-current for the correction circuit 61 of a second current-source arrangement 60 comprising seventeen transistor configurations, whose currents are made equal to the current I_{ref} in a manner as described above. One of the currents I_{ref} in the arrangement 60 is applied to a binary current divider 63 which in the present example supplies the currents for the eight least significant bits. The other currents of the arrangement are combined so as to obtain a binary-weighted series of currents I_{ref} , $2I_{ref}$... $8I_{ref}$. The sixteen other currents in the current-source arrangement 50 are combined to obtain a current $16I_{ref}$, which is applied as a reference-current to the correction circuit 71 of a third current-source arrangement 70 comprising sixteen transistor configurations, whose currents are made equal to the current $16I_{ref}$ in a manner as described above. The fifteen currents in the current-source arrangement 70 are combined so as to obtain the binary-weighted series $16I_{ref}$, $32I_{ref}$... $128I_{ref}$. The output currents of the current-source arrangements 60 and 70 and the current divider 63 are used in known manner to convert a digital input code into an analog output signal.

Fig. 10 shows a second embodiment of a 16-bit D/A converter comprising a current-source arrangement in accordance with the invention. It comprises a current-source 90, shown diagrammatically, for generating 64 substantially equal currents which are successively and continually made equal to a reference-current by means of a correction circuit 95 in a manner as described above. By means of a switching network 100, comprising 63 two-way switches, which are not shown for simplicity, 63 currents are applied either to the summing point 125 or to a positive power-supply terminal depending on the 6 most significant bits of the

digital input code. One of the 64 currents is applied to the current-dividing circuit 115, which is shown diagrammatically. The current-dividing circuit 115 supplies the currents for the 10 least significant bits, which currents by means of a switching network 120 comprising two-way switches, which are not shown for simplicity, are applied either to the summing point 125 or to the positive power-supply terminal depending on the digital input code. The total output current I_{out} appearing on the summing point 125 can be converted into an output voltage V_{out} by means of a current-voltage converter 130, shown diagrammatically.

In the present embodiment the 16-bit digital input word is applied serially to an input 111 of a data register 110. The 10 least significant bits directly control the switches of the switching network 120. The 6 most significant bits are first applied to a decoding device 105, which derives the switching signals for the 63 switches of the switching network 100 from these bits.

In the D/A converters comprising current-source arrangements in accordance with the invention the frequency with which the correction network is connected to the successive transistor configurations is preferably selected in such a way that the frequency with which the digital input code is applied is equal to a multiple ($N \geq 1$) of said switching frequency. This results in switching transients, which may be caused by the correction and switching network, being smoothed by the customary deglitching network arranged at the output of a D/A converter in order to smooth switching transients produced by the actual D/A converter.

Claims

1. A current source arrangement for supplying a required number of currents (1, 2,...,N) comprising:
 - a plurality of transistor configurations (2.1,...,2.N+1) for generating a plurality of substantially equal currents,
 - each transistor configuration comprising a control transistor (T1,...,TN+1) whose control voltage is adjustable to supply an adjustable first current, and
 - correction means (4) for reducing the mutual deviation in the currents from the transistor configurations (2.1,...,2.N+1), characterized in that
 - the number of transistor configurations (2.1,...,2.N+1) is at least one larger than the required number of currents, and
 - the correction means (4) are adapted to make the current from each transistor configuration (2.1,...,2.N+1) equal to a reference-current (6) in accordance with



a cyclic pattern by adjusting the control voltage of the control transistor of each said transistor configuration, and

- in each period of the cycle a corrected transistor configuration (2.1,...,2.N+1) is exchanged with an uncorrected transistor configuration (2.1,...,2.N+1) by means of a switching network (7) such that the transistor configuration to be corrected is switched out of the current source arrangement.

2. A current-source arrangement as claimed in Claim 1, characterized in that each transistor configuration is constituted by the control transistor (T₂) having a capacitor (C₂) arranged between its gate and its source electrode.

3. A current-source arrangement as claimed in Claim 2, characterized in that the capacitor is constituted by the gate source capacitance of the relevant control transistor.

4. A current-source arrangement as claimed in Claim 2 or 3, characterized in that the correction means (4) comprise means for applying the reference-current (6) to the drain electrode of the control transistor (T₂) and negative-feedback means (16) between the drain and the gate electrode for controlling the voltage on the capacitor in such a way that the first current (I₂) is equal to the reference-current (I_{ref}).

5. A current-source arrangement as claimed in Claim 2 or 3, characterized in that the correction means comprise:

- a first resistor (R₁) for converting the reference-current in a reference voltage,
- a second resistor (R₂) for converting the first current into a second voltage, and
- negative-feedback means (16) connected to the first (R₁) and the second (R₂) resistor and the capacitor (C₂) for adjusting the voltage on the capacitor (C₂) in such a way that the second voltage is equal to the reference voltage.

6. A current-source arrangement as claimed in Claim 4, characterized in that the negative-feedback means comprise adjustment means for adjusting the voltage on the drain electrode of the control transistor.

7. A current-source arrangement as claimed in Claim 6, characterized in that the adjustment means comprise a current-follower transistor (T₆) whose source electrode is coupled to the drain electrode of the control transistor (T₂),

whose gate electrode is coupled to a reference voltage terminal (V_{ref}), and whose drain electrode is coupled to a bias-current-source (20).

8. A current-source arrangement as claimed in Claim 1, characterized in that each transistor configuration is constituted by the control transistor (T₂) having a capacitor (C₂) arranged between its gate and its source electrode, and a transistor current-source (B₂) for supplying a second current, the current from the transistor configuration being equal to the sum of the first and the second current.

9. A current-source arrangement as claimed in Claim 8, characterized in that the capacitor is constituted by the gate-source capacitance of the relevant control transistor (T₂).

10. A current-source arrangement as claimed in Claim 8 or 9, characterized in that the correction means comprise means for applying the difference between the reference-current and the second current to the drain electrode of the control transistor (T₂) and negative-feedback means arranged between the drain and the gate electrode for adjusting the voltage on the capacitor in such a way that the sum of the first and the second current is equal to the reference-current.

11. A current-source arrangement as claimed in Claim 8 or 9, characterized in that the correction means comprise means for supplying the difference between the reference-current and the second current to the drain electrode of a second transistor (T₅) having its gate-source junction arranged in parallel with the gate source junction of the control transistor (T₂), and negative-feedback means arranged between the drain and the gate electrode of the second transistor (T₅) to control the voltage on the capacitor (C₂) in such a way that the sum of the current from the second transistor (T₅) and the second current is equal to the reference-current.

12. A current-source arrangement as claimed in Claim 8 or 9, characterized in that the correction means comprise:

- a first resistor (R₁) for converting the reference-current into a reference voltage,
- a second resistor (R₂) for converting the sum of the first and the second current into a second voltage, and
- negative-feedback means connected to the first (R₁) and the second (R₂) resistor



and the capacitor (C_2) for adjusting the voltage on the capacitor (C_2) in such a way that the second voltage is equal to the reference voltage.

13. A current-source arrangement as claimed in Claim 11, characterized in that the negative-feedback means comprise adjustment means for adjusting the voltage on the drain electrode of the control transistor.

14. A current-source arrangement as claimed in Claim 13, characterized in that the adjustment means comprise a current follower transistor (T_6), having its source electrode coupled to the drain electrode of the control transistor (T_2), having its gate electrode coupled to a reference voltage terminal (V_{ref}), and having its drain electrode coupled to a bias-current-source (20).

15. A digital-to-analog converter comprising a current source arrangement as claimed in any one of the preceding claims, and further comprising:

- an input terminal (111) for a digital signal,
- an output terminal (125) for summing a plurality of selected currents determined by said digital signal,
- a data register (110) coupled to said input terminal (111),
- a switching network (100) controlled by said data register (110) selectively coupling to said output terminal (125) a plurality of outputs of said current source arrangement.

Patentansprüche

1. Stromquellenanordnung zur Lieferung einer benötigten Anzahl Ströme (1, 2, ... N) mit:

- einer Anzahl Transistorkonfigurationen (2.1, ... 2.N+1) zur Erzeugung einer Anzahl nahezu gleicher Ströme,
- wobei jede Transistorkonfiguration einen Regeltransistor (T_1 , ... T_{N+1}) umfaßt, dessen Steuerspannung zur Lieferung einen einstellbaren ersten Stroms einstellbar ist, und
- Korrekturmitteln (4) zur Verkleinerung der gegenseitigen Abweichung der Ströme aus den Transistorkonfigurationen (2.1, ..., 2.N+1),
dadurch gekennzeichnet, daß
- die Zahl der Transistorkonfigurationen (2.1, ..., 2.N+1) um mindestens eins größer als die benötigte Anzahl Ströme ist,

und

- die Korrekturmittel (4) eingerichtet sind, um den aus jeder Transistorkonfiguration (2.1, ..., 2.N+1) kommenden Strom durch Einstellen der Steuerspannung des Regeltransistors jeder genannten Transistorkonfiguration in zyklischer Weise gleich einem Bezugsstrom (6) zu machen, und
- in jeder Periode des Zyklus mit Hilfe eines Schaltnetzes (7) eine korrigierte Transistorkonfiguration (2.1, ..., 2.N+1) gegen eine unkorrigierte Transistorkonfiguration (2.1, ..., 2.N+1) ausgetauscht wird, so daß die zu korrigierende Transistorkonfiguration aus der Stromquellenanordnung herausgeschaltet wird.

2. Stromquellenanordnung nach Anspruch 1, dadurch gekennzeichnet, daß jede Transistorkonfiguration von dem Regeltransistor (T_2) gebildet wird, der einen zwischen seine Gate-Elektrode und seine Source-Elektrode geschalteten Kondensator (C_2) aufweist.

3. Stromquellenanordnung nach Anspruch 2, dadurch gekennzeichnet, daß der Kondensator von der Gate-Source-Kapazität des betreffenden Regeltransistors gebildet wird.

4. Stromquellenanordnung nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß die Korrekturmittel (4) Mittel zum Zuführen des Bezugsstroms (6) zur Drain-Elektrode des Regeltransistors (T_2) und Gegenkopplungsmittel (16) zwischen der Drain- und der Gate-Elektrode enthalten, um die Spannung am Kondensator so zu steuern, daß der erste Strom (12) gleich dem Bezugsstrom (I_{ref}) ist.

5. Stromquellenanordnung nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß die Korrekturmittel folgendes umfassen:

- einen ersten Widerstand (R_1) zum Umwandeln des Bezugsstroms in eine Bezugsspannung,
- einen zweiten Widerstand (R_2) zum Umwandeln des ersten Stroms in eine zweite Spannung, und
- mit dem ersten (R_1) und dem zweiten (R_2) Widerstand und dem Kondensator (C_2) verbundene Gegenkopplungsmittel zum Einstellen der Spannung am Kondensator (C_2) in solcher Weise, daß die zweite Spannung gleich der Bezugsspannung ist.



6. Stromquellenanordnung nach Anspruch 4, dadurch gekennzeichnet, daß die Gegenkopplungsmittel Einstellmittel zum Einstellen der Spannung an der Drain-Elektrode des Regeltransistors umfassen.

7. Stromquellenanordnung nach Anspruch 6, dadurch gekennzeichnet, daß die Einstellmittel einen Stromfolgertransistor (T6) umfassen, dessen Source-Elektrode mit der Drain-Elektrode des Regeltransistors (T2) gekoppelt ist, dessen Gate-Elektrode mit einer Bezugsspannungsklemme (V_{ref}) gekoppelt ist und dessen Drain-Elektrode mit einer Eingangsruhestromquelle (20) gekoppelt ist.

8. Stromquellenanordnung nach Anspruch 1, dadurch gekennzeichnet, daß jede Transistorkonfiguration von dem Regeltransistor (T_2), der einen zwischen seiner Gate- und seiner Source-Elektrode geschalteten Kondensator (C_2) hat, und einer Transistorstromquelle (B2) zur Lieferung eines zweiten Stroms gebildet wird, wobei der aus der Transistorkonfiguration kommende Strom gleich der Summe aus dem ersten und dem zweiten Strom ist.

9. Stromquellenanordnung nach Anspruch 8, dadurch gekennzeichnet, daß der Kondensator von der Gate-Source-Kapazität des betreffenden Regeltransistors (T_2) gebildet wird.

10. Stromquellenanordnung nach Anspruch 8 oder 9, dadurch gekennzeichnet, daß die Korrekturmittel Mittel zur Zuführung der Differenz zwischen dem Bezugsstrom und dem zweiten Strom an die Drain-Elektrode des Regeltransistors (T_2) enthalten sowie zwischen der Drain- und der Gate-Elektrode angeordnete Gegenkopplungsmittel zum Einstellen der Spannung am Kondensator in solcher Weise, daß die Summe aus dem ersten und dem zweiten Strom gleich dem Bezugsstrom ist.

11. Stromquellenanordnung nach Anspruch 8 oder 9, dadurch gekennzeichnet, daß die Korrekturmittel Mittel zur Lieferung der Differenz zwischen dem Bezugsstrom und dem zweiten Strom an die Drain-Elektrode eines zweiten Transistors (T5), dessen Gate-Source-Übergang parallel zum Gate-Source-Übergang des Regeltransistors (T_2) angeordnet ist, enthalten sowie zwischen der Drain- und der Gate-Elektrode des zweiten Transistors (T5) angeordnete Gegenkopplungsmittel zum Steuern der Spannung am Kondensator (C_2) in solcher Weise, daß die Summe aus dem Strom des zweiten Transistors (T5) und dem zweiten Strom gleich

dem Bezugsstrom ist.

12. Stromquellenanordnung nach Anspruch 8 oder 9, dadurch gekennzeichnet, daß die Korrekturmittel folgendes umfassen:

- einen ersten Widerstand (R_1) zum Umwandeln des Bezugsstroms in eine Bezugsspannung,
- einen zweiten Widerstand (R_2) zum Umwandeln der Summe aus dem ersten und dem zweiten Strom in eine zweite Spannung, und
- mit dem ersten (R_1) und dem zweiten (R_2) Widerstand und den Kondensator (C_2) verbundene Gegenkopplungsmittel zum Einstellen der Spannung am Kondensator (C_2) in solcher Weise, daß die zweite Spannung gleich der Bezugsspannung ist.

13. Stromquellenanordnung nach Anspruch 11, dadurch gekennzeichnet, daß die Gegenkopplungsmittel Einstellmittel zum Einstellen der Spannung an der Drain-Elektrode des Regeltransistors umfassen.

14. Stromquellenanordnung nach Anspruch 13, dadurch gekennzeichnet, daß die Einstellmittel einen Stromfolgertransistor (T6) umfassen, dessen Source-Elektrode mit der Drain-Elektrode des Regeltransistors (T_2) gekoppelt ist, dessen Gate-Elektrode mit einer Bezugsspannungsklemme (V_{ref}) gekoppelt ist und dessen Drain-Elektrode mit einer Eingangsruhestromquelle (20) gekoppelt ist.

15. Digital-Analog-Umsetzer mit einer Stromquellenanordnung nach einem der vorhergehenden Ansprüche und außerdem:

- einer Eingangsklemme (111) für ein Digitalsignal,
- einer Ausgangsklemme (125) zum Summieren einer Anzahl von dem genannten Digitalsignal bestimmter ausgewählter Ströme,
- einem mit der genannten Eingangsklemme (111) gekoppelten Datenregister (110),
- einem von dem Datenregister (110) gesteuerten Schaltnetz (100), das mit der Ausgangsklemme (125) eine Anzahl Ausgänge der genannten Stromquellenanordnung koppelt.

Revendications

1. Circuit de source de courant pour fournir un nombre souhaité de courants (1, 2, ..., N), com-



portant

- une pluralité de configurations de transistors (2.1,...,2.N+1) pour engendrer une pluralité de courants sensiblement égaux,
 - chaque configuration de transistors comportant un transistor de commande (T1,...,TN+1) dont la tension de commande peut être réglée pour fournir un premier courant réglable, et
 - des moyens de correction (4) pour diminuer l'écart mutuel entre les courants des configurations de transistors (2.1,...,2.N+1), caractérisé en ce que
 - le nombre de configurations de transistors (2.1,...,2.N+1) est au moins supérieur de un au nombre nécessaire de courants et
 - les moyens de correction (4) sont conçus pour rendre le courant de chaque configuration de transistors (2.1,...,2.N+1) de façon cyclique égal à un courant de référence (6) en réglant la tension de commande du transistor de commande de la configuration de transistors concernée et
 - dans chaque période du cycle, une configuration de transistors corrigée (2.1,...,2.N+1) est échangée contre une configuration de transistors non corrigée (2.1,...,2.N+1) au moyen d'un circuit de commutation (7), de telle manière que la configuration de transistors devant être corrigée soit enlevée du circuit de source de courant.
2. Circuit de source de courant selon la revendication 1, caractérisé en ce que chaque configuration des transistors est constituée par le transistor de commande (T2) ayant un condensateur (C2) disposé entre ses électrodes de grille et de source.
 3. Circuit de source de courant selon la revendication 2, caractérisé en ce que le condensateur est constitué par la capacité de grille-source du transistor de commande concerné.
 4. Circuit de source de courant selon la revendication 2 ou 3, caractérisé en ce que les moyens de correction (4) comportent des moyens pour fournir le courant de référence (6) à l'électrode de drain du transistor de commande (T2) et des moyens de contre-réaction (16) disposés entre les électrodes de drain et de grille pour commander la tension aux bornes du condensateur de façon que le premier courant (I2) soit égal au courant de référence

(Iref).

5. Circuit de source de courant selon la revendication 2 ou 3, caractérisé en ce que les moyens de correction comportent:
 - une première résistance (R1) pour convertir le courant de référence en une tension de référence,
 - une deuxième résistance (R2) pour convertir le premier courant en une deuxième tension et
 - des moyens de contre-réaction (16) reliés aux première (R1) et deuxième (R2) résistances et au condensateur (C2) pour régler la tension aux bornes du condensateur (C2) de façon que la deuxième tension soit égale à la tension de référence.
6. Circuit de source de courant selon la revendication 4, caractérisé en ce que les moyens de contre-réaction comportent des moyens de réglage pour régler la tension sur l'électrode de drain du transistor de commande.
7. Circuit de source de courant selon la revendication 6, caractérisé en ce que les moyens de réglage comportent un transistor suiveur de courant (T6) dont l'électrode de source est couplée à l'électrode de drain du transistor de commande (T2), qui a son électrode de grille couplée à une borne de tension de référence (Vref) et son électrode de drain couplée à une source de courant de polarisation (20).
8. Circuit de source de courant selon la revendication 1, caractérisé en ce que chaque configuration de transistors est constituée par le transistor de commande (T2) ayant un condensateur (C2) disposé entre ses électrodes de grille et de source, et une source de courant à transistor (B2) pour fournir un deuxième courant, le courant de la configuration de transistors étant égal à la somme des premier et deuxième courants.
9. Circuit de source de courant selon la revendication 8, caractérisé en ce que le condensateur est constitué par la capacité de grille-source du transistor de commande concerné (T2).
10. Circuit de source de courant selon la revendication 8 ou 9, caractérisé en ce que les moyens de correction comportent des moyens pour fournir la différence entre le courant de référence et le deuxième courant à l'électrode de drain du transistor de commande (T2), et



des moyens de contre-réaction disposés entre les électrodes de drain et de grille pour régler la tension aux bornes du condensateur de façon que la somme des premier et deuxième courants soit égale au courant de référence.

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11. Circuit de source de courant selon la revendication 8 ou 9, caractérisé en ce que les moyens de correction comportent des moyens pour fournir la différence entre le courant de référence et le deuxième courant à l'électrode de drain d'un deuxième transistor (T5) ayant sa jonction de grille-source disposée en parallèle avec la jonction de grille-source du transistor de commande (T2), et des moyens de contre-réaction disposés entre les électrodes de drain et de grille du deuxième transistor (T5) pour commander la tension aux bornes du condensateur (C2) de façon que la somme du courant du deuxième transistor (T5) et du deuxième courant soit égale au courant de référence.

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12. Circuit de source de courant selon la revendication 8 ou 9, caractérisé en ce que les moyens de correction comportent:

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- une première résistance (R1) pour convertir le courant de référence en une tension de référence,
- une deuxième résistance (R2) pour convertir la somme des premier et deuxième courants en une deuxième tension et
- des moyens de contre-réaction reliés aux première (R1) et deuxième (R2) résistances et au condensateur (C2) pour régler la tension aux bornes du condensateur (C2) de façon que la deuxième tension soit égale à la tension de référence.

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13. Circuit de source de courant selon la revendication 11, caractérisé en ce que les moyens de contre-réaction comportent des moyens de réglage pour régler la tension sur l'électrode de drain du transistor de commande.

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14. Circuit de source de courant selon la revendication 13, caractérisé en ce que les moyens de réglage comportent un transistor suiveur de courant (T6) ayant son électrode de source couplée à l'électrode de drain du transistor de commande (T2), dont l'électrode de grille est couplée à une borne de tension de référence (V_{ref}) et dont l'électrode de drain est couplée à une source de courant de polarisation (20).

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15. Convertisseur numérique-analogique comportant un circuit de source de courant selon l'une

quelconque des revendications précédentes et comportant en outre:

- une borne d'entrée (111) pour un signal numérique,
- une borne de sortie (125) pour sommer une pluralité de courants choisis, déterminés par ledit signal numérique,
- un registre de données (110) couplé à ladite borne d'entrée (111),
- un réseau de commutation (100) commandé par ledit registre de données et couplant de façon sélective à ladite borne de sortie (125) une pluralité de sorties dudit circuit de source de courant.