

SPECIFICATION

Camera focussing system

- 5 The present invention relates to a focussing system for a photographic or cinematographic camera having a lens for adjusting the lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, a pair of radiation receiving elements for receiving radiation produced by the radiation emitting element, a means for terminating each measuring cycle, a signal processing circuit responsive to the radiation receiving elements, an integrator circuit responsive to the output of the signal processing circuit, the integrator circuit being reset at the end of each measuring cycle, and a threshold circuit responsive to the output of the integrator circuit and including memory elements, the output of the memory elements being connected for adjusting the lens and/or indicating when the lens is focussed.

The system set out above is described in our co-pending application No. 7912436.

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- According to the present invention there is provided in a photographic or cinematographic camera having a lens, a focussing system for adjusting the lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, a pair of radiation receiving elements for receiving radiation produced by the radiation emitting element, a means for terminating each measuring cycle, a signal processing circuit responsive to the radiation receiving element, an integrator circuit responsive to the output of the signal processing circuit, the integrator circuit being reset at the end of each measuring cycle, and a threshold circuit responsive to the output of the integrator circuit, the threshold stages each of which is associated with a respective one of the receiving elements, a pair of second threshold stages each of which is associated with a respective one of the receiving elements and a pair of memory elements each of which is associated with a respective one of the receiving elements, each memory element having a data input responsive to the output of the associated first threshold stage and having a control input responsive to the output of the two second threshold stages and also to the measuring cycle terminating means, the threshold values of the first and second threshold stages being set so that during any measuring cycle the

threshold value of a first threshold stage is reached before that of the associated second threshold stage, and the output of the memory elements being connected for adjusting the lens and/or indicating when the lens is focussed.

- During any measuring cycle, after a sufficient number of pulses have been produced by the pulse generator circuit, the threshold value of one of the first threshold stages may be reached. The output signals of this threshold circuit will then be applied to the data input of the associated memory element. After this, the integration circuit will continue to integrate the output of the signal processing circuit until the threshold value of the associated second threshold stage is reached. When this happens, the second threshold circuit will apply a signal to the control input of the memory element with the result that a signal will appear at the output of this memory element. Then, at the end of the measuring cycle, the measuring cycle terminating means will cause the integration circuit to be reset. In the event of not reaching the threshold value of either of the second threshold stages, the measuring cycle terminating means will apply a signal to both of the memory elements.

- Preferably, the measuring cycle terminating means has a control input responsive to the output of the two second threshold stages, the measuring cycle terminating means resetting the integrator circuit and terminating the measuring cycle before the expiry of the basic measuring cycle period upon receiving a signal from one of the second threshold stages.

- This has the advantage of not needing to wait for the end of the basic measuring cycle in the event of a signal appearing at the output of one of the second threshold stages.

- Conveniently, the measuring cycle terminating means includes a counter clocked by pulses from the output of the pulse generator circuit and arranged to count a predetermined number of pulses, the counter having a reset input responsive to the output of the two second threshold stages.

- The integrator circuit may comprise two individual integrator sections, each section being associated with a respective one of the receiving elements, and under the control of pulses produced by the pulse generator circuit, each integrator section being responsive to the output of the signal processing circuit when a pulse is expected from its associated receiving element.

- In a preferred arrangement, each integrator section comprises an operational amplifier having a feed-back integration capacitor and each threshold stage comprises a voltage comparator responsive to an associated one of the integrator sections.

- Preferably the system includes means for limiting the output signal of the signal processing circuit to the integrator circuit in at

least the close-up range of the camera. This has the advantage of providing a uniform integration characteristic in the close-up range of the camera and consequently uniform accuracy in focussing in this range.

The limiting means may comprise a signal limiting stage in the signal processing circuit.

Alternatively, the limiting means may comprise a regulating circuit for controlling the radiation intensity of the radiation emitting element in accordance with the radiation incident on the receiving elements.

Each memory element of the threshold circuit may comprise a flip-flop.

In each integrator section the feed-back capacitor may be discharged at the end of each measuring cycle by a semiconductor switch element.

Conveniently, the measuring cycle terminating means includes a gate having one input responsive to the outputs of the second threshold stages and another input responsive to the output of the counter, and a delay circuit, the input of which is responsive to the output of the gate, the output of which is connected to the reset input of the counter, and an intermediate point of which is connected to the control inputs of the semiconductor switch elements.

The present invention will now be described in more detail, by way of example, with reference to Figs. 1 and 2 of the accompanying drawings which show a circuit diagram of a focussing system embodying the present invention.

Referring now to Fig. 1, the system then shown comprises a battery 1, the negative pole of which is connected to a negative supply line and the positive pole of which is connected by a switch 2 to the anode of the diode 5. The cathode of diode 5 is connected through a resistor 6 to a positive supply line. A capacitor 3 is connected in parallel with battery 1 and switch 2 and a further capacitor 4 is connected between the positive and negative supply lines, the capacitors 3 and 4, and the diode 5 and the resistor 6 serving to stabilize the voltage between the positive and negative supply lines. Two equal value resistors 7 and 8 are connected in series between the positive and negative supply lines and the junction between these two resistors is connected to an earth line, the potential of which is exactly midway between the positive and negative supply lines. The system includes a pair of radiation receiving elements in the form of infra-red sensitive diodes 9, 10. The cathode of infra-red sensitive diode 9 is connected to the inverting input of an operational amplifier 11, the non-inverting input of which is connected to earth, and the cathode of infra-red sensitive diode 10 is connected to the inverting input of an operational amplifier 12, the non-inverting input of which is connected to earth.

A pair of resistors 13, 14 connected in series provide a feed-back connection between the output of amplifier 11 and its inverting input and a further pair of resistors 15 and 16 connected in series provide a feed-back connection between the output of amplifier 12 and its non-inverting input. These resistors determine the amplification factor of amplifiers 11, and 12. The junction of resistors 13 and 14 and the junction of resistors 15, and 16 are connected to earth by capacitors 17 and 18 respectively. As the impedance of capacitors 17 and 18 decreases with increasing frequency, the amplification factor of the two amplifiers 11 and 12 increases with frequency. It is preferred that the resistors 13 and 14 have identical values to the resistors 15 and 16, and also that the capacitors 17 and 18 are of equal value.

The output of amplifier 11 is connected by a coupling capacitor 19 to the inverting input of an operational amplifier 20, the output of which is connected by a feed-back resistor 21 to its non-inverting input, and the non-inverting input is connected to earth by a resistor 22. The resistors 21 and 22 determine the amplification factor of this amplifier, which functions as an AC amplifier.

Likewise, the output of amplifier 12 is connected by a coupling capacitor 24 to the non-inverting input of an operational amplifier 23, the output of which is connected by a feed-back resistor 25 to its non-inverting input, and the non-inverting input of which is connected to earth by a resistor 26. The resistors 25, 26 determine the amplification factor of this amplifier and this amplifier also functions as an AC amplifier.

The outputs of amplifiers 20 and 23 are connected respectively to switching elements 28 and 29 of a first multiplex stage 27. The outputs of switching elements 28 and 29 are connected together to the input of a high pass active filter comprising an operational amplifier 30, resistors 31 and 32, and capacitors 33 and 34. The high pass filter is arranged so that interference signals of mains frequency and also interference signals from incandescent and fluorescent lamps having a frequency which is double mains frequency are filtered out.

The high pass filter 30 to 34 is connected by coupling capacitor 35 to an AC amplifier consisting of an operational amplifier 36 and feed-back resistors 37 and 38.

The output of the operational amplifier 36 is connected to the inputs of two switching elements 40 and 41 of a second multiplex stage 39. The output of switching element 40 is connected to a terminal B and the output of switching element 41 is connected to a terminal C.

The amplifiers 11, 12, 20, 23, 30 and 36 together with their associated elements form a signal processing circuit.

The system further includes a generator circuit comprising a square wave pulse generator 42, the output of which is connected to the clock input of a counter 43. The output of pulse generator 42 and also the Q4 output of counter 43 are connected to the two inputs of an AND gate 34, the output of which is connected to the reset input R of counter 43. The Q3 output of counter 43 is connected to the clock input of a D flip-flop 45, the Q output of which is connected to its D input.

The Q output of flip-flop 45 is connected to the control terminal of switching element 28 and also to one input of an AND gate 46. The Q output of flip-flop 45 is connected to the control terminal of switching element 29 and to one input of an AND gate 47.

The remaining inputs of AND gates 46, and 47 are connected together to the output of a delay circuit 48, having timing elements 49 and 50. The input of the delay circuit 48 to 50 is connected to the output of an AND gate 51, one input of which is connected to the Q4 output of the counter 43 and the other input of which is connected to a timing circuit comprising a capacitor 52 and a resistor 53.

The output of AND gate 51 is also connected by a resistor 54 to the base of a transistor 55, the emitter of which is connected to the base of an output transistor 56. The collector of transistor 56 is connected to the cathode of an infra-red emitting diode 57, the anode of which is connected to the positive terminal of battery 1 through switch 2. The emitter of transistor 56 is connected to the negative supply line by a resistor 58.

The infra-red emitting diode 57 forms a radiation emitting element and is arranged in the camera so that, in use, it emits a measuring beam towards the subject to be photographed. The infra-red sensitive diodes 9 and 10 are arranged to receive the infra-red radiation reflected back from the subject towards the camera. The diodes 9 and 10 are located behind a lens, not shown, which is coupled to the camera focussing system and which causes the received radiation to fall equally on the two diodes 9 and 10 when the main objective lens of the camera is focussed.

The output of AND gate 47 is connected to the switching element 41 and the output of AND gate 46 is connected to the switching element 40 of the second multiplex stage 39.

In order to regulate the intensity of the radiation emitted by the diode 57, a regulating circuit is provided, this regulating circuit comprises a pair of resistors 60 and 60' connected in series as a potential divider between the positive and negative supply lines, the junction of resistors 60 and 60' being connected by a capacitor 59 to the output of amplifier 36 and also to the anode of a diode 61, the cathode of which is connected to the negative supply line by a capacitor 62 and a resistor 63, connected in paral-

lel, and also to the base of a transistor 64. The collector of transistor 64 is connected to the positive supply line and the emitter is connected to the base of a transistor 65. The collector of transistor 65 is connected to the base of transistor 55 and the emitter of transistor 65 is connected to the negative supply line.

In the regulating circuit, the transistor 65, and consequently the transistor 56 is controlled in accordance with the intensity of the radiation falling on the diodes 9 and 10. Within the close-up range of the camera, the regulating circuit thus ensures that the intensity of the radiation falling on the diodes 9 and 10 has an almost constant value.

This regulating circuit also has the effect of regulating or limiting the signal appearing at the output of the signal processing circuit, that is at terminals B and C. In an alternative embodiment, not shown, the signal appearing at the output of the signal processing circuit is regulated by a signal limiting stage forming part of the signal processing circuit.

The output of switching element 40 is connected by terminal B to the input of an integration section, which forms one half of an integrator circuit, and which comprises an operational amplifier 66, a feed-back integration capacitor 67 and a resistor 68. The output of the integrator stage 66 to 68 is connected to the inverting inputs of two operational amplifiers 69 and 95 which function as voltage comparators. Three resistors 70, 71 and 72 are connected in series between the positive and negative supply lines and function as a potential divider chain, the junction F of resistors 70 and 71 being connected to the non-inverting input of amplifier 69. The inverting input of operational amplifier 66 can be connected to earth by means of the collector emitter path of a transistor 73.

The output of amplifier 69 is connected to the D input of a D flip-flop 84.

There is also provided a delay circuit comprising gates 76 and 77, resistors 78 and 79, and capacitors 80 and 81.

The base of transistor 73 is connected through a resistor 82 to an intermediate point, namely the junction of gate 76 and resistor 79, of the delay circuit 76 to 81. The input of the delay circuit 76 to 81 is connected to the output of an OR-gate 85, one input of which is connected to the Qm output of a counter 83. The reset input R of counter 83 is connected to the output of the delay circuit. The clock input of the counter 83 is connected by terminal E to the output of delay circuit 48 to 50.

The delay circuit 76 to 81 together with the counter 83 comprises a means for terminating the end of each measuring cycle as will become clear from the description which follows.

The other input of OR-gate 85 is connected

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to the output of an OR-gate 96, the output of OR-gate 96 also being connected to the control or clock input of flip-flop 84. A first input of OR-gate 96 is connected to the output of operational amplifier 95 and the second input of OR-gate 96 is connected to the output of OR-gate 85.

The switching element 41 of the second multiplex stage 39 is connected by way of terminal C to the input of a second integrator section comprising an operational amplifier 86, a feed-back integration capacitor 87 and a resistor 88. The resistor 88 is connected to the inverting input of the operational amplifier 86 and the non-inverting input of the amplifier is connected to earth by way of terminal D. The first and second integrator sections together form the integrator circuit. The integration capacitor 67 and 87 are of equal value, the resistors 66 and 88 are of equal value, and the amplifiers 66 and 86 are of identical structure. The output of operational amplifier 86 is connected to the inverting inputs of a pair of operational amplifiers 74 and 75, which function as voltage comparators.

The non-inverting input of operational amplifier 74 is connected to the junction F of resistors 70 and 71. The voltage comparator 74 thus has the same threshold value as the voltage comparator 69. The inverting input of amplifier 86 can be connected to earth by the collector emitter path of a transistor 93, the base of which is connected through a resistor 94 in the delay circuit 76 to 81.

In an alternative arrangement, not shown, the collector emitter paths of transistors 73 and 93 are connected respectively in parallel with the capacitors 67 and 87.

The output of operational amplifier 74 is connected to the D input of a D flip-flop 97, the clock input of which is connected to the output of OR-gate 96.

The non-inverting inputs of amplifiers 95 and 75 are connected to the junction H of resistors 71 and 72 of the potential dividing chain 70, 71 and 72. Thus, the amplifiers 95 and 75 have the same threshold value. The output of amplifier 75 is connected to the third input of OR-gate 96.

The amplifiers 69, 95, 74 and 75 together with the potential divider chain 70, 71 and 72 and the flip-flops 84 and 97 form a threshold circuit, the amplifiers 69 and 74 forming a pair of first threshold stages and the amplifiers 95 and 75 forming a pair of second threshold stages.

During each measuring cycle, the outputs of the amplifiers 66 and 86 gradually decrease as these amplifiers integrate the signals applied to their inputs. The threshold values of the operational amplifiers 69 and 74 are determined by the potential at junction point F. Normally, the threshold value of one of the amplifiers 69 and 74 will be reached first in any one measuring cycle but, when the lens is

focussed, the threshold values of these two amplifiers could be reached almost simultaneously.

The threshold values of the operational amplifiers 95 and 75 are lower than those of the amplifier 69 and 74. In consequence, during any measuring cycle the threshold values of these amplifiers 95 and 75 is reached at a later stage than that of the amplifiers 69 and 74. The difference in the threshold values between the amplifiers 69 and 74 and the amplifiers 95 and 75 is selected so that if the camera lens is focussed within an acceptable tolerance range during any measuring cycle the input to the amplifiers 69 and 74 will reach their threshold value before the threshold value is reached of one of the amplifiers 95 and 75.

If during a measuring cycle the input to the amplifier 69 reaches its threshold value, the output of this amplifier will go high thereby providing a high signal at the D input of flip-flop 84. If at a later stage in the measuring cycle the threshold value of amplifier 95 is reached, then the output of this amplifier will go high with a result that the output of OR-gate 96 will go high thereby applying a high positive signal to the clock input of flip-flop 84. This will result in the Q-output of flip-flop 84 going high.

Similarly, in the case of the amplifiers 74 and 75, if the inputs to these amplifiers reach their threshold value during a measuring cycle, a high positive signal will be applied to the D input of flip-flop 97 and also to the clock input of flip-flop 97, with a result that the Q output of this flip-flop will go low.

If during a measuring cycle the threshold value of amplifier 69 and also the threshold value of amplifier 74 is reached before the threshold value of one of the amplifiers 95 and 75, a high positive signal will be applied to both of the flip-flops 84 and 97 before these flip flops receive a positive signal at their clock inputs.

The high positive signal appearing at the output of OR-gate 96 is also applied to the OR-gate 85, and then through the delay circuit 76 to 81 to the reset input R of counter 83, thereby resetting this counter.

If during a measuring cycle the inputs to the amplifiers 69 and 74 do not reach their threshold values, the Qm output of counter 83 will provide a high signal to OR-gate 85 which will be transmitted through the delay circuit 76 to 81 to the reset input R. Also, the OR-gate 85 will apply a high signal to the OR-gate 96 which will be transmitted to the clock inputs of flip-flops 84 and 97. Since the outputs of the amplifiers 69 and 74 have not gone high, the signal applied to the clock inputs of flip-flops 84 and 97 will cause the Q output of flip-flop 84 to go low and Q output of flip-flop 97 to go high.

During any measuring cycle, the integration

circuit including amplifiers 66 and 86 will be reset immediately before the counter 83 is reset.

The Q output of flip-flop 84 is connected to one input of an AND-gate 101, the second input of which is connected to the Q output of flip-flop 97. The output of AND-gate 101 is connected by a resistor 102 to the base of a transistor 103, the collector of which is connected by a light emitting diode 104 and a resistor 105 to the positive supply line, and the emitter of which is connected to the negative supply line. The light emitting diode 104 indicates to the user of the camera, when it is energised, that the lens must be rotated in the direction of the arrow in order to focus it.

The Q output of flip-flop 84 is connected to one input of an AND-gate 106, the second input of which is connected by a switch 107 and a resistor to the negative supply line. The output of AND-gate 106 is connected by a resistor 108 to the base of a transistor 109, the collector of which is connected by a light emitting diode 110 and a resistor 111 to the positive supply line, and the collector of which is connected through a resistor to the negative supply line. The light emitting diode 110 indicates to the user of a camera, when it is energised, that the lens must be rotated in the direction indicated in order to obtain focus.

The switch 107 is closed when the lens is at its infinity setting.

Although in the example described above the output of flip-flops 84 and 97 are used to control the two light emitting diodes 104 and 110, the output of flip-flops 84 and 97 could alternatively or in addition be used to control a servo motor which adjusts the focus of the lens.

CLAIMS

1. In a photographic or cinematographic camera having a lens, a focussing system for adjusting the lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, a pair of radiation receiving elements for receiving radiation produced by the radiation emitting element, a means for terminating each measuring cycle, a signal processing circuit responsive to the radiation receiving elements, an integrator circuit responsive to the output of the signal processing circuit, the integrator circuit being reset at the end of each measuring cycle, and a threshold circuit responsive to the output of the integrator circuit, the threshold circuit comprising a pair of first threshold stages each of which is associated with a respective one of the receiving elements, a pair of second threshold stages each of which

is associated with a respective one of the radiation receiving elements and a pair of memory elements each of which is associated with a respective one of the radiation receiving elements, each memory element having a data input responsive to the output of the associated first threshold stage and having a control input responsive to the outputs of the two second threshold stages and also the measuring cycle terminating means, the threshold values of the first and second threshold stages being set so that during any measuring cycle the threshold value of a first threshold stage is reached before that of the associated second threshold stage, and the outputs of the measuring elements being connected for adjusting the lens and/or indicating when the lens is focussed.

2. A system as claimed in claim 1 in which the measuring cycle terminating means has a control input responsive to the output of the two second threshold stages, the measuring cycle terminating means resetting the integrator circuit and terminating the measuring cycle before the expiry of the basic measuring cycle period upon receiving a signal from one of the second threshold stages.

3. A system as claimed in claim 1 or claim 2 in which the measuring cycle terminating means includes a counter clocked by pulses derived from the output of the pulse generator circuit and arranged to count a predetermined number of pulses, the counter having a reset input responsive to the output of the two second threshold stages.

4. A system as claimed in any one of the preceding claims in which the integrator circuit comprises two individual integrator sections, each section being associated with a respective one of the receiving elements and, under the control of pulses produced by the pulse generator circuit, each integrator section being responsive to the output of the signal processing circuit when a pulse is expected from its associated receiving element.

5. A system as claimed in claim 4 in which each integrator section comprises an operational amplifier having a feedback integrator capacitor and in which each threshold stage comprises a voltage comparator responsive to an associated one of the integrator sections.

6. A system as claimed in any one of the preceding claims including means for limiting the output signal of the signal processing circuit to the integrator circuit in at least the close-up range of the camera.

7. A system as claimed in claim 6 in which the limiting means comprises a signal limiting stage in the signal processing circuit.

8. A system as claimed in claim 6 in which the limiting means comprises a regulating circuit for controlling the radiation intensity of the radiation emitting elements in accordance with the radiation incident on the



circuit including amplifiers 66 and 86 will be reset immediately before the counter 83 is reset.

The Q output of flip-flop 84 is connected to one input of an AND-gate 101, the second input of which is connected to the Q output of flip-flop 97. The output of AND-gate 101 is connected by a resistor 102 to the base of a transistor 103, the collector of which is connected by a light emitting diode 104 and a resistor 105 to the positive supply line, and the emitter of which is connected to the negative supply line. The light emitting diode 104 indicates to the user of the camera, when it is energised, that the lens must be rotated in the direction of the arrow in order to focus it.

The $\bar{Q}$ output of flip-flop 84 is connected to one input of an AND-gate 106, the second input of which is connected by a switch 107 and a resistor to the negative supply line. The output of AND-gate 106 is connected by a resistor 108 to the base of a transistor 109, the collector of which is connected by a light emitting diode 110 and a resistor 111 to the positive supply line, and the collector of which is connected through a resistor to the negative supply line. The light emitting diode 110 indicates to the user of a camera, when it is energised, that the lens must be rotated in the direction indicated in order to obtain focus.

The switch 107 is closed when the lens is at its infinity setting.

Although in the example described above the output of flip-flops 84 and 97 are used to control the two light emitting diodes 104 and 110, the output of flip-flops 84 and 97 could alternatively or in addition be used to control a servo motor which adjusts the focus of the lens.

CLAIMS

1. In a photographic or cinematographic camera having a lens, a focussing system for adjusting the lens in accordance with the distance between a subject to be photographed and the camera and/or for indicating when the lens is focussed, the system including a pulse generator circuit, a radiation emitting element driven by the pulse generator circuit for producing a measuring beam, a pair of radiation receiving elements for receiving radiation produced by the radiation emitting element, a means for terminating each measuring cycle, a signal processing circuit responsive to the radiation receiving elements, an integrator circuit responsive to the output of the signal processing circuit, the integrator circuit being reset at the end of each measuring cycle, and a threshold circuit responsive to the output of the integrator circuit, the threshold circuit comprising a pair of first threshold stages each of which is associated with a respective one of the receiving elements, a pair of second threshold stages each of which

is associated with a respective one of the radiation receiving elements and a pair of memory elements each of which is associated with a respective one of the radiation receiving elements, each memory element having a data input responsive to the output of the associated first threshold stage and having a control input responsive to the outputs of the two second threshold stages and also the measuring cycle terminating means, the threshold values of the first and second threshold stages being set so that during any measuring cycle the threshold value of a first threshold stage is reached before that of the associated second threshold stage, and the outputs of the measuring elements being connected for adjusting the lens and/or indicating when the lens is focussed.

2. A system as claimed in claim 1 in which the measuring cycle terminating means has a control input responsive to the output of the two second threshold stages, the measuring cycle terminating means resetting the integrator circuit and terminating the measuring cycle before the expiry of the basic measuring cycle period upon receiving a signal from one of the second threshold stages.

3. A system as claimed in claim 1 or claim 2 in which the measuring cycle terminating means includes a counter clocked by pulses derived from the output of the pulse generator circuit and arranged to count a predetermined number of pulses, the counter having a reset input responsive to the output of the two second threshold stages.

4. A system as claimed in any one of the preceding claims in which the integrator circuit comprises two individual integrator sections, each section being associated with a respective one of the receiving elements and, under the control of pulses produced by the pulse generator circuit, each integrator section being responsive to the output of the signal processing circuit when a pulse is expected from its associated receiving element.

5. A system as claimed in claim 4 in which each integrator section comprises an operational amplifier having a feedback integrator capacitor and in which each threshold stage comprises a voltage comparator responsive to an associated one of the integrator sections.

6. A system as claimed in any one of the preceding claims including means for limiting the output signal of the signal processing circuit to the integrator circuit in at least the close-up range of the camera.

7. A system as claimed in claim 6 in which the limiting means comprises a signal limiting stage in the signal processing circuit.

8. A system as claimed in claim 6 in which the limiting means comprises a regulating circuit for controlling the radiation intensity of the radiation emitting elements in accordance with the radiation incident on the

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receiving elements.

9. A system as claimed in any one of the preceding claims in which each memory element of the threshold circuit comprises a flip-flop.

5 10. A system as claimed in claim 5 or in any one of claim 6 to 9 when dependent on claims in which in each integrator section the feedback capacitor is discharged at the end of each measuring cycle by a semi-conductor switch element.

11. A system as claimed in claim 10 when dependent on claim 3 in which the measuring cycle terminating means includes a 15 gate having one input responsive to the outputs of the second threshold stages and another input responsive to the output of the counter, and a delay circuit, the input of which is responsive to the output of the gate, 20 the output of which is connected to the reset input of the counter, and an intermediate point of which is connected to the control inputs of the semi-conductor switch elements.

25 12. In a photographic or cinematographic camera a focussing system substantially as hereinbefore described with reference to and as shown in Figs. 1 and 2 of the accompanying drawings.