

Description

The present invention relates to a method for polishing a silicon wafer to provide an extremely flat, damage-free mirror surface, which is especially suitable for semiconductor devices. The present invention also relates to a method for producing a silicon wafer.

Conventionally, in order to provide a mirror surface and the flatness required for semiconductor device fabrication, polishing is accomplished by a mechanochemical process in which a polishing pad of synthetic fibers, an alkaline polishing fluid, and fine silica particles are used. The silicon wafer is supported between a base plate covered with a polishing pad and a carrier plate to which the wafer adheres, or the wafer may be held between two base plates covered with polishing pads about 2 mm thick. A pressure of 100 to 500 g/cm² is applied to the wafer surface. The wafer is mechanochemically polished by means of relative movement between the base plate and the wafer, as for example, by the rotation of the base plate and the carrier plate, supplying polishing fluid which includes an alkaline fluid in a pH range of 10 to 12, and using polishing particles of high-purity silica of 0.02 to 0.10 μ m (cf. US-A-3740900; US-A-4692223).

With such a method, the pressure is applied to the surface of the wafer via the cloth, whereby a uniform pressure is generated over the entire surface owing to the compressive deformation of cloth, and therefore the differences in rate of among areas of the silicon wafer are small.

However, a problem develops because of the generally uniform rate of removal as shown in Fig. 1. In Fig. 1, a silicon wafer 20 includes a surface 22 to be polished which has a variation in thickness. In the polishing process, a volume 24 of the silicon wafer is removed and a surface 26 is exposed. According to the generally uniform rate of removal, thickness variations still remain on the surface 26. In order to finish the surface 26 to the flatness required for VLSI fabrication, much time is spent removing a relatively large amount of material. Recently, to meet the stricter thickness variation specifications, harder and harder polishing cloths (pads) are employed, however reducing the total thickness variation to less than 2 μ m is nonetheless very difficult.

Recently, in device development design, smaller size and higher integration are increasingly important considerations. To meet these requirements, we must consider the use of a step-and-repeat-camera in the photolithographic process, as well as for example, focusing, condition of the surface with which focusing must coincide during resist coating, film formation, and etching off. Prac-

tically, for example, to produce a submicron device, thickness variations of wafers at 15 x 15 mm or 20 x 20 mm must be less than 1 μ m, preferably 0.5 μ m. The requirement for total thickness variation of a wafer used must now therefore be less than 2 μ m.

In recent years, the dielectric-isolation structure, the Bi-CMOS structure, and the SOI (Silicon-On-Insulator) structure devices were developed. In the SOI structure, an island of monocrystalline silicon, polycrystalline silicon, or amorphous silicon is formed; and a dielectric or insulator area is also formed on a substrate. It is necessary to polish the silicon island and the dielectric area to be damage-free according to the method described above. In addition, the thickness of the silicon island must be adjusted to the device to be fabricated. The circuit defined by the silicon island must have a desirable properties.

In the method, for example, a substrate made of a monocrystalline silicon or polycrystalline silicon is first prepared as shown in Fig. 2. An insulator raised pattern 32 of SiO₂ is formed on one surface of the substrate 30. Next, by means of a thin-film forming method such as CVD (Chemical Vapor Deposition), a silicon layer 34 made of monocrystalline or polycrystalline silicon is formed on the surface of the substrate 30 in such a manner that the insulator pattern 32 is surrounded by the substrate 30 and the silicon layer 34, so that the unfinished silicon wafer shown in Fig. 2 is produced with some thickness variations.

To flatten the surface of the wafer, three methods are known, (a) the etch-back method, (b) the reflow method, and (c) the selective polishing method. However, the etched back method requires much processing and only produces a tolerance of $\pm$ 0.2 μ m, and the reflow method is applied only to the wiring process. Therefore, the selective polishing process is the only solution.

After initial processing, the selective polishing method is applied to finish the outer surface of the silicon layer 34, so that the silicon layer is surrounded laterally by the insulator pattern as shown in Fig. 3. In the polishing method, when the polishing removal reaches the insulator pattern 32, the removal rate becomes very low. Then, the polishing pad is deformed compressively to excavate the silicon island 40 as shown in Fig. 3. (In Fig. 3, numbers 36 and 38 designate the surfaces of the silicon wafer before and after polishing, respectively.) Therefore, the thicknesses of the crystal island on which circuit is later to be fabricated varies, differing from an identical finished wafer shown in Fig. 4, and thus defocusing is occurred in the photolithographic process.

If it is necessary that the device structure has a certain thickness remaining over the insulator pat-

tern 32 as shown in Fig. 5. Polishing with the polishing pad must not flatten the surface 38 nor control the thickness of the remained silicon layer 34 over the insulator pattern 32.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method for polishing a silicon wafer for providing a damage-free mirror surface with a degree of flatness suitable for submicron lithography, and to provide selective polishing of an unfinished wafer which has some warp and thickness variation produced by the arrangement of the insulator pattern and the deposition of the silicon.

Another object of the present invention is to provide a method for producing a silicon wafer for providing a mirror surface with a degree of flatness suitable for submicron lithography and having a desired thickness.

These objects are achieved by a method according to claim 1. Claims 2-9 describe preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side elevation showing a silicon wafer with surfaces before and after polishing by the prior art.

Fig. 2 is a side elevation showing another silicon wafer before polishing by a method for producing a silicon wafer which is compared with the present invention.

Fig. 3 is a side elevation showing the silicon wafer of Fig. 2 with surfaces before and after polishing.

Fig. 4 is a side elevation showing an example of a desired silicon wafer of desired dimensions after polishing.

Fig. 5 is a side elevation showing another example of a desired silicon wafer of desired dimensions after polishing.

Fig. 6 is a side elevation showing a silicon wafer with surfaces before and after polishing using a method for polishing according to the first embodiment of the present invention.

Figs. 7 through 10 are side elevations showing a production process of a silicon wafer according to a hypothetical method of a second embodiment of the present invention.

Figs. 11 through 13 are side elevations showing a production process of a silicon wafer according to an actual method of the second embodiment of the present invention.

Figs. 14 through 16 are side elevations showing a producing process for a silicon wafer according to another actual method of the second embodiment of the present invention.

Fig. 17 is a side elevation showing a polishing block used in the above embodiments.

Fig. 18 is an enlarged side elevation showing a portion of the block determined by XVIII area in Fig. 17.

Figs. 19 and 20 are graphs showing the thickness variation in a comparison between the second embodiment and another method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to the accompanying drawings, various preferred embodiments will be described hereinafter.

First Embodiment

In Fig. 6, an unfinished silicon wafer 50 includes a surface 52 and has thickness variations so that the degree of flatness is outside the necessary range of tolerance. A ceramic polishing block, having a surface of a high degree of flatness is installed on a rotating apparatus. On the ceramic polishing block, polishing fluid is supplied which has an alkaline fluid in a pH of 10 to 11 and high-purity silica particles dispersed in the alkaline fluid. The wafer 50 is directly in contact with the planar surface of a polishing block at a pressure of 50 to 200 g/cm² in such a manner that the surface 52 faces generally parallel to the planar surface of the polishing block. The wafer surface is subjected to friction and the abrasion of the silica particles as well as the polishing surface of the block by rotating the polishing block, and then chemically etching. This process is well-known as mechanochemical polishing. The polishing block is made of a ceramic material to preventing the wafer from being contaminated and for the rigidity thereof. The ceramic material, which is preferably harder than the silicon wafer and more resistant to mechanochemical polishing than silicon, is preferably selected from SiO₂, Al₂O₃, Si₃N₄, and SiC. For example, if the ceramic material is Al₂O₃, its hardness is preferably more than 1,100 kg/mm² (Vickers hardness with 500 g), its bending strength is preferably more than 3,000 kg/cm², its compressive strength is preferably more than 19,000 kg/cm², and its Young's modulus is preferably more than 2.5x10⁵ kg/cm². The grain size of the polishing particles is preferably less than 0.05 μm. More preferably, the polishing particles are 0.01 to 0.02 μm in grain size.

According to the processing under the above conditions, elevated portions of the surface 52 are primarily removed. Therefore, the finished silicon wafer 54 has a damage-free mirror surface 56 of desirable flatness.

[Experiment 1]

A silicon wafer of a circular cross section and diameter of 125 mm was used which had a total thickness variation of 11 μm , and a maximum surface roughness of 2.5 μm . A polishing block, having a circular cross section of which the diameter was 250 mm and a thickness of 20 mm was used; the polishing block had a total thickness variation of 5 μm , and maximum surface roughness of 0.01 μm . The ceramic polishing block was made of high-purity quartz having a purity of 99.99%. The polishing fluid included an alkaline liquid of pH 10.2 and high-purity silica particles of 0.02 μm size at 5.0% by weight. The silicon wafer was applied to the polishing block at 100 g/cm². The polishing fluid was mounted on a metal plate at a temperature of 35 $\pm$ 1 $^\circ$ C, so that the silicon wafer was polished at 35 $^\circ$ C.

Under the above conditions, the silicon wafer was polished for 5 minutes. Only the upper portions of the surface of the silicon wafer were mirror-polished. Other portions of the surface were not polished.

After polishing for 35 additional minutes, the entire surface of the silicon wafer was mirror-polished. The total thickness variation of the polished silicon wafer was very small at 1.3 μm .

[Experiment 2]

In order to make a comparison with the results of Experiment 1, the silicon wafer was polished by the prior method with a polishing pad, and the thickness variation produced was measured. In Experiment 2, a 2mm-thick pad fabricated of an unsaturated polyester fiber was provided on a metal polishing block. A 125mm-diameter silicon wafer was used which had a total thickness variation of 9 μm , and a maximum surface roughness of 2 μm . Other conditions were the same as those in Experiment 1.

After polishing for 5 minutes, the entire surface of the silicon wafer was mirror-polished. The entire surface, which included some raised and some lower portions appeared to have been polished at a uniform rate.

After polishing for 35 additional minutes, the surface was polished to a mirror surface with a surface roughness of 1.5 nm. The total thickness variation of the polished silicon wafer however was still 5 μm . Therefore, the total thickness variation was not reduced using the method of Experiment 2.

Second Embodiment

A method for producing a silicon wafer according to a second embodiment of the present invention is described hereinafter with reference to Figs. 7 through 10.

As shown in Fig. 7, a substrate 60 made of monocrystalline silicon, polycrystalline silicon, or high-purity quartz is first prepared. Then, an insulator raised pattern 64 is formed on the surface of the substrate 60 by photolithography and dry etching. The thickness of the raised pattern 64 is determined to be the same as the thickness of the silicon layer as described in the following. Then, if necessary, an insulator raised pattern 62, which has a lesser height than the raised pattern 64, is formed by another photolithography and dry etching process. The raised patterns 62 and 64 are made of a material that is more resistant than silicon to mechanochemical polishing such as Al₂O₃, SiO₂, SiC, or Si₃N₄. The entire area of the raised pattern 64 is preferably in a range of 1 to 20% of the area of the substrate 60.

Next, by using chemical vapor deposition, a polysilicon layer 66 is formed on the surface of the substrate 60 in such a manner that the raised patterns 62 and 64 are surrounded by the substrate 60 and the polysilicon layer 66, so that the unfinished silicon wafer 67 with some thickness variation shown in Fig. 8 is produced.

Then, a mechanochemical polishing method similar to that of the first embodiment is applied to finish the outer surface of the silicon layer 66, so that a volume 68 is removed which is above the raised pattern 64, as shown in Fig. 9. The removal rate of mechanochemical polishing is greater in the upper portion of the silicon layer 66 which does not enclose any raised patterns 62 and 64. The removal rate is then rapidly reduced when the polishing reaches the top of the higher raised pattern 64 made of the more resistant mechanochemical polishing material. Then, the polishing is terminated, thereby providing a finished silicon wafer 70 which has a silicon layer 72 of prescribed thickness and a damage-free mirror surface 74 shown in Fig. 10. The thickness of the silicon layer 72 is the same as the height of the raised pattern 64. Therefore, the raised pattern 64 functions as a braking structure during polishing.

Figs. 19 and 20 are graphs to compare between the second embodiment and with another method. Fig. 19 depicts the result according to the second embodiment. Fig. 20 depicts the result of the method using a polishing pad. From the figures, it is apparent that there is a much greater variation between the levels of the silicon islands and the SiO₂ portions in the method utilizing the polishing pad.

With the method for producing a silicon wafer of the second embodiment, the height of the raised pattern 64 is determined by the desirable thickness of the silicon layer 72, and therefore the method facilitates microlithography and produces uniform volumes of the polysilicon layer 72.

[Example 1]

Referring to Figs. 11 through 13, an actual example of the second embodiment will be described hereinafter. First, a substrate 80, shown in Fig. 11, made of monocrystalline silicon was prepared. On the surface of the substrate 80, grooves 82 of 0.1 μm depth were formed to be spaced 10 μm apart. Next, a 0.1 μm -thick surface layer 84 of the substrate 80, including the walls of the grooves 82, was thermally oxidized to SiO_2 . The walls 86 of the grooves 82, which were also oxidized to SiO_2 , projected inward to the wafer 90. Next, polysilicon layer 114 was formed by a CVD method in such a manner that the polysilicon layer 114 covers the SiO_2 layer 84 and fills to the grooves 82. The surface of the polysilicon layer 114 was polished according to the above-mentioned method (Experiment 1), and was flattened thereby. The substrate 80 is hereinafter referred to as wafer 90.

A substrate 100, also made of monocrystalline silicon, was prepared as is also shown in Fig. 11. The substrate 100 is hereinafter referred to as wafer 110.

After preparation, the wafers 90 and 110 were bonded to a bonded substrate 112 by means of a hydrogen junction at 1,100° C, in such a manner that the surface layers 84 and 102 faced each other.

Next, the bonded substrate 112 was ground from the outer surface of the portion (substrate) 80, to form the unfinished wafer 120 shown in Fig. 12, until the thickness of the portion (substrate) 80 equaled about 2 μm .

Furthermore, a polishing apparatus with a 250 mm-diameter of circular cross section which had a total thickness variation of 5 μm , and a maximum surface roughness of 0.01 μm , was used. The polishing block was made of high-purity Al_2O_3 . The polishing fluid included an alkaline fluid of pH 10.5 and was 5% by weight high-purity silica particles of 0.02 μm . The unfinished wafer 120 was pressed at 100 g/cm² against the rotating polishing block in such a manner that the surface of the polishing block and the outer surface of the portion (substrate) 80 of the wafer 120 faced each other while supplying polishing fluid to the surface of the polishing block. After about 20 minutes of polishing, the polishing block came into contact with the polycrystalline silicon layer 114 and the raised SiO_2 walls 86. At that time, the polishing was generally

interrupted by the walls 86, and the polishing process was thereby stopped.

In the above polishing process, as shown in Fig. 13, a finished wafer 130 with an silicon island 132 (the silicon portion of the substrate 80) was produced which had a thickness generally equal to the depth of the grooves 82. When the finished wafer 130 was used as an SOI semiconductor substrate for a 256K SRAM device, the resulting device was of very high quality.

[Example 2]

Figs. 14 through 16 show another actual example of the second embodiment. In this example, a 1.0 μm layer of thermally oxidized SiO_2 was formed on a surface of a silicon crystal substrate. Then, a two-step photolithographic and etching process was applied to the SiO_2 surface layer, so that a substrate 140 shown in Fig. 14 was formed. The substrate 140 had a partially exposed monocrystalline silicon region 142 and a SiO_2 layer 144 in such a manner that some of the raised pattern 146 served as the braking structure for the mechanochemical polishing were partially formed on the surface of the SiO_2 layer 144.

Next, by means of a selective epitaxial method, a silicon crystal layer was grown only from the exposed surface 142, so as to surround the SiO_2 layer 144.

The conditions for the selective epitaxial method are as follows. The substrate 140 was heat-annealed at a temperature of 1,100° C for 10 minutes in an atmosphere of hydrogen gas. Then, the substrate 140 was treated in an atmosphere of SiH_2Cl_2 gas, HCl gas, and H_2 gas under 30 Torr (4000 Pa) at 900° C; this resulted in the growth of the epitaxial silicon layer 148 from the region 142. The growth rate of the epitaxial silicon was 0.1 $\mu\text{m}/\text{min}$ in both vertical and lateral directions.

The epitaxial silicon layer 148 was polished to the same degree as in the previous example. After about 20 minutes of polishing, the polishing block came into contact with the SiO_2 raised pattern 146. Then, the rate of removal was greatly reduced by the raised pattern 146, and the polishing process was thereby interrupted.

With the above polishing process, as shown in Fig. 16, the thickness of the silicon layer 152 on a finished wafer 150 was equal to the height of the raised pattern 146 plus the thickness of the SiO_2 layer 144. When the finished wafer 150 was used for an advanced semiconductor device, the device was of very high quality on the silicon layer 152.

In the present invention, the silicon layer to be polished could be made of monocrystalline silicon, polycrystalline silicon, or amorphous silicon. The present invention does not limit the relative move-

ment between the ceramic block and the wafer must be the rotation of the ceramic block. Alternatively, the holder which supports the wafer could be moved, or both the polishing block and the holder could be moved.

While in the above embodiments the reverse surface of the substrate is not polished, the invention is not so limited. Since the polishing can be simultaneously applied to two surfaces of the substrate if the substrate is held in engagement with a ring-shaped holder so that the holder holds the lateral edge of the substrate. In this case, both surfaces are polished by means of two polishing blocks facing parallel to each other. Therefore, in the second embodiment, the SiO₂ portions 62, 64, 84, 86, 144, and, 146 can be formed on both the obverse and reverse surfaces of the substrate.

In order to better understand the configuration of the polishing block, an example thereof is shown in Figs. 17 and 18. The polishing block is a circular plate with straight grooves 160 spaced 30 mm apart, extending bidirectionally like a checkerboard. The grooves 160 functions as drains for the by-products of the mechanochemical polishing and as retainers for the polishing particles, as well as supply polishing fluid to every portion of the wafer surface. The grooves 160 are 1.5 mm in width. The total thickness variation of the surface of the polishing block is 1 μ m.

Claims

1. A method for polishing a silicon wafer (50) by using a polishing block for mechanochemical polishing of a silicon wafer (50), the polishing block comprising:
 - a polishing surface for mechanochemical polishing said silicon wafer (50), said polishing surface made of a ceramic material, said polishing surface being harder than the silicon wafer and more resistant to mechanochemical polishing than the silicon wafer (50), and said polishing surface having a maximum surface roughness of less than 0.02 μ m, comprising the steps of:
 - (a) supplying a polishing fluid including an alkaline fluid and polishing particles of high-purity silica dispersed in the alkaline fluid to the polishing surface of the polishing block;
 - (b) pressing a silicon wafer (50) in contact with said polishing surface; and
 - (c) moving at least one of the said silicon wafer (50) and the said polishing surface relative to the other, thereby mechanochemically polishing said silicon wafer (50).
2. Method according to claim 1, characterized in that the method further comprises the use of a second polishing block.
3. A method for producing a silicon wafer (50, 67), the method comprising the steps of:
 - (a) preparing a substrate (60), which has at least one planar surface, for a silicon wafer (67);
 - (b) forming a raised pattern (62, 64) on said planar surface of the prepared substrate (60), the raised pattern (62, 64) being made of a material which is more resistant to mechanochemical polishing than silicon;
 - (c) forming a silicon layer (52, 66) on said planar surface of said prepared substrate (60), the silicon layer (52, 66) cooperating with said substrate (60), to surround said raised pattern (62, 64), thereby forming an unfinished silicon wafer (50, 67);
 - (d) supplying a polishing fluid including an alkaline fluid and polishing particles of high-purity silica dispersed in the alkaline fluid to the polishing surface of a polishing block for mechanochemical polishing of a silicon wafer (50), the polishing block comprising a polishing surface for mechanochemical polishing said silicon wafer (50), said polishing surface made of a ceramic material, said polishing surface being harder than the silicon wafer and more resistant to mechanochemical polishing than the silicon wafer (50), and said polishing surface having a maximum surface roughness of less than 0.02 μ m;
 - (e) pressing said unfinished silicon wafer (50, 67) into contact with said polishing surface in such a manner that a side of said silicon layer (52, 66) faces to the polishing surface; and
 - (f) moving at least one of the said unfinished silicon wafer (50, 67) and the said polishing surface relative to the other, thereby polishing mechanochemically said unfinished silicon wafer (50, 67).
4. Method according to claim 3, characterized in that said polishing particles are of a grain size less than 0.05 μ m.
5. Method according to claim 3 or 4, characterized in that said forming steps of the raised pattern (62, 64) and the silicon layer (52, 66) further comprise the steps of:
 - preparing a second substrate (80) made of silicon which has at least one planar surface;
 - forming grooves (82, 86) on said planar surface of said second prepared substrate (80);

ment between the ceramic block and the wafer must be the rotation of the ceramic block. Alternatively, the holder which supports the wafer could be moved, or both the polishing block and the holder could be moved.

While in the above embodiments the reverse surface of the substrate is not polished, the invention is not so limited. Since the polishing can be simultaneously applied to two surfaces of the substrate if the substrate is held in engagement with a ring-shaped holder so that the holder holds the lateral edge of the substrate. In this case, both surfaces are polished by means of two polishing blocks facing parallel to each other. Therefore, in the second embodiment, the SiO_2 portions 62, 64, 84, 86, 144, and, 146 can be formed on both the obverse and reverse surfaces of the substrate.

In order to better understand the configuration of the polishing block, an example thereof is shown in Figs. 17 and 18. The polishing block is a circular plate with straight grooves 160 spaced 30 mm apart, extending bidirectionally like a checkerboard. The grooves 160 functions as drains for the by-products of the mechanochemical polishing and as retainers for the polishing particles, as well as supply polishing fluid to every portion of the wafer surface. The grooves 160 are 1.5 mm in width. The total thickness variation of the surface of the polishing block is 1 μm .

Claims

1. A method for polishing a silicon wafer (50) by using a polishing block for mechanochemical polishing of a silicon wafer (50), the polishing block comprising:
 - a polishing surface for mechanochemical polishing said silicon wafer (50), said polishing surface made of a ceramic material, said polishing surface being harder than the silicon wafer and more resistant to mechanochemical polishing than the silicon wafer (50), and said polishing surface having a maximum surface roughness of less than 0.02 μm , comprising the steps of:
 - (a) supplying a polishing fluid including an alkaline fluid and polishing particles of high-purity silica dispersed in the alkaline fluid to the polishing surface of the polishing block;
 - (b) pressing a silicon wafer (50) in contact with said polishing surface; and
 - (c) moving at least one of the said silicon wafer (50) and the said polishing surface relative to the other, thereby mechanochemically polishing said silicon wafer (50).
2. Method according to claim 1, characterized in that the method further comprises the use of a second polishing block.
3. A method for producing a silicon wafer (50, 67), the method comprising the steps of:
 - (a) preparing a substrate (60), which has at least one planar surface, for a silicon wafer (67);
 - (b) forming a raised pattern (62, 64) on said planar surface of the prepared substrate (60), the raised pattern (62, 64) being made of a material which is more resistant to mechanochemical polishing than silicon;
 - (c) forming a silicon layer (52, 66) on said planar surface of said prepared substrate (60), the silicon layer (52, 66) cooperating with said substrate (60), to surround said raised pattern (62, 64), thereby forming an unfinished silicon wafer (50, 67);
 - (d) supplying a polishing fluid including an alkaline fluid and polishing particles of high-purity silica dispersed in the alkaline fluid to the polishing surface of a polishing block for mechanochemical polishing of a silicon wafer (50), the polishing block comprising a polishing surface for mechanochemical polishing said silicon wafer (50), said polishing surface made of a ceramic material, said polishing surface being harder than the silicon wafer and more resistant to mechanochemical polishing than the silicon wafer (50), and said polishing surface having a maximum surface roughness of less than 0.02 μm ;
 - (e) pressing said unfinished silicon wafer (50, 67) into contact with said polishing surface in such a manner that a side of said silicon layer (52, 66) faces to the polishing surface; and
 - (f) moving at least one of the said unfinished silicon wafer (50, 67) and the said polishing surface relative to the other, thereby polishing mechanochemically said unfinished silicon wafer (50, 67).
4. Method according to claim 3, characterized in that said polishing particles are of a grain size less than 0.05 μm .
5. Method according to claim 3 or 4, characterized in that said forming steps of the raised pattern (62, 64) and the silicon layer (52, 66) further comprise the steps of:
 - preparing a second substrate (80) made of silicon which has at least one planar surface;
 - forming grooves (82, 86) on said planar surface of said second prepared substrate (80);



forming a layer (84) at least at the bottom of said grooves (82, 86) the layer (84) being made of a material which is more resistant to mechanochemical polishing than silicon;
forming a silicon layer (114) which has an outer surface of said surface of said more resistant layer (84) in such a manner that the silicon layer (114) covers the surface of said more resistant layer (84),
polishing said outer surface of said silicon layer (114); and
bonding said first substrate (60, 110) and said second substrate (80) in such a manner that said planar surface of said first substrate (60, 100) and said outer surface of said silicon layer (114) of said second substrate (80) face each other whereby said bottom of said grooves (82, 86) being as said raised pattern (62, 64).

6. Method according to any of claims 3 to 5, characterized in that the method further comprises the use of a second polishing block according to any of claims 1 to 3, thereby polishing mechanochemically a pair of surfaces of said unfinished wafer (50, 67).
7. Method according to any of claims 1 to 6, characterized in that the polishing particles are of a grain size less than 0.05 nm.
8. Method according to any of claims 1 to 7, characterized in that the ceramic material of the polishing block is selected from the group consisting of SiO_2 , Al_2O_3 , SiC , and Si_3N_4 .
9. Method according to any of claims 3 to 8, characterized in that the surface of the polishing block has a plurality of grooves.

Patentansprüche

1. Verfahren zum Polieren eines Siliciumwafers (50) unter Verwendung eines Polierblocks für das mechanochemische Polieren eines Siliciumwafers (50), wobei der Polierblock umfaßt:
Eine Polieroberfläche zum mechanochemischen Polieren des Siliciumwafers (50), wobei die Polieroberfläche aus einem keramischen Material hergestellt ist, und die Polieroberfläche härter ist als der Siliciumwafer und beständiger gegen ein mechanochemisches Polieren als der Siliciumwafer (50), und die Polieroberfläche eine maximale Oberflächenrauheit von weniger als $0,02\mu\text{m}$ hat, umfassend die Stufen:
(a) Aufbringen einer Polierflüssigkeit einschließlich einer alkalischen Flüssigkeit und

von Polierteilchen aus hochreinem Siliciumdioxid dispergiert in der alkalischen Flüssigkeit zum Polieren der Oberfläche des Polierblocks;

- (b) Aufpressen des Siliciumwafers (50) in Kontakt mit der Polieroberfläche; und
(c) Bewegen des Siliciumwafers (50) und/oder der Polieroberfläche relativ zueinander unter mechanochemischem Polieren des Siliciumwafers (50).
2. Verfahren gemäß Anspruch 1, dadurch gekennzeichnet, daß das Verfahren weiterhin die Verwendung eines zweiten Polierblocks umfaßt.
3. Verfahren zur Herstellung eines Siliciumwafers (50, 67), wobei das Verfahren die Stufen umfaßt:
(a) Herstellen eines Substrats (60) mit wenigstens einer planaren Oberfläche für eine Siliciumwafer (67);
(b) Ausbilden eines erhabenen Musters (62, 64) auf der planaren Oberfläche des hergestellten Substrats (60), wobei das erhabene Muster (62, 64) aus einem Material hergestellt ist, das gegenüber mechanochemischem Polieren beständiger ist als Silicium;
(c) Ausbilden einer Siliciumschicht (52, 66) auf der planaren Oberfläche des hergestellten Substrats (60), wobei die Siliciumschicht (52, 66) mit dem Substrat (60) kooperiert und das erhabene Muster (62, 64) umgibt unter Ausbildung eines unfertigen Siliciumwafers (50, 67);
(d) zur Verfügungstellen einer Polierflüssigkeit, die ein alkalisches Fluid einschließt und von von Polierteilchen aus hochreinem Siliciumdioxid dispergiert in der alkalischen Flüssigkeit zum Polieren der Oberfläche eines Polierblocks zum mechanochemischen Polieren eines Siliciumwafers (50), wobei der Polierblock umfaßt eine Polieroberfläche zum mechanochemischen Polieren des Siliciumwafers (50), die Polieroberfläche aus einem keramischen Material hergestellt ist, wobei die Polieroberfläche härter ist als der Siliciumwafer und gegenüber mechanochemischem Polieren beständiger ist als der Siliciumwafer (50), wobei die Polieroberfläche eine maximale Oberflächenrauheit von weniger als $0,02\mu\text{m}$ hat;
(e) Pressen des unfertigen Siliciumwafers (50, 67) in Kontakt mit der Polieroberfläche derart, daß die Seite der Siliciumschicht 52, 66) der Polieroberfläche gegenüberliegt;
(f) Bewegen des unfertigen Siliciumwafers (50, 67) und/oder der Polieroberfläche rela-



tiv zueinander unter mechanochemischem Polieren des unfertigen Siliciumwafers (50, 67).

4. Verfahren gemäß Anspruch 3, dadurch **gekennzeichnet**, daß die Polierteilchen eine Korngröße von weniger als 0,05µm haben. 5
5. Verfahren gemäß Anspruch 3 oder 4, dadurch **gekennzeichnet**, daß die Ausbildungsstufe des erhabenen Musters (62, 64) und der Siliciumschicht (52, 66) weiterhin die Stufen umfaßt: 10
 - Herstellen eines zweiten Substrats (80) aus Silicium mit wenigstens einer planaren Oberfläche; 15
 - Ausbilden von Rillen (82, 86) auf der planaren Oberfläche des zweiten hergestellten Substrats (80);
 - Ausbilden einer Schicht (84) wenigstens am Boden der Rillen (82, 86), wobei die Schicht (84) aus einem Material hergestellt ist, daß gegenüber mechanochemischem Polieren beständiger ist als Silicium; 20
 - Ausbilden einer Siliciumschicht (114), die eine äußere Oberfläche an der Oberfläche der beständigeren Schicht (84) hat derart, daß die Siliciumschicht (114) die Oberfläche der beständigeren Schicht (84) bedeckt, 25
 - Polieren der äußeren Oberfläche der Siliciumschicht (114) und
 - Binden des ersten Substrats (60, 110) und des zweiten Substrats (80) derart, daß die planare Oberfläche des ersten Substrats (60, 100) und die äußere Oberfläche der Siliciumschicht (114) auf dem zweiten Substrat (80) sich gegenüberstehen, wodurch der Boden der Rillen (82, 86) das erhabene Muster (62, 64) darstellt. 30
6. Verfahren gemäß einem der Ansprüche 3 bis 5, dadurch **gekennzeichnet**, daß das Verfahren weiterhin umfaßt die Verwendung eines zweiten Polierblocks gemäß einem der Ansprüche 1 bis 3, wodurch das mechanochemische Polieren eines Paares von Oberflächen des unfertigen Wafers (50, 67) erfolgt. 40
7. Verfahren gemäß einem der Ansprüche 1 bis 6, dadurch **gekennzeichnet**, daß die Polierteilchen eine Korngröße von weniger als 0,05 nm haben. 50
8. Verfahren gemäß einem der Ansprüche 1 bis 7, dadurch **gekennzeichnet**, daß das keramische Material des Polierblocks ausgewählt ist aus der Gruppe bestehend aus SiO₂, Al₂O₃, SiC und Si₃N₄. 55

9. Verfahren gemäß einem der Ansprüche 3 bis 8, dadurch **gekennzeichnet**, daß die Oberfläche des Polierblocks eine Vielzahl von Rillen hat.

Revendications

1. Procédé pour polir une tranche de silicium (50) par l'utilisation d'un bloc de polissage pour polir mécano-chimiquement une tranche de silicium (50), le bloc de polissage comprenant :
 - une surface de polissage pour polir mécano-chimiquement ladite tranche de silicium (50), ladite surface de polissage étant constituée d'un matériau de céramique, ladite surface de polissage étant plus dure que la tranche de silicium et plus résistante au polissage mécano-chimique que la tranche de silicium (50), et ladite surface de polissage ayant une rugosité superficielle maximale inférieure à 0,02 µm, comprenant les étapes consistant à :
 - (a) délivrer un fluide de polissage incluant un fluide alcalin et des particules de polissage de silice de haute pureté dispersées dans le fluide alcalin, à la surface de polissage du bloc de polissage,
 - (b) appliquer une tranche de silicium (50) en contact avec ladite surface de polissage, et
 - (c) déplacer au moins soit ladite tranche de silicium (50) soit ladite surface de polissage l'une rapport à l'autre, polissant de ce fait mécano-chimiquement ladite tranche de silicium (50).
2. Procédé selon la revendication 1, caractérisé en ce que le procédé comprend de plus l'utilisation d'un second bloc de polissage.
3. Procédé pour produire une tranche de silicium (50, 67), le procédé comprenant les étapes consistant à :
 - (a) préparer un substrat (60), qui a au moins une surface plane, pour une tranche de silicium (67),
 - (b) former un motif surélevé (62, 64) sur ladite surface plane du substrat préparé (60), le motif surélevé (62, 64) étant constitué d'un matériau qui est plus résistant au polissage mécano-chimique que le silicium,
 - (c) former une couche de silicium (52, 66) sur ladite surface plane dudit substrat préparé (60), la couche de silicium (52, 66) coopérant avec ledit substrat (60) pour entourer ledit motif surélevé (62, 64) formant de ce fait une tranche de silicium non finie (50, 67),
 - (d) délivrer un fluide de polissage incluant un fluide alcalin et des particules de polis-



sage de silice de haute pureté dispersées dans le fluide alcalin, à la surface de polissage du bloc de polissage pour polir mécano-chimiquement une tranche de silicium (50), le bloc de polissage comprenant une surface de polissage pour polir mécano-chimiquement ladite tranche de silicium (50), ladite surface de polissage étant constituée d'un matériau de céramique, ladite surface de polissage étant plus dure que ladite tranche de silicium et plus résistante au polissage mécano-chimique que ladite tranche de silicium (50) et ladite surface de polissage ayant une rugosité superficielle maximale inférieure à $0,02 \mu\text{m}$,
 (e) appliquer ladite tranche de silicium non finie (50, 67) en contact avec ladite surface de polissage de manière telle qu'une face de ladite tranche de silicium (52, 66) soit en regard de la surface de polissage, et
 (f) déplacer au moins soit la tranche de silicium non finie (50, 67) soit ladite surface de polissage l'une par rapport à l'autre, en polissant de ce fait mécano-chimiquement ladite tranche de silicium non finie (50, 67).

4. Procédé selon la revendication 3, caractérisé en ce que lesdites particules de polissage sont d'une dimension de grain inférieure à $0,05 \mu\text{m}$.

5. Procédé selon la revendication 3 ou 4, caractérisé en ce que lesdites étapes de formation du motif surélevé (62, 64) et de ladite couche de silicium (52, 66) comprennent de plus les étapes consistant à :

préparer un second substrat (80) préparé avec du silicium qui a au moins une surface plane,

former des rainures (82, 86) sur ladite surface plane dudit second substrat préparé (80),

former une couche (84) au moins au fond desdites rainures (82, 86), la couche (84) étant constituée d'un matériau qui est plus résistant au polissage mécano-chimique que le silicium,

former une couche de silicium (114) qui comporte une surface extérieure de ladite surface de ladite couche plus résistante (84) de manière telle que la couche de silicium (114) recouvre la surface de ladite couche plus résistante (84),

polir ladite surface extérieure de ladite couche de silicium (114) et

coller ledit premier substrat (60, 110) et ledit second substrat (80) de manière telle que ladite surface plane dudit premier substrat (60, 100) et ladite surface extérieure de ladite couche de silicium (114) dudit second substrat (80) soient en regard l'une par rapport à l'autre

d'où il résulte que ledit fond desdites rainures (82, 86) constitue ledit motif surélevé (62, 64).

6. Procédé selon l'une quelconque des revendications 3 à 5, caractérisé en ce que le procédé comprend de plus l'utilisation d'un second bloc de polissage selon l'une quelconque des revendications 1 à 3, polissant de ce fait mécano-chimiquement une paire de surfaces de ladite tranche non finie (50, 67).

7. Procédé selon l'une quelconque des revendications 1 à 6, caractérisé en ce que les particules de polissage sont d'une taille de grain inférieure à $0,05 \text{ nm}$.

8. Procédé selon l'une quelconque des revendications 1 à 7, caractérisé en ce que le matériau de céramique du bloc de polissage est choisi dans le groupe qui est constitué de SiO_2 , Al_2O_3 , SiC et Si_3N_4 .

9. Procédé selon l'une quelconque des revendications 3 à 8, caractérisé en ce que la surface du bloc de polissage comporte une multitude de rainures.

