## CLAIMS

What is claimed is:

1. A memory access popularity statistics method, wherein the method is performed by a controller and comprises:

determining a first address based on an obtained access request, wherein the access request indicates an operation performed on a memory of a computer device by an application program run by a processor in the computer device in which the controller is located, and the first address is a physical address in the memory;

collecting statistics about access frequency of accessing a data block in which the first address is located, wherein a size of the data block is a multiple of unit storage space in the memory that is accessible to the processor; and

determining access popularity of the data block based on the access frequency.

2. The method according to claim 1, wherein the collecting statistics about access frequency of accessing a data block in which the first address is located comprises:

collecting statistics about the access frequency of accessing the data block in which the unit storage space to which the first address belongs is located.

3. The method according to claim 2, wherein the method further comprises:

identifying a second address based on an address of the data block in which the first address is located and an address mapping relationship, wherein the second address indicates a location, in the controller, at which the access frequency of accessing the data block is stored, and the address mapping relationship indicates a mapping relationship between the address of the data block and an address of storage space in which the access frequency is stored.

4. The method according to claim 3, wherein the method further comprises:

identifying the second address based on a third address indicated by the processor and the address mapping relationship, to obtain the access frequency of accessing the data block, wherein the third address is determined based on the second address.

5. The method according to any one of claims 1 to 4, wherein the size of the data block is a size of one page in the memory that is accessible to the processor.

6. The method according to any one of claims 1 to 4, wherein the size of the data block is a size of an interleaved data block in the memory that is accessible to the processor in an interleaving manner, and the interleaving manner means that the processor in the computer device distributes, to a plurality of memories for an operation, data of the operation performed by the running application program on the memory of the computer device.

7. The method according to any one of claims 1 to 6, wherein a size of the unit storage space

is a size of a cache line when the processor accesses the memory.

8. A memory access popularity statistics apparatus, comprising:

a communication module, configured to determine a first address based on an obtained access request, wherein the access request indicates an operation performed on a memory of a computer device by an application program run by a processor in the computer device in which a controller is located, and the first address is a physical address in the memory; and

a statistics module, configured to collect statistics about access frequency of accessing a data block in which the first address is located, wherein a size of the data block is a multiple of unit storage space in the memory that is accessible to the processor, wherein

the statistics module is further configured to determine access popularity of the data block based on the access frequency.

9. The apparatus according to claim 8, wherein when collecting statistics about the access frequency of accessing the data block in which the first address is located, the statistics module is specifically configured to:

collect statistics about the access frequency of accessing the data block in which the unit storage space to which the first address belongs is located.

10. The apparatus according to claim 9, wherein the statistics module is further configured to:

identify a second address based on an address of the data block in which the first address is located and an address mapping relationship, wherein the second address indicates a location, in the controller, at which the access frequency of accessing the data block is stored, and the address mapping relationship indicates a mapping relationship between the address of the data block and an address of storage space in which the access frequency is stored.

11. The apparatus according to claim 10, wherein the statistics module is further configured to:

identify the second address based on a third address indicated by the processor and the address mapping relationship, to obtain the access frequency of accessing the data block, wherein the third address is determined based on the second address.

12. The apparatus according to any one of claims 8 to 11, wherein the size of the data block is a size of one page in the memory that is accessible to the processor.

13. The apparatus according to any one of claims 8 to 11, wherein the size of the data block is a size of an interleaved data block in the memory that is accessible to the processor in an interleaving manner, and the interleaving manner means that the processor in the computer device distributes, to a plurality of memories for an operation, data of an operation performed by the running application program on the memory of the computer device.

14. The apparatus according to any one of claims 8 to 13, wherein a size of the unit storage

space is a size of a cache line when the processor accesses the memory.

15. A controller, wherein the controller comprises a storage unit and a processing unit, the storage unit is configured to store a group of computer instructions, and when executing the group of computer instructions, the processing unit performs an operation step of the method according to any one of claims 1 to 7, to identify access frequency of accessing a data block in a memory by an application program.

16. The controller according to claim 15, wherein the controller is a register clock driver RCD in the memory of a computer device.

17. The controller according to claim 15, wherein the controller is an extended controller in the memory of a computer device.

18. A chip, comprising a processor and a power supply circuit, wherein the power supply circuit is configured to supply power to the processor, and the processor is configured to perform an operation step of the method according to any one of claims 1 to 7.

19. A memory, wherein the memory comprises a storage device and the controller according to any one of claims 15 to 17, the storage device is configured to store a group of computer instructions, and when executing the group of computer instructions, the controller performs an operation step of the method according to any one of claims 1 to 7, to identify access frequency of accessing a data block in a memory by an application program.

20. A mainboard, wherein the mainboard comprises the controller according to any one of claims 15 to 17, and the controller performs an operation step of the method according to any one of claims 1 to 7, to identify access frequency of accessing a data block in a memory by an application program.