

ABSTRACT

A semiconductor memory device includes a device isolation pattern on a substrate and defining a first active section, a first storage node pad on the first active section, a word line in the substrate and extending across the first active section, a bit line on the first storage node pad and crossing over the word line, a storage node contact on one side of the bit line and adjacent to the first storage node pad, and an ohmic layer between the storage node contact and the first storage node pad. A bottom surface of the ohmic layer is rounded.

FIG. 3A