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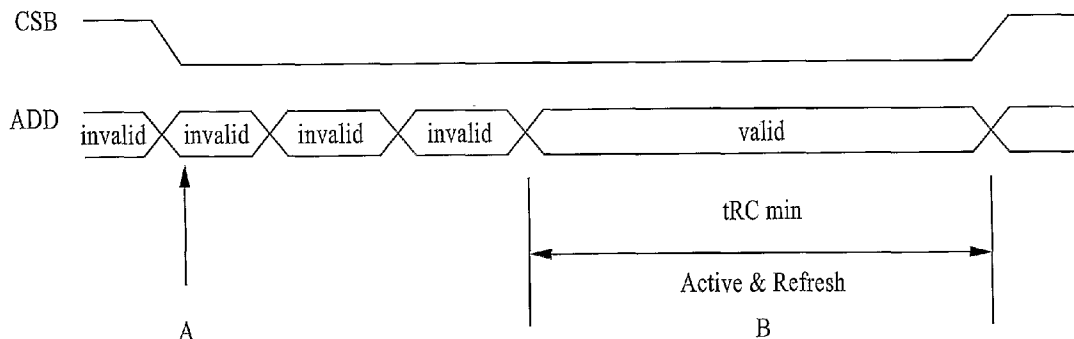
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(54) Title: 1T1C SRAM



(57) Abstract: Memory circuits and methods are described providing an interface with high density dynamic memory (DRAM), such 1T1C (1 transistor and 1 capacitor) memory cells, providing full compatibility with static memory (SRAM). The circuitry overcomes the shortcomings with DRAM, such as associated with the restore and refresh operations, which have prevented full utilization of DRAM cores with SRAM compatible devices. The circuit can incorporate a number of inventive aspects, either singly or more preferably in combination, including a pulsed word line structure for limiting the maximum page mode cycle time, an address duration compare function with optional address buffering, and a late write function wherein the write operation commences after the write control signals are disabled.

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