(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 May 2011 (05.05.2011)

PCT

(10) International Publication Number
WO 2011/051078 A1

(51) International Patent Classification:
H01L 21/762 (2006.01)

(21) International Application Number:
PCT/EP2010/064604

(22) International Filing Date:
30 September 2010 (30.09.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09 57662 30 October 2009 (30.10.2009) FR

(71) Applicant *(for all designated States except US)*: **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique des Fontaines, Chemin des Franques, F-38190 Bernin (FR).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **KERDILES, Sébastien** [FR/FR]; 281, Impasse de Pageonnière, F-38330 Saint-ismier (FR). **REYNAUD, Patrick** [FR/FR]; 20, rue Flora Tristan, F-38400 Saint Martin D'heres (FR).

(74) Agents: **WARCOIN,AHNER,TEXIER,LE FORESTIER,CALLON DE LAMARCK,COLLIN,TETAZ,FAIVRE PETIT** et al.; Cabinet Regimbeau, 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

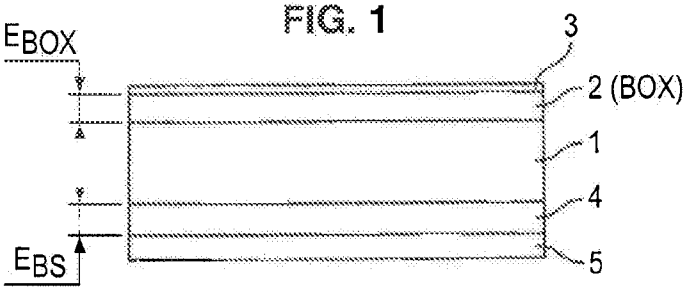
— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: METHOD FOR CONTROLLING THE DISTRIBUTION OF STRESSES IN A SEMICONDUCTOR-ON-INSULATOR TYPE STRUCTURE AND CORRESPONDING STRUCTURE.

FIG. 1



(57) **Abstract**: The present invention relates to a method for controlling the distribution of the stresses in a structure of the semiconductor-on-insulator type during its manufacturing, which includes a thin layer of semiconducting material (3) on a supporting substrate (1), an insulating layer (2, 4) being present on each of the front and rear faces of the supporting substrate (1), the insulating layer on the front face (2) forming at least one portion of a thick buried insulator (BOX), a manufacturing method according to which it is proceeded with adhesive bonding of said thin layer (3) on said supporting substrate (1), characterized by the fact that, prior to adhesive bonding, it is proceeded with covering of the insulating layer (4), on the rear face of said supporting substrate with a distinct material (5), withstanding deoxidations, a material which, in combination with this insulating layer (4) on the rear face of the supporting substrate (1), at least partly compensates for the stress exerted by the buried insulator (BOX) on the supporting substrate (1).

WO 2011/051078 A1