

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR INTEGRATED CIRCUITS

(71) We, NIPPON ELECTRIC COMPANY, LIMITED, a Company duly organized and existing under the laws of Japan and having its executive office at 7-15, Shiba Gochome, Minato-ku, Tokyo-to, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor integrated circuits.

As known, semiconductor integrated circuits are such that active elements and passive elements are incorporated in one main surface of a semiconductor substrate. These elements are connected to each other via a metal layer disposed on an insulation film, thereby forming an electronic circuit capable of switching operation or amplifying operation. In such semiconductor integrated circuits, various parasitic effects are observed because various elements are incorporated into one substrate. This causes operating failure. For example, in an MOS semiconductor integrated circuit, each circuit element is electrically isolated within the substrate from the other and is connected thereto by way of wiring. Practically, however, a parasitic channel is produced between the elements which are supposed to be isolated from one another, if a wiring metal layer to which a high voltage is applied is present on the insulation film located on the substrate between the elements. As a result, a parasitic leakage current is produced therein.

The reason why the parasitic leakage current is produced is because an inversion layer is induced on the substrate surface due to a high voltage applied to the wiring metal layer on the insulation film between the elements, and thus a conduction channel is formed between the elements.

The threshold voltage V_T of the MOS field effect transistor used for the MOS (metal-oxide-semiconductor) integrated circuit is expressed as

$$V_T = \frac{Q_{ss} + Q_b}{e} t,$$

where

Q_{ss} stands for effective surface charge per unit area;

Q_b , bulk charge per unit area in channel depletion layer;

e , dielectric constant of insulation film; and
 t , thickness of insulation film.

In general, the insulation film used in an MOS type semiconductor integrated circuit device, of which the active element is usually a P-channel MOS transistor, is thermally oxidized silicon oxide. The threshold voltage V_T of the MOS transistor is controlled by the thickness of the silicon oxide film of its gate region. More specifically, when the thickness of the silicon oxide film of the gate region is about 0.2 microns, the threshold voltage V_{T1} is about 3 to 5 volts. (Note: The threshold voltage V_T in the gate region is denoted by V_{T1} . All values shown hereinafter will be of absolute value.)

Usually, the thickness of the silicon oxide film between the elements is about 1.5 microns, and the threshold voltage V_{T2} in this area is around 20 volts. (Note: The threshold voltage V_T between the elements is denoted by V_{T2} .)

When a voltage above V_{T2} is applied to the wiring metal layer on the silicon oxide film between the elements, a parasitic channel is produced immediately below the wiring metal, and a leakage current is produced between the elements. This phenomenon is usually called parasitic MOS effect. When a wiring metal layer to which a high voltage is applied is present in the vicinity of the region between the elements, the charge from the wiring metal layer is spread on the silicon oxide film in the vicinity of the region between the elements, and the potential of the silicon oxide film near the wiring metal layer

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becomes high. Under this condition, a parasitic channel is formed on the substrate surface between the elements, and thus a leakage current is produced. This phenomenon appears distinctly in the edge portion of the wiring metal layer and, hence, this is called "edge effect". The occurrence of the edge effect is dependent upon external atmosphere and voltage applied. Especially, the higher the humidity and the higher the voltage applied, the more frequently the edge effect occurs. This is known as one of the causes of introducing failure into the MOS semiconductor integrated circuit.

Such failure can be prevented if the threshold voltage V_{T2} is increased to a value above the power supply voltage used. For the purpose of increasing the threshold voltage V_{T2} , there is a method in which the surface impurity concentration of at least one portion of the substrate between the elements is increased. This method is described, for example, in United States Patent No. 3,456,169 issued to T. Klein. However, the edge effect is not prevented by such method. Generally, in an MOS semiconductor integrated circuit, the distance between the elements is as small as about 15 microns. In practice, it is very difficult to diffuse an impurity whose conduction type is the same as that of the substrate deeply in to the narrow region between the elements since there is a limitation on the photo-etching technique. It is therefore very probable that said deeply diffused region between the elements is overlapped with the source, drain, etc. of the element whose conduction type is different from that of the substrate. Therefore, the breakdown voltage at the P-N junction becomes low. In the operating state of an MOS type integrated circuit, a reverse bias is applied to such an overlapped P-N junction having a low breakdown voltage. Therefore the breakdown voltage at the P-N junction must be higher than the power supply voltage used. To obtain a breakdown voltage higher than the power supply voltage, it is necessary that the impurity concentration of the layer diffused into the region between the elements is not so high. While, on the other hand, the surface impurity concentration must be as high as possible in order to increase the threshold voltage V_{T2} . In short, it is very difficult to obtain a perfect isolation between the elements and a high threshold voltage V_{T2} by diffusion of a high surface impurity concentration region only in the necessary area on the substrate surface between the elements.

The present invention consists in a semiconductor integrated circuit comprising a semiconductor substrate of one conductivity type, circuit elements having regions of different conductivity type from the said one conductivity type and formed in an area of the substrate surface, a highly doped region of

said one conductivity type formed at the whole of said area except for the areas occupied by the circuit elements, the surface impurity concentration of said highly doped region being ten to one hundred times higher than the impurity concentration of the remainder of said substrate, an insulation layer deposited on selected portions of said substrate, and a wiring metal conductor deposited on a predetermined portion of the substrate and the elements, electrically connecting said elements.

In a circuit according to this invention, the highly doped region is N type when the substrate has N type conductivity, and P type when the substrate has P type conductivity. Preferably the upper limit of the surface impurity concentration of the highly doped region has a breakdown voltage, at a P-N junction formed by any overlapping with the circuit element, as high as the supply voltage.

By diffusing the impurity into the surface except for those parts occupied by the elements, the leakage current produced by the parasitic MOS effect can be eliminated. More especially, the edge effect is effectively prevented. Moreover, the reliability of the semiconductor integrated circuit is improved, and the yield rate is increased.

This invention is particularly effective in an MOS type integrated circuit. Therefore, the description of the invention will be given hereunder referring to an MOS type integrated circuit.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:—

Figure 1 is a circuit diagram showing a one bit shift register using MOS transistors;

Figure 2 is a plan model view showing an example of an integrated circuit formed into the conventional structure based on the circuit shown in Figure 1;

Figure 3 is a plan model view showing an MOS type integrated circuit embodying the present invention; and

Figure 4 is a graph illustrating the principles of the MOS semiconductor integrated circuit of the present invention.

Referring to Fig. 1 which shows a circuit diagram of a one bit shift register based on P-channel MOS transistors, the references Q_1 and Q_4 denote the main MOS transistors; Q_2 and Q_5 , the load MOS transistors operated as resistors; Q_3 and Q_6 , the gate MOS transistors operated by clock pulses ϕ_1 and ϕ_2 ; V_{DD} , the power source for operating these transistors; V_{in} an input; and V_{out} an output.

Figure 2 is a plan view showing an example of the integrated circuit formed by diffusing a P type impurity of surface concentration 10^{17} atoms/cm.³ as source and drain regions into an N-type substrate of surface concentration 2×10^{15} atoms/cm.³ from the circuit shown in Figure 1. The reference 1 denotes a power line; reference 2 is a wiring metal con-

ductor, for the clock pulse ϕ_1 ; 3, the load MOS transistor Q_2 ; 4, the transistor Q_3 serving as a gate operated by clock pulse ϕ_1 ; 5, an input line; 6, the main MOS transistor Q_1 ; 7, the load MOS transistor Q_5 ; 8, the main MOS transistor Q_4 ; 9, the transistor Q_6 serving as a gate operated by clock pulse ϕ_2 ; 10, an output line; 11, a wiring metal conductor for the clock pulse ϕ_2 ; and 12, a grounding lead.

In this integrated circuit shown in Fig. 2, input information is applied to the input V_{in} (5) and transmitted to the main MOS transistor Q_1 (6), and further transmitted to the main MOS transistor Q_4 (8) by the clock pulse ϕ_1 which is applied to the transistor Q_3 (4). The information is then transmitted to V_{out} (10) by the clock pulse ϕ_2 applied to the transistor Q_6 (9). In this case, Q_2 (3) and Q_5 (7) are operated as load MOS transistors. In such an MOS semiconductor integrated circuit, the parasitic leakage current due to the parasitic MOS effect or edge effect serves as a significant cause of deterioration in the characteristics. Specifically, the information at the point A between the transistors Q_3 (4) and Q_4 (8) is supposed to be held until the gate of the transistor Q_6 (9) is opened by the clock pulse ϕ_2 . While, if a leakage current is produced between the points A and B along the path indicated by the dotted line, namely between said point A and the point B located between the transistors Q_1 (6) and Q_4 (8), the current flows into the point B and the information at the point A is not held any more. In Figure 2, the wiring metal layer 11 for the clock pulse ϕ_2 is present in the vicinity of the area of A and B. The potential of this layer 11 is of pulse form with a large negative potential. As a result, a negative charge is spread on the oxide film from the metal layer 11, and the corresponding area on the silicon oxide film stands uniformly at a high negative potential. If this negative potential is greater than the threshold voltage V_{T2} of the same area, a parasitic leakage current is produced along the path indicated by the dotted line between the points A and B. Consequently, the information at the point A is not held any more.

Figure 4 is a graph showing characteristics obtained at various impurity concentrations, wherein the abscissa indicates N-type silicon impurity concentration, the ordinate (on the left) the threshold voltage V_{T2} of a 1.5 μ thick oxide film, and the ordinate (on the right) the breakdown voltage V_w at a junction between the diffused region and a circuit element at the surface. As indicated by the characteristic curves, the oxide film threshold voltage V_{T2} is increased in proportion as the N-type diffusion surface impurity concentration increases. Whereas, the breakdown voltage at the junction with the diffused region is decreased in proportion as the N-type diffusion impurity concentration increases and comes out in a con-

cave curve. The practically usable N-type diffusion surface impurity concentration is located around the crossing point of the two characteristic curves.

The surface density of the N-type silicon substrate used for this MOS integrated circuit is about 1×10^{15} atoms/cm². In this structure, the threshold voltage V_{T2} is about 20 volts as shown in Figure 4, when the thickness of the silicon oxide film is 1.5 μ . The breakdown voltage V_w of the P-N junction is about 150 volts. In view of the fact that the N-type impurity diffusion layer into the region between the elements is overlapped on the P+ source and drain diffusion layer, it is known that the diffusion surface impurity concentration is about 1×10^{16} atoms/cm² to 10×10^{16} atoms/cm² in the range where the breakdown voltage is above 30 volts and the threshold voltage V_{T2} is also above the 30 volts of the power supply voltage.

Figure 3 shows the region for N-type diffusion, wherein the diffusion is made on the whole surface of the region 5 μ distant from the source, drain and gate regions. In this case, it is strongly anticipated that the N-type diffusion layer is overlapped on the P+ diffusion layer of the element when the masking accuracy and pattern coincidence accuracy are taken into consideration. Therefore low impurity concentration diffusion must be made so that the breakdown voltage of the junction with the element is more than the power supply voltage.

The following means is used for making an N-type diffusion having a low surface impurity concentration such as 1×10^{16} atoms/cm² to 10×10^{16} atoms/cm² into an N-type silicon substrate whose surface impurity concentration is 1×10^{15} atoms/cm².

For example, diffusion from a glass layer will be described below. According to this method, a glass layer containing phosphorus, which is an N-type impurity, is deposited on an N-type silicon substrate having a diffusion window by a vapor-growth process. In this case, the phosphorus in the glass layer is kept at a low concentration so that a low concentration diffusion such as 10^{16} atoms/cm² is made possible. The resultant wafer is placed in a furnace in an inactive gas atmosphere wherein the diffusion is done by heating treatment. Thereafter, the glass layer is removed. Another diffusion method is such that antimony pentachloride is used for the source. The N-type layer using antimony pentachloride is hardly diffused into a silicon substrate and therefore is suited for low concentration diffusion. The highly doped region may be formed not by diffusing an impurity into the substrate but by epitaxially growing a semiconductor layer of the specific impurity concentration on the surface of the substrate.

In the MOS type integrated circuit described above, an N-type region having such

a nature that its impurity concentration is higher than that of the silicon substrate and the breakdown voltage of the P-N junction formed by overlapping the N-type region with a P+ region of the element is sufficiently higher than the power supply voltage even if such a P-N junction is formed whereby the threshold voltage V_{T2} between the elements can be increased. For this purpose, the surface impurity concentration of said N-type region is ten to one-hundred times higher than that of the substrate. As a result, the parasitic MOS effect or the edge effect which has hitherto been a significant cause of deterioration in the characteristics of MOS integrated circuits is eliminated, and the yield rate is improved. Thus, according to this invention, it is possible to manufacture highly reliable MOS semiconductor integrated circuits.

In the above description, this invention is described as applied to an MOS semiconductor integrated circuit. However, it will be apparent that the invention is applicable to other semiconductor integrated circuits. In such a case, an impurity of the same conductivity type as the substrate is deeply diffused into the surface except at the element i.e. collector region of the bipolar transistor and resistor element etc.

Moreover, it would be apparent to one skilled in this art that the spacing between the circuit element region and the highly diffused region shown in the embodiment can be eliminated.

WHAT WE CLAIM IS:—

1. A semiconductor integrated circuit comprising a semiconductor substrate of one con-

ductivity type, circuit elements having regions of different conductivity type from said one conductivity type and formed in an area of the substrate surface, a highly doped region of said one conductivity type formed at the whole of said area except for the areas occupied by the circuit elements, the surface impurity concentration of said highly doped region being ten to one hundred times higher than the impurity concentration of the remainder of said substrate, an insulation layer deposited on selected portions of said substrate, and a wiring metal conductor deposited on a predetermined portion of the substrate and the elements, electrically connecting said elements.

2. A semiconductor integrated circuit as claimed in claim 1, wherein the said one conductivity type is N-type.

3. A semiconductor integrated circuit as claimed in claim 1 or 2, wherein said circuit element comprises an MOS transistor as the active element.

4. A semiconductor integrated circuit as claimed in claim 1 or 2, wherein said surface impurity concentration of said highly doped region is 1×10^{16} atoms/cm³ to 10×10^{16} atoms/cm³.

5. A semiconductor integrated circuit constructed, arranged and adapted to operate substantially as hereinbefore described with reference to, and as illustrated in, Figures 3 and 4 of the accompanying drawings.

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