internally stored in the nonvolatile memory device while the nonvolatile memory device is manufactured. In other example embodiments, the dividing scheme in step S120 may be determined based on the command CMD and the address ADDR received from the memory controller. The method for dividing and selecting subpages may be performed according to one or more known techniques.

[0084] Each of the first through M-th subpages SP1, SP2, ..., SPM may include two or more memory cells that are not physically adjacent to one another (e.g., that are physically spaced apart from one another).

[0085] For example, the program target page TP may be connected to first through N-th bitlines BL1, BL2, ..., BLM, BL(M+1), BL(M+2), ..., BL2M, ..., BL(N-M+1), BL(N-M+2), ..., BLN, where N is a natural number greater than or equal to two. The program target page TP may include first through N-th memory cells MC1, MC2, ..., MCM, MC(M+1), MC(M+2), ..., MC2M, ..., MC(N-M+1), MC(N-M+2), ..., MCN that are connected to the first wordline WL1 and are disposed along the first direction D1. Each of the first through N-th memory cells MC1, MC2, ..., MCM, MC(M+1), MC(M+2), ..., MC2M, ..., MC(N-M+1), MC(N-M+2), ..., MCN may be connected to a respective one of the first through N-th bitlines BL1, BL2, ..., BLM, BL(M+1), BL(M+2), ..., BL2M, ..., BL(N-M+1), BL(N-M+2), ..., BLN.

[0086] The memory cells MC1, MC(M+1), ..., MC(N-M+1) included in the first subpage SP1 may be connected to K*(M+1)-th bitlines BL1, BL(M+1), ..., BL(N-M+1) among the first through N-th bitlines. Similarly, the memory cells MC2, MC(M+2), ..., MC(N-M+2) included in the second subpage SP2 may be connected to K*(M+2)-th bitlines BL2, BL(M+2), ..., BL(N-M+2) among the first through N-th bitlines, and the memory cells MCM, MC2M, ..., MCN included in the M-th subpage SPM may be

and are disposed along the first direction D1, and (N+1)-th through 2N-th memory cells MC21, MC22, ..., MC2P, MC2(P+1), MC2(P+2), ..., MC22P, ..., MC2(N-P+1), MC2(N-P+2), ..., MC2N that are connected to the second wordline WL2 and are disposed along the first direction D1. Each of the first through N-th memory cells MC11, MC12, ..., MC1P, MC1(P+1), MC1(P+2), ..., MC12P, ..., MC1(N-P+1), MC1(N-P+2), ..., MC1N may be connected to a respective one of the first through N-th bitlines BL1, BL2, ..., BLP, BL(P+1), BL(P+2), ..., BL2P, ..., BL(N-P+1), BL(N-P+2), ..., BLN. Each of the (N+1)-th through 2N-th memory cells MC21, MC22, ..., MC2P, MC2(P+1), MC2(P+2), ..., MC22P, ..., MC2(N-P+1), MC2(N-P+2), ..., MC2N may be connected to a respective one of the first through N-th bitlines BL1, BL2, ..., BLP, BL(P+1), BL(P+2), ..., BL2P, ..., BL(N-P+1), BL(N-P+2), ..., BLN.

[00112] The memory cells MC11, MC1(P+1), ..., MC1(N-P+1), MC21, MC2(P+1), ..., MC2(N-P+1) included in the first subblock SB1 may be connected to L*(P+1)-th bitlines BL1, BL(P+1), ..., BL(N-P+1) among the first through N-th bitlines. Similarly, the memory cells MC12, MC1(P+2), ..., MC1(N-P+2), MC22, MC2(P+2), ..., MC2(N-P+2) included in the second subblock SB2 may be connected to L*(P+2)-th bitlines BL2, BL(P+2), ..., BL(N-P+2) among the first through N-th bitlines, and the memory cells MC1P, MC12P, ..., MC1N, MC2P, MC22P, ..., MC2N included in the P-th subblock SBP may be connected to L*(P+P)-th bitlines BLP, BL2P, ..., BLN among the first through N-th bitlines. For example, when L is equal to 6, the memory cells MC11, MC1(P+1), ..., MC1(N-P+1), MC21, MC2(P+1), ..., MC2(N-P+1) included in the first subblock SB1 may be connected to 6*(P+1)-th bitlines BL1, BL(P+1), ..., BL(N-P+1), the memory cells MC12, MC1(P+2), ..., MC1(N-P+2), MC22, MC2(P+2), ...,

What is claimed is:

1. A method of writing data in a nonvolatile memory device including a plurality of cell strings, each of the plurality of cell strings including a plurality of memory cells disposed in a vertical direction, the method comprising:

dividing a program target page into a plurality of subpages, the program target page being connected to one of a plurality of wordlines, each of the plurality of subpages including memory cells that are physically spaced apart from one another;

sequentially performing a program operation on the plurality of subpages; and

performing a program verification operation on the program target page including performing the program verification operation on the plurality of subpages at the same time.

2. The method of claim 1, wherein the sequentially performing the program operation includes:

setting a program voltage;

selecting one subpage of the plurality of subpages; and

applying the program voltage to bitlines connected to the selected one subpage.

3. The method of claim 2, wherein the selecting one of the plurality of subpages and the applying the program voltage to the bitlines connected to the selected one subpage are repeated until all of the plurality of subpages are programmed.

4. The method of claim 2 or claim 3, further comprising:

determining a result of the program operation;

when it is determined, based on the result of the program verification operation, that at least a part of the program target page corresponds to a failed program state, resetting the program voltage to a reset program voltage; and

sequentially re-performing the program operation on the plurality of subpages based on the reset program voltage.

5. The method of any one of claims 1 to 4, wherein each of the plurality of cell strings includes:

a string selection transistor connected to a bitline and a string selection line;

the plurality of memory cells disposed in the vertical direction between the string selection transistor and a common source line, the plurality of memory cells being connected to the plurality of wordlines, respectively; and

a channel structure penetrating the string selection line and the plurality of wordlines that are stacked in the vertical direction, the channel structure including a variable resistive film, a channel layer surrounding the variable resistive film, and an insulation film surrounding the channel layer.

6. The method of any one of claims 1 to 5, wherein:

the program target page is connected to first through N-th bitlines where N is a natural number greater than or equal to two,

the plurality of subpages include first through M-th subpages where M is a natural number greater than or equal to two, and

memory cells included in the first subpage are connected to K*(M+1)-th bitlines among the first through N-th bitlines, respectively.

7. The method of any one of claims 1 to 6, wherein a number of the plurality of subpages is determined based on a peak limit current of the nonvolatile memory device.

8. A method of erasing data in a nonvolatile memory device including a plurality of cell strings, each of the plurality of cell strings including a plurality of memory cells disposed in a vertical direction, the method comprising:

dividing an erase target block into a plurality of subblocks, the erase target block being connected to at least one of a plurality of wordlines, each of the plurality of subblocks including memory cells that are physically spaced apart from one another;

sequentially performing an erase operation on the plurality of subblocks; and

performing an erase verification operation on the erase target block including the plurality of subblocks at the same time,

wherein each of the plurality of cell strings includes:

a string selection transistor connected to a bitline and a string selection line;

the plurality of memory cells disposed in the vertical direction between the string selection transistor and a common source line, the plurality of memory cells being connected to the plurality of wordlines, respectively; and

a channel structure penetrating the string selection line and the plurality of wordlines that are stacked in the vertical direction, the channel structure including a variable resistive film, a channel layer surrounding the variable resistive film, and an insulation film surrounding the channel layer.

9. The method of claim 8, wherein the sequentially performing the erase operation includes:

setting an erase voltage;

selecting one subblock of the plurality of subblocks; and

applying the erase voltage to bitlines connected to the selected one subblock.

10. The method of claim 9, wherein the selecting one of the plurality of subblocks and the applying the erase voltage to the bitlines connected to the selected one subblock are repeated until all of the plurality of subblocks are erased.

11. The method of claim 9 or claim 10, further comprising:

determining a result of the erase verification operation;

when it is determined, based on the result of the erase verification operation, that at least a part of the erase target block corresponds to a failed erase state, resetting the erase voltage to a reset erase voltage; and

sequentially re-performing the erase operation on the plurality of subblocks based on the reset erase voltage.

12. The method of any one of claims 8 to 11, wherein:

the erase target block is connected to first through N-th bitlines where N is a natural number greater than or equal to two,

the plurality of subblocks include first through P-th subblocks where P is a natural number greater than or equal to two, and

memory cells included in the first subblock are connected to L*(P+1)-th bitlines among the first through N-th bitlines, respectively.

13. The method of any one of claims 8 to 12, wherein a number of the

plurality of subblocks is determined based on a peak limit current of the nonvolatile memory device.

14. A nonvolatile memory device comprising:

a memory cell array including a plurality of cell strings formed in a vertical direction,

wherein each of the plurality of cell strings includes:

a string selection transistor connected to a bitline and a string selection line;

a plurality of memory cells disposed in the vertical direction between the string selection transistor and a common source line, the plurality of memory cells being connected to a plurality of wordlines, respectively; and

a channel structure penetrating the string selection line and the plurality of wordlines that are stacked in the vertical direction, the channel structure including a variable resistive film, a channel layer surrounding the variable resistive film, and an insulation film surrounding the channel layer, further comprising:

a control circuit configured to perform a data writing operation by dividing a program target page into a plurality of subpages, sequentially performing a program operation on the plurality of subpages, and performing a program verification operation on the program target page including the plurality of subpages at the same time, and

wherein the control circuit is configured to further perform a data erasing operation by dividing an erase target block into a plurality of subblocks, sequentially performing an erase operation on the plurality of subblocks, and performing an erase verification operation on the erase target block including the plurality of subblocks at the same time.

15. The nonvolatile memory device of claim 14,

wherein the program target page is connected to one of the plurality of wordlines, and each of the plurality of subpages includes memory cells that are physically spaced apart from one another.

16. The nonvolatile memory device of claim 14, wherein:

the erase target block is connected to at least one of the plurality of wordlines, and

each of the plurality of subblocks includes memory cells that are physically spaced apart from one another.

17. The nonvolatile memory device of claim 16, wherein a number of the plurality of subpages is equal to a number of the plurality of subblocks.

18. The nonvolatile memory device of claim 16, wherein a number of the plurality of subpages is different from a number of the plurality of subblocks.

19. The nonvolatile memory device of any one of claims 14 to 18, wherein a number of the plurality of subpages and a number of the plurality of subblocks are determined based on a peak limit current of the nonvolatile memory device.