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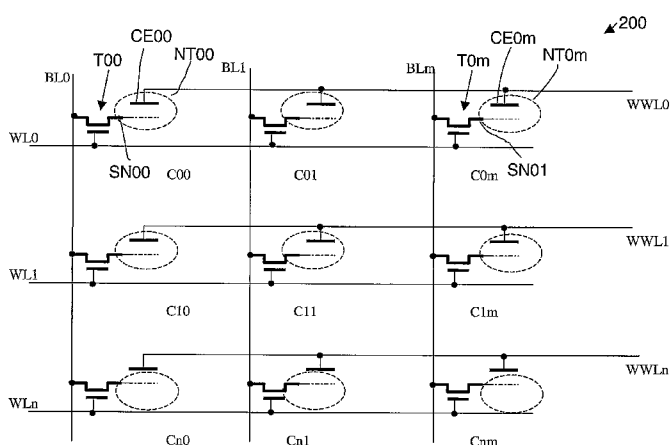
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[Continued on next page]

(54) Title: MEMORY ARRAYS USING NANOTUBE ARTICLES WITH REPROGRAMMABLE RESISTANCE



(57) Abstract: A memory array includes a plurality of memory cells, each of which receives a bit line, a first word line, and a second word line. Each memory cell includes a cell selection circuit, which allows the memory cell to be selected. Each memory cell also includes a two-terminal switching device, which includes first and second conductive terminals in electrical communication with a nanotube article. The memory array also includes a memory operation circuit, which is operably coupled to the bit line, the first word line, and the second word line of each cell. The circuit can select the cell by activating an appropriate line, and can apply appropriate electrical stimuli to an appropriate line to reprogrammably change the relative resistance of the nanotube article between the first and second terminals. The relative resistance corresponds to an informational state of the memory cell.



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