(ref only)

SIMPLIFIED HIGH Q INDUCTOR SUBSTRATE

Technical Field Of The Invention

The present invention is directed, in general, to semiconductor devices and, more specifically, to a semiconductor device having a simplified high Q inductor substrate and a method for manufacturing that substrate.

Background Of The Invention

Integrated circuits are critical to the success of many technology areas, and especially critical to the continued growth of the telecommunications industry. Semiconductor devices in the form of integrated circuits are the cornerstone of many telecommunications systems involving a broad spectrum of different circuits, many of which require high frequency capabilities. High frequency telecommunications circuits typically require the use of inductors to either tune a circuit to a particular desired frequency, to perform critical circuit functions such as maintaining a critical current flow, or to filter and eliminate undesired electrical noise from desired signals.

If a collection of inductors is needed to allow a particular integrated circuit device to perform correctly, the use of discrete inductors that are separate from the integrated circuit device may give rise to implementation problems due to the need for many interconnections. This situation has driven the industry to move in the direction of integrating as many of these needed inductors as possible into the semiconductor device itself. However, the integration of an inductor into a semiconductor device creates other problems due to the inductor's magnetic nature.

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The magnetic field associated with a conductive coil forming an inductor is a well known donut or torus shaped structure, usually having an elliptical cross-section. This magnetic field alternates with the frequency applied to the inductor and may cause interfering effects within the semiconductor device itself. The generation of spurious currents due to this magnetic field may produce several undesirable effects. One of these is to reduce the effectiveness of the conductive coil's ability to perform as an inductor due to energy losses.

It is well known that the Q of an inductive circuit is a figure of merit that relates the energy stored to the energy dissipated or lost. High Q inductor circuits (a Q of 10 or greater) conserve sufficient energy to allow an appropriate inductive response. Alternately, low Q inductor circuits (a Q of three or less) lose a sufficient portion of the energy applied, often through the generation of eddy currents in the semiconductor device, causing them to perform poorly as inductive elements. Eddy currents are minimized in a semiconductor layer that corresponds to lower dopant concentrations thereby providing a layer having comparatively higher resistivity.

An example of an integrated circuit, that will not support a high Q inductor, has a highly conductive substrate and a highly resistive epitaxial (EPI) layer grown on the substrate. This integrated circuit is typical of a fundamental building block used in many current communications microchips. This substrate may have a positive dopant, such as boron, with a P+ dopant concentration that is typically greater than $10^{18}cm^{-3}$ making the substrate highly conductive electrically. The EPI layer also has a positive dopant but with a reduced or P- dopant concentration of about $10^{15}cm^{-3}$ making the EPI layer highly

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resistive.

The highly conductive substrate is used to prevent a functionally destructive phenomenon known as latch-up. Latch-up occurs when a voltage is applied to a semiconductor device in a direction opposite to the normal operating polarity. Latch-up is reduced in a semiconductor layer corresponding to higher dopant concentrations, which thereby provide a layer having comparatively higher conductivity (lower resistivity). A highly resistive substrate, however, would exacerbate the latch-up phenomenon.

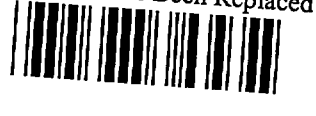
High frequency communications microchips require that inductors be integrated into a microchip to achieve a required circuit performance and size, as stated earlier. If an integrated inductor were formed over the EPI layer under discussion, the inductor would induce eddy currents into the highly conductive substrate thereby incurring a large energy loss. To be energy efficient and therefore low loss, the integrated inductor would have to be formed over a highly resistive substrate. A semiconductor device, therefore, must incorporate trade-offs within its design to eliminate the generation of spurious currents and successfully accommodate integrated inductors. However, achievement of the required trade-offs currently requires many additional process steps in the construction of the semiconductor device thereby adding substantial manufacturing time and therefore cost to the semiconductor wafer.

Accordingly, what is needed in the art is a simplified and more cost-effective way to accommodate integrated inductors into semiconductor wafers.

Summary Of The Invention

To address the above-discussed deficiencies of the prior

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art, the present invention provides for a method of manufacturing a simplified high Q inductor substrate and a semiconductor device having that substrate. In one embodiment, the method for manufacturing the simplified high Q inductor substrate comprises forming a base substrate over a semiconductor wafer, wherein the base substrate has a given dopant concentration and then forming an epitaxial (EPI) layer over the base substrate that uniquely has differently doped regions. The EPI layer includes epitaxially forming a first doped region in the EPI layer over the base substrate and then epitaxially forming a second doped region in the EPI layer over the first doped region. The first doped region preferably has a dopant concentration greater than the given dopant concentration of the base substrate, and the second doped region has a dopant concentration less than the first doped region.

The present invention therefore introduces the broad concept of manufacturing a simplified high Q inductor substrate through the forming of the EPI layer containing at least two dopant concentrations. These differently doped regions provide a balance in the semiconductor device between maximizing the Q for an integrated inductor formed in the device and maintaining a required latch-up resistance for the device.

Forming the base substrate, in one embodiment of the present invention, includes doping the base substrate with a p-type dopant to a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3} wherein a dopant concentration of about $10^{15}cm^{-3}$ is typical.

In an embodiment to be illustrated and described, epitaxially forming an EPI layer includes epitaxially forming an EPI layer having first and second doped regions to a

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thickness ranging from about 3μm to about 7μm.

Epitaxially forming a first doped region in the EPI layer, in an alternate embodiment, includes doping the first doped region with a p-type dopant to a dopant concentration equal to or greater than about 10^{17} cm^{-3}. In a further aspect of this embodiment, a dopant concentration of about $10^{18}cm^{-3}$ is used, and the first doped region has a thickness ranging from about 0.5μm to about 2μm.

In yet another embodiment of the present invention, epitaxially forming a second doped region over the first doped region includes doping the second doped region with a p-type dopant to a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3} wherein a dopant concentration of about $10^{15}cm^{-3}$ is typical. The second doped region has a thickness ranging from about 3μm to about 5μm.

In another aspect, the present invention provides a semiconductor wafer that comprises a base substrate that is formed over a semiconductor wafer and that has a given dopant concentration. An epitaxial (EPI) layer is formed over the base substrate, which includes at least first and second doped regions. The first doped region is located over the base substrate and has a dopant concentration greater than the given dopant concentration of the base substrate. The second doped region is located over the first doped region and has a dopant concentration less than the first doped region. While two doped regions have been specifically set forth, those who are skilled in the art will appreciate that other embodiments of the present invention could provide for more than two differently doped regions within the EPI layer.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that

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those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

Brief Description Of The Drawings

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a diagram showing a prior art construction of an integrated circuit wafer that will support a high Q inductor;

FIGURE 2 illustrates a diagram showing an embodiment of an integrated circuit wafer that will support a high Q inductor constructed according to the principles of the present invention;

FIGURE 3 illustrates a diagram showing an embodiment of an integrated circuit wafer constructed according to the principles of the present invention having a high Q thick metal inductor; and

FIGURE 4 illustrates a flow diagram of a method that may be used to construct the integrated circuit wafer of FIGURE 2.

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Detailed Description

Referring initially to FIGURE 1, illustrated is a diagram showing a prior art construction of an integrated circuit wafer 100 that will support a high Q inductor. The integrated circuit wafer 100 includes a substrate 105, an induced layer 110 and an EPI layer 115. The substrate 105 has a positive dopant with a P- dopant concentration that is typically about $10^{15}cm^{-3}$ making the substrate 105 highly resistive electrically. The induced layer 110 is a thin, highly conductive layer that is constructed by diffusing or implanting a P+ dopant into the substrate 105. A P+ dopant concentration of $10^{18}cm^{-3}$is typical. The EPI layer 115 is then grown on the induced layer 110 and has a P- dopant concentration of about $10^{15}cm^{-3}$.

A typical diffusion process which may be used to form the induced layer 110 includes the following steps: 1) Brush scrub cleaning, 2) 100:1 HF cleaning, 3) Deposit solid diffusion source,

4) Deposit cap layer, 5) Drive in dopants,,6) Remove solid diffusion source, and 7) Clean wafer for EPI growth.

A typical implantation process which may also be used to form the induced layer 110 includes the following steps: 1) Brush scrub cleaning, 2) 100:1 HF cleaning, 3) Implant dopants, 4) Drive in dopants, and 5) Clean wafer for EPI growth.

The integrated circuit wafer 100 provides a structure that will both support a high Q integrated inductor and prevent a latch-up condition. The substrate 105 is highly resistive and therefore does not support eddy currents that would lead to energy loss and low Q inductor circuit situations. Additionally, the induced layer 110, being

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highly conductive, prevents latch-up from occurring. Since the induced layer 110 is thin, it will also not support sufficient eddy current activity to cause low Q inductor current situations, as well. Unfortunately, however, the process steps needed to construct the induced layer are many and therefore both time consuming and costly.

Turning now to FIGURE 2, illustrated is a diagram showing an embodiment of an integrated circuit wafer 200 that will support a high Q inductor constructed according to the principles of the present invention. The integrated circuit wafer 200 includes a base substrate 205 and an EPI layer 210 having first and second doped regions 210A, 210B, which are preferably formed by an epitaxial process.

The present invention includes the semiconductor wafer 200 that comprises the base substrate 205 having a given dopant concentration that is formed over the semiconductor wafer 200. The EPI layer 210 is preferably expitaxially formed over the base substrate 205, which includes first and second doped regions 210A, 210B. The first doped region 210A is located over the base substrate 205 and has a dopant concentration greater than the given dopant concentration of the base substrate 205. The second doped region 210B is located over the first doped region 210A and has a dopant concentration less than the first doped region 210A.

In one embodiment, the first doped region 210A may be formed by using 120 ppm boron source directly fed into one dopant controller and which is then mixed with trichlorosilane (TCS)and flowed at a rate of about 5 liters/minute. The EPI layer 210 is grown at a temperature of about 1150°C. The second doped region 210B may be formed by removing the 120 ppm boron source while maintaining the TCS flow at 5 liters/minute at about 1150°C.

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The present invention therefore introduces the broad concept of manufacturing a simplified high Q inductor substrate through the forming of the EPI layer 210 containing at least two dopant concentrations. These differently doped regions 210A, 210B provide a balance in the semiconductor device between maximizing the Q for an integrated inductor formed in the device and maintaining a required latch-up resistance for the device. While the two doped regions 210A, 210B have been specifically set forth in this embodiment, those who are skilled in the art will appreciate that other embodiments of the present invention could provide for more than two differently doped regions within the EPI layer 210.

Forming the base substrate 205 in this embodiment of the present invention includes doping the base substrate 205 with a p-type dopant to a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3} wherein a dopant concentration of about $10^{15}cm^{-3}$ is preferred. Then, the EPI layer 210 is epitaxially formed having first and second doped regions 210A, 210B to a thickness ranging from about 3μm to about 7μm. The first doped region 210A has a thickness ranging from about 0.5μm to about 2μm, and the second doped region 210B has a thickness ranging from about 3μm to about 5μm.

Epitaxially forming the first doped region 210A in the EPI layer 210 includes doping the first doped region 210A with a p-type dopant to a dopant concentration equal to or greater than about 10^{17} cm^{-3} wherein a dopant concentration of about $10^{18}cm^{-3}$ is preferably achieved. Then epitaxially forming the second doped region 210B over the first doped region 210A includes doping the second doped region 210B with a p-type dopant to a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3} wherein a dopant concentration of about $10^{15}cm^{-3}$ is preferred.

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Therefore, the base substrate 205 is highly resistive electrically, the first doped region 210A of the EPI layer 210 is highly conductive and the second doped region 210B of the EPI layer 210 is highly resistive. The integrated circuit wafer 200 affords a structure that will both support a high Q integrated inductor and prevent a latch-up condition as seen in the prior art example of FIGURE 1. However, epitaxially forming the EPI layer 210 using two differently doped regions allows the structure to be constructed using basically only one additional process step wherein only the dopant concentration is reduced to form the second doped region 210B. The time at which the dopant concentration is reduced, and the amount of the dopant concentration reduction determine the thickness of the first doped region 210A and the resistivity of the second doped region 210B, respectively. This process may be accomplished much more quickly, easily and cost effectively than the diffusion or the implantation processes used in the example of FIGURE 1.

Turning now to FIGURE 3, illustrated is a diagram showing an embodiment of an integrated circuit wafer 300 constructed according to the principles of the present invention having a high Q thick metal inductor. The integrated circuit wafer 300 includes a base substrate 305, an EPI layer 310 having first and second doped regions 310A, 310B, first and second field effect transistors (FETs) 315, 320 having sources, drains and interposed gates, an inter-level dielectric region 325 having metal interconnections 330 and a thick metal inductor 335.

The integrated circuit wafer 300 employs the first doped region 310A of the EPI layer 310, which is highly conductive and the second doped region 310B of the EPI layer 310, which is highly resistive to afford a structure that will both support a high Q integrated inductor and prevent a latch-up

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condition as seen in FIGURE 2. The thick metal inductor 335 is located well "up-level" from the first and second FETs 315, 320 and is connected to other appropriate circuit components through the metal interconnections 330 in the inter-level dielectric region 325.

Turning now to FIGURE 4, illustrated is a flow diagram of a method 400 that may be used to construct the integrated circuit wafer 200 of FIGURE 2. The method 400 of manufacturing a simplified high Q inductor substrate starts in a step 405 and continues in a step 410 with the forming of a base substrate over a semiconductor wafer. The base substrate formed in the step 410 has a given dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3} wherein a dopant concentration of about $10^{15}cm^{-3}$ is typical. Then, an EPI layer is formed over the base substrate to a thickness ranging from about 3μm to about 7μm in steps 415A and 415B, that uniquely has differently doped regions.

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The EPI layer includes epitaxially forming a first doped region in the EPI layer in the step 415A over the base substrate and then epitaxially forming a second doped region in the EPI layer over the first doped region in the step 415B. The first doped region formed in the step 415A has a dopant concentration greater than the given dopant concentration of the base substrate formed in the step 410. The first doped region has a dopant concentration equal to or greater than about 10^{17} cm^{-3}, where a dopant concentration of about $10^{18}cm^{-3}$ is typical. The first doped region has a thickness ranging from about 0.5μm to about 2μm.

The second doped region in the EPI layer formed in the step 415B has a dopant concentration less than the first doped region.

The second doped region has a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3} wherein a dopant concentration of about $10^{15}cm^{-3}$ is typical. The second doped region has a thickness ranging from about 3μm to about 5μm.

The thickness of the first doped region of the EPI layer formed in the steps 415A and 415B is determined by a first length of time that the first dopant concentration is applied. Then, the dopant concentration is reduced and the growth of the EPI layer is continued for a second length of time to determine the thickness of the second doped region. The method 400 ends in a step 420 when the second length of time is complete. The method 400 of using a single EPI layer with two separate doped regions greatly simplifies the manufacture of a structure, that will support a high Q integrated inductor while inhibiting latch-up, as compared to the current use of a diffusion or implantation process.

Although the present invention has been described in

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detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

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Claims:

1. A method for manufacturing a semiconductor substrate, comprising:

forming a base substrate over a semiconductor wafer, the base substrate having a given dopant concentration; and

forming an epitaxial (EPI) layer over the base substrate, including:

epitaxially forming a first doped region in the EPI layer over the base substrate, the first doped region having a dopant concentration greater than the given dopant concentration of the base substrate; and

epitaxially forming a second doped region in the EPI layer over the first doped region, the second doped region having a dopant concentration less than the first doped region.

2. The method as recited in Claim 1 wherein completing formation of the semiconductor device includes forming an inductor in the semiconductor device.

3. The method as recited in Claim 1 wherein forming a base substrate includes doping the base substrate with a p-type dopant.

4. The method as recited in Claim 1 wherein forming a base substrate include doping the base substrate to a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3}.

5. The method as recited in Claim 4 wherein doping the base substrate includes doping the base substrate to a dopant concentration of about $10^{15}cm^{-3}$ with a p-type dopant.

6. The method as recited in Claim 1 wherein

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epitaxially forming a first doped region in the EPI layer includes doping the first doped region with a p-type dopant.

7. The method as recited in Claim 1 wherein epitaxially forming a first doped region in the EPI layer includes doping the first doped region to a dopant concentration equal to or greater than about 10^{17} cm^{-3}.

8. The method as recited in Claim 7 wherein doping the first doped region includes doping the first doped region to a dopant concentration of about $10^{18}cm^{-3}$ with a p-type dopant.

9. The method as recited in Claim 8 wherein doping the first doped region includes using a 120 ppm boron source directly fed into one dopant controller and mixed with trichlorosilane flowed at 5 liters/minute and at a temperature of 1150°C.

10. The method as recited in Claim 1 wherein epitaxially forming a second doped region over the first doped region includes doping the second doped region with a p-type dopant.

11. The method as recited in Claim 1 wherein epitaxially forming a second doped region over the first doped region includes doping the second doped region to a dopant concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3}.

12. The method as recited in Claim 11 wherein doping the second doped region includes discontinuing a flow of 120 ppm boron while maintaining a trichlorosilane flow at 5 liters/minute at 1150°C.

13. The method as recited in Claim 11 wherein doping the second doped region includes doping the second doped

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region to a dopant concentration of about $10^{15}cm^{-3}$ with a p-type dopant.

14. The method as recited in Claim 1 wherein epitaxially forming an EPI layer includes epitaxially forming an EPI layer to a thickness ranging from about 3μm to about 7μm.

15. The method as recited in Claim 1 wherein epitaxially forming a first doped region in the EPI layer includes epitaxially forming a first doped region to a thickness ranging from about 0.5μm to about 2μm.

16. The method as recited in Claim 1 wherein epitaxially forming a second doped region over the first doped region includes forming a second doped region to a thickness ranging from about 3μm to about 5μm.

17. The method as recited in Claim 1 wherein forming a base substrate includes forming a p-type substrate to a dopant concentration of about $10^{15}cm^{-3}$, epitaxially forming a first doped region over the base substrate includes epitaxially forming a p-type first region to a dopant concentration of about $10^{18}cm^{-3}$, and forming a second doped region over the first doped region includes epitaxially forming a p-type first region to a dopant concentration of about $10^{15}cm^{-3}$.

18. A semiconductor wafer, comprising:

a base substrate over a semiconductor wafer, the base substrate having a given dopant concentration;

an epitaxial (EPI) layer over the base substrate, including:

an epitaxially formed first doped region located

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over the base substrate, the first doped region having a dopant concentration greater than the given dopant concentration of the base substrate; and

an epitaxially formed second doped region located over the first doped region, the second doped region having a dopant concentration less than the first doped region.

19. The semiconductor wafer as recited in Claim 18 further comprising an integrated circuit having an inductor incorporated therein.

20. The semiconductor wafer as recited in Claim 18 wherein the base substrate has a p-type dopant.

21. The semiconductor wafer as recited in Claim 18 wherein the base substrate is doped to a concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3}.

22. The semiconductor wafer as recited in Claim 21 wherein the base substrate is doped to a concentration of about $10^{15}cm^{-3}$ with a p-type dopant.

23. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed first doped region is doped with a p-type dopant.

24. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed first doped region is doped to a concentration equal to or greater than about 10^{17} cm^{-3}.

25. The semiconductor wafer as recited in Claim 23 wherein the first doped region is doped to a concentration of about $10^{18}cm^{-3}$ with a p-type dopant.

26. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed second doped region is doped

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with a p-type dopant.

27. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed second doped region is doped to a concentration ranging from about 10^{14} cm^{-3} to about 10^{16} cm^{-3}.

28. The semiconductor wafer as recited in Claim 27 wherein the second doped region is doped to a concentration of about $10^{15}cm^{-3}$ with a p-type dopant.

29. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed EPI layer has a thickness ranging from about 3μm to about 7μm.

30. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed first doped region has a thickness ranging from about 0.5μm to about 2μm.

31. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed second doped region has a thickness ranging from about 3μm to about 5μm.

32. The semiconductor wafer as recited in Claim 18 wherein the epitaxially formed first doped region provides a Q equal to or greater than about 10.

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