Description

This invention relates to a method for manufacturing a semiconductor device having a non-volatile memory cell region and a logic region including MOS transistors.

A conventional method for manufacturing a semiconductor device having a non-volatile memory cell region and a logic region including MOS transistors will now be explained.

First, to form a first insulating film and a first polysilicon film in the memory cell region, a gate oxide film is formed over a semiconductor wafer or substrate by thermal oxidization, and then a polysilicon film is deposited on the oxide film.

Subsequently, only those portions of the gate oxide film and polysilicon film which are located in the logic region are removed from the wafer. Then, another insulating film is formed all over the wafer by thermal oxidization. A resist film is directly coated on the insulating film. Thereafter, an opening is formed in a desired portion of the resist film, through which impurity ions are implanted into the substrate of the logic region, thereby forming the channel region of a MOS transistor. The resist film is then removed, and a second polysilicon film is deposited over the memory cell region and logic region.

Thereafter, predetermined portions of the memory cell region and logic region are subjected to self-align dry etching, thus forming a memory cell and MOS transistors constituting a logic circuit, respectively.

However, this method has the following disadvantages:

1. Due to the process of implanting impurity ions into the logic region through the gate oxide film, the gate film is charged with part of the impurity ions, and traps are formed therein. Thus, the gate threshold voltage Vth of the MOSFET is unstable.
2. To implant impurity ions into the channel region of the logic region, the resist film is directly formed on a poly-poly insulating film (an insulating film formed between a floating gate and a control gate) in the non-volatile memory cell region, and on the gate oxide film in the logic region. This causes part of the resist film to remain as a pollutant in the poly-poly insulating film and in the gate oxide film.

It is the object of the invention to provide a method for manufacturing a superior semiconductor device having a non-volatile memory cell of high quality, and MOS transistors of high reliability constituting a logic circuit.

To attain the object, the method of manufacturing a semiconductor device having a non-volatile memory cell region and a logic region including MOS transistors, comprises the steps of: forming in succession a first insulating film and a first electrode layer on a semiconductor substrate; removing the first insulating film and first electrode layer which are located in the logic region, without removing the first insulating film and first electrode layer which are located in the non-volatile memory cell region; forming a deposited sacrificial film for insulation over the entire surface in the memory cell region and logic region; and coating a resist film on the sacrificial film; forming an opening in a desired portion of the resist film, and implanting impurity ions into the semiconductor substrate located in the logic region through the opening; removing the resist film and sacrificial film, and forming in succession a second insulating film and a second electrode layer in the non-volatile memory cell region and logic region.

According to the method, the resist film is coated after the sacrificial film is formed over the entire surface of the non-volatile memory cell region and logic region. Subsequently, impurity ions are implanted only into a desired channel region of the logic region, then the resist film and sacrificial film are removed, and a gate oxide film is formed.

This being so, the traps or the like will not formed in the gate insulating film of the MOS transistors, and also a fluctuation in the gate threshold voltage Vth of the transistor will not occur. Further, part of the resist film, acting as a pollutant, does not remain in the poly-poly insulating film and gate oxide film, which are important elements for the operation of the non-volatile memory cell and MOS transistors. As a result, these films are enhanced in reliability.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A through 1F show a flowchart, useful in explaining a manufacturing method of a semiconductor device according to an embodiment of the present invention.

The method of this invention will be explained in detail with reference to the accompanying drawings showing an embodiment thereof.

Figs. 1A - 1F show a semiconductor device having an EPROM and MOS transistors. In the figures, broken line 21 is a boundary which defines a non-volatile memory cell region 10 and a logic region 11.

Referring first to Fig. 1A, a first gate oxide film 23 having a thickness of 250 A is formed on a P^- type silicon semiconductor substrate 22 by thermal oxidization. Then, a first polysilicon film 24 is formed on the first gate oxide film 23 by CVD (Chemical Vapor Deposition). Subsequently, those portions of the oxide film 23 and polysilicon film 24 which located in the logic region 11 are removed by CDE (Chemical Dry Etching) or RIE (Reactive Ion Etching).

Thereafter, as is shown in Fig. 1B, an oxide film 25 having a thickness of 250 Å is deposited by CVD, over the first polysilicon film 24 in the memory cell region 10 and the P^- silicon substrate 22 in the logic re-

gion, thereby protecting them from contamination caused by a resist film to be formed later, or ions to be implanted later. The film 25 is a deposited sacrificial oxide film for insulation.

Referring to Fig. 1C, a resist film 26 is formed on the oxide film 25, and then an opening is formed in the resist film 26 at a desired location in the logic region 11, through the opening impurity ions are implanted, thereby forming a channel region 27. After removing the resist film 26, the oxide film 25 is also removed by etching in NH_4F solution, which prevents the material of the resist film from remaining in the semiconductor integrated circuit. Heat process can be applied to the wafer in non-oxidizing atmosphere to electrically activate the impurity ions after removing the resist film 26. If the resist material remains in the circuit, the material is scattered therein during heating etc. performed later, which may deteriorate the quality of the device.

Subsequently, as is shown in Fig. 1D, a second gate oxide film 28 is formed by thermal oxidization at 900 - 1000°C in the atmosphere of oxygen, and a second polysilicon film 29 having a thickness of 0.4 µm is deposited on the film 28. Then, as is shown in Fig. 1E, that portion of the second polysilicon film 29 located in the non-volatile memory cell region 10 and the remaining first polysilicon film 24 are subjected to self align dry etching, thereby forming a non-volatile memory cell comprising a control gate 29a and a floating gate 24a. On the other hand, that portion of the second polysilicon film 29 located in the logic region 11 is subjected to dry etching, thereby forming a gate electrode 29b.

Referring to Fig. 1F, impurity ions are implanted into the substrate, forming N^+ type drain regions 33 and N^+ type source regions 34 for the MOS transistors in the logic region 11, and for the EPROM in the non-volatile memory cell region 10, respectively. Thereafter, an oxide film 35 and a passivation film 36 are provided on the chip. Contact holes are formed in the films 35 and 36, through which A1 wiring 37 is formed.

As is described above, the deposited sacrificial oxide film for protecting the first polysilicon film and P^- type silicon semiconductor substrate, is formed by CVD, in order that the surface of first polysilicon film 24, which serves as the floating gate 24a of the non-volatile memory cell, may not be oxidized. If the sacrificial layer is formed by thermal oxidization (usually performed at 800 - 1000°C), the polysilicon film 24 must be subjected to high heat thermal oxidization twice, which may emphasize the asperity of the surface of the film 24, thereby decreasing the breakdown voltage of a cell and hence the reliability thereof. Consequently, it is more desirable to deposit the sacrificial oxide layer through a process performed at low temperature such that oxidation may be suppressed, than by thermal oxidization performed at high temperature.

Though the sacrificial oxide film is formed by CVD in the embodiment, it can be deposited by any other process, if the process is performed at low temperature. Further, this film can be an insulating film made of a material other than an oxide.

Moreover, the embodiment employs N-channel MOSs, but it can employ P-channel MOSs or complementary MOSs. The present invention can be applied to an EEPROM, a non-volatile memory cell of another type, or a flash EEPROM (which allows one-time erasure of the EEPROM).

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A method of manufacturing a semiconductor device having a non-volatile memory cell region (10) and a logic region (11) including MOS transistors, characterized by comprising the steps of:

   forming in succession a first insulating film (23) and a first electrode layer (24) on a semiconductor substrate (22);

   removing the first insulating film (23) and first electrode layer (24) which are located in the logic region (11), without removing the first insulating film (23) and first electrode layer (24) which are located in the non-volatile memory cell region (10);

   forming a sacrificial film (25) for insulation over the entire surface in the memory cell region (10) and logic region (11); and coating a resist film (26) on the sacrificial film (25);

   forming an opening in a desired portion of the resist film (26), and implanting impurity ions into the semiconductor substrate (22) located in the logic region (11) through the opening; and

   removing the resist film (26) and sacrificial film (25), and forming in succession a second insulating film (28) and a second electrode layer (29) in the non-volatile memory cell region (10) and logic region (11).

2. The method according to claim 1, characterized in that the sacrificial film (25) is an insulating film formed by chemical vapor deposition.

Patentansprüche

1. Verfahren zum Herstellen einer Halbleitervorrichtung mit einem nicht-flüchtigen Speicherzellenbereich (10) und einem Logikbereich (11) einschließlich MOS-Transistoren, gekennzeichnet durch die Schritte:
   aufeinanderfolgendes Bilden eines ersten Isolierfilms (23) und einer ersten Elektrodenschicht

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gion, thereby protecting them from contamination caused by a resist film to be formed later, or ions to be implanted later. The film 25 is a deposited sacrificial oxide film for insulation.

Referring to Fig. 1C, a resist film 26 is formed on the oxide film 25, and then an opening is formed in the resist film 26 at a desired location in the logic region 11, through the opening impurity ions are implanted, thereby forming a channel region 27. After removing the resist film 26, the oxide film 25 is also removed by etching in NH_4F solution, which prevents the material of the resist film from remaining in the semiconductor integrated circuit. Heat process can be applied to the wafer in non-oxidizing atmosphere to electrically activate the impurity ions after removing the resist film 26. If the resist material remains in the circuit, the material is scattered therein during heating etc. performed later, which may deteriorate the quality of the device.

Subsequently, as is shown in Fig. 1D, a second gate oxide film 28 is formed by thermal oxidization at 900 - 1000°C in the atmosphere of oxygen, and a second polysilicon film 29 having a thickness of 0.4 μm is deposited on the film 28. Then, as is shown in Fig. 1E, that portion of the second polysilicon film 29 located in the non-volatile memory cell region 10 and the remaining first polysilicon film 24 are subjected to self align dry etching, thereby forming a non-volatile memory cell comprising a control gate 29a and a floating gate 24a. On the other hand, that portion of the second polysilicon film 29 located in the logic region 11 is subjected to dry etching, thereby forming a gate electrode 29b.

Referring to Fig. 1F, impurity ions are implanted into the substrate, forming N^+ type drain regions 33 and N^+ type source regions 34 for the MOS transistors in the logic region 11, and for the EPROM in the non-volatile memory cell region 10, respectively. Thereafter, an oxide film 35 and a passivation film 36 are provided on the chip. Contact holes are formed in the films 35 and 36, through which A1 wiring 37 is formed.

As is described above, the deposited sacrificial oxide film for protecting the first polysilicon film and P^- type silicon semiconductor substrate, is formed by CVD, in order that the surface of first polysilicon film 24, which serves as the floating gate 24a of the non-volatile memory cell, may not be oxidized. If the sacrificial layer is formed by thermal oxidization (usually performed at 800 - 1000°C), the polysilicon film 24 must be subjected to high heat thermal oxidization twice, which may emphasize the asperity of the surface of the film 24, thereby decreasing the breakdown voltage of a cell and hence the reliability thereof. Consequently, it is more desirable to deposit the sacrificial oxide layer through a process performed at low temperature such that oxidation may be suppressed, than by thermal oxidization performed at high temperature.

Though the sacrificial oxide film is formed by CVD in the embodiment, it can be deposited by any other process, if the process is performed at low temperature. Further, this film can be an insulating film made of a material other than an oxide.

Moreover, the embodiment employs N-channel MOSs, but it can employ P-channel MOSs or complementary MOSs. The present invention can be applied to an EEPROM, a non-volatile memory cell of another type, or a flash EEPROM (which allows one-time erasure of the EEPROM).

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A method of manufacturing a semiconductor device having a non-volatile memory cell region (10) and a logic region (11) including MOS transistors, characterized by comprising the steps of:

   forming in succession a first insulating film (23) and a first electrode layer (24) on a semiconductor substrate (22);

   removing the first insulating film (23) and first electrode layer (24) which are located in the logic region (11), without removing the first insulating film (23) and first electrode layer (24) which are located in the non-volatile memory cell region (10);

   forming a sacrificial film (25) for insulation over the entire surface in the memory cell region (10) and logic region (11); and coating a resist film (26) on the sacrificial film (25);

   forming an opening in a desired portion of the resist film (26), and implanting impurity ions into the semiconductor substrate (22) located in the logic region (11) through the opening; and

   removing the resist film (26) and sacrificial film (25), and forming in succession a second insulating film (28) and a second electrode layer (29) in the non-volatile memory cell region (10) and logic region (11).

2. The method according to claim 1, characterized in that the sacrificial film (25) is an insulating film formed by chemical vapor deposition.

Patentansprüche

1. Verfahren zum Herstellen einer Halbleitervorrichtung mit einem nicht-flüchtigen Speicherzellenbereich (10) und einem Logikbereich (11) einschließlich MOS-Transistoren, gekennzeichnet durch die Schritte:
   aufeinanderfolgendes Bilden eines ersten Isolierfilms (23) und einer ersten Elektrodenschicht

(24) auf einem Halbleitersubstrat (22);
Entfernen des ersten Isolierfims (23) in der ersten Elektrodenschicht (24), welche in dem Logikbereich (11) angesiedelt sind, ohne Entfernen des ersten Isolierfilms (23) und der ersten Elektrodenschicht (24), welche in dem nicht-flüchtigen Speicherzellenbereich (10) angesiedelt sind;
Bilden eines Opferfilms (25) zur Isolation über der gesamten Oberfläche in dem Speicherzellenbereich (10) und Logikbereich (11); und Auftragen eines Lackfilms (26) auf dem Opferfilm (25);
Bilden einer Öffnung in einem gewünschten Abschnitt des Lackfilms (26) und Implantieren von Verunreingungsionen in das Halbleitersubstrat (22), das in dem Logikbereich (11) angesiedelt ist, durch die Öffnung; und
Entfernen des Lackfilms (26) und Opferfilms (25), und aufeinanderfolgendes Bilden eines zweiten Isolierfilms (28) und einer zweiten Elektrodenschicht (29) in dem nicht-flüchtigen Speicherzellenbereich (10) und Logikbereich (11).

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß der Opferfim (25) ein Isolierfilm ist, der durch chemische Dampfphasenabscheidung gebildet ist.

Revendications

1. Un procédé de fabrication de dispositif semiconducteur ayant une région (10) de cellule de mémoire non rémanente et une région (11) logique incluant des transistors MOS,
caractérisé en ce qu'il comprend les étapes de :
formation successivement d'un premier film (23) isolant et une première couche (24) d'électrode sur un substrat (22) de semiconducteur ;
retrait du premier film (23) isolant et de la première couche (24) d'électrode, qui sont situés dans la région (11) logique, sans retrait du premier film (23) isolant et de la première couche (24) d'électrode, qui sont situés dans la région (10) de cellule de mémoire non rémanente ;
formation d'un film (25) secrificiel pour isolation au-dessus de la surface entière dans la région (10) de cellule de mémoire et la région (11) logique ; et dépôt par enduction d'un film (26) de résiste sur le film (25) sacrificiel ;
formation d'une ouverture dans une portion désirée du film (26) de résiste, et implantation d'ions d'impureté dans le substrat (22) de semi-conducteur situé dans la région (11) logique, à travers l'ouverture ; et
retrait du film (26) de résiste et du film (25) sacrificiel, et formation successivement d'un second film (28) isolant et d'une seconde couche (29) d'électrode dans la région (10) de cellule de mémoire non rémanente et la région (11) logique.

2. Le procédé selon la revendication 1, caractérisé en ce que le film (25) sacrificiel est un film isolant formé par dépôt de vapeur chimique.