CLAIMS

What is claimed is

1. A method to fabricate semiconductor devices with die sizes larger than 900mm^2, the method comprising:

providing a first type of source wafers that contain high-resolution circuit elements partitioned into a multitude of pre-fabricated blocks (PFBs), wherein each PFB is at most 900mm^2 in size;

providing a second type of source wafers that contain lower-resolution circuit elements partitioned into a multitude of PFBs, wherein each PFB is at most 1500mm^2 in size;

assembling PFBs from the first type of source wafers onto a product substrate, followed by assembling PFBs from the second type of source wafers onto previously assembled PFBs, wherein the fully-assembled group of high-resolution and low-resolution PFBs is equivalent in function to a monolithically constructed SoC but arbitrarily larger in size than 900mm^2.

2. The method of claim 1, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

3. The method of claim 1, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

4. The method of claim 1, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

5. The method of claim 1, wherein the first type of source wafers or the second type of source wafers have multiple kinds of PFBs.

6. The method of claim 1, wherein the PFBs are less than 10um thick.

7. The method of claim 1, wherein the PFBs are less than 1um thick.

8. The method of claim 1, wherein the PFBs are less than 100nm thick.

9. The method of claim 1, wherein the low-resolution PFBs contain custom-metal dies (CMDs) that include only metal layers.

10. The method of claim 1, wherein a superstrate assembly is used to pick-and-place PFBs and wherein the superstrate assembly has one or more, connected or unconnected, sub-superstrates.

11. The method of claim 10, further comprising controlling, using an overlay control architecture, distortions in PFBs to nanometer scales.

12. The method of claim 10, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

13. The method of claim 10, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

14. The method of claim 1, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive;

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

15. The method of claim 1, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the first type of source wafers and the second type of source wafers.

16. The method of claim 15, wherein the goodness of an entire PFB is inferred by testing select portions of the PFBs, and extrapolating using statistical models.

17. A method to ensure hardware security during fabrication of semiconductor devices, the method comprising:

providing a first type of source wafers that contain high-resolution circuit elements partitioned into a multitude of pre-fabricated blocks (PFBs), wherein the first type of source wafers can be fabricated at one or more, trusted or untrusted facilities;

providing a second type of source wafers that contain lower-resolution circuit elements partitioned into a multitude of PFBs, wherein the second type of source wafers can be fabricated at one or more, trusted or untrusted facilities; and

assembling PFBs from source wafers of the first type on to a product substrate, followed by assembling PFBs from source wafers of the second type onto previously assembled PFBs, wherein the fully-assembled group of high-resolution and low-resolution PFBs is equivalent in function to a monolithically constructed SoC, wherein the assembly is performed at a trusted facility.

18. The method of claim 17, wherein the overlay precision between the high and low resolution PFBs is better than 100nm.

19. The method of claim 17, wherein the overlay precision between the high and low resolution PFBs is better than 50nm.

20. The method of claim 17, wherein the overlay precision between the high and low resolution PFBs is better than 25nm.

21. The method of claim 17, wherein a source wafer has multiple kinds of PFBs.

22. The method of claim 17, wherein the PFBs are less than 10um thick.

23. The method of claim 17, wherein, the PFBs are less than 1um thick.

24. The method of claim 17, wherein the PFBs are less than 100nm thick.

25. The method of claim 17, wherein the low-resolution PFBs contain only custom-metal dies (CMDs) having only metal layers.

26. The method of claim 17, wherein a superstrate assembly is used to pick-and-place PFBs, wherein superstrate assembly has one or more, connected or unconnected, sub-superstrates.

27. The method of claim 26, wherein an overlay control architecture is used to control distortions in PFBs to nanometer scales.

28. The method of claim 26, wherein the superstrate assembly and/or sub-superstrates have routing for sacrificial layer etchants to etch PFB tethers in-situ.

29. The method of claim 26, wherein the superstrate assembly and/or sub-superstrates have airflow routing for vacuum pickup.

30. The method of claim 17, wherein pick-and-place assembly is implemented with PFBs that are wafer thick, the pick-and-place assembly further comprising:

providing a transparent, thermo-mechanically stable substrate;

attaching the PFB-containing source wafer to the transparent, thermo-mechanically stable substrate using an adhesive; and

dicing of source wafer into PFBs; and

pick-and-place of PFBs from the transparent substrate onto the product substrate using a nano-precise pick-and-place assembly process.

31. The method of claim 17, further comprising testing the PFBs on the source wafers to identify good known PFBs for assembly, wherein the testing determines good known PFBs by functionality and connectivity checks, and wherein the testing utilizes areas on the inside, periphery or outside of the PFBs the first type of source wafers and the second type of source wafers.

32. The method of claim 31, wherein the goodness of an entire PFB is inferred by testing select portions of the PFBs, and extrapolating using statistical models.