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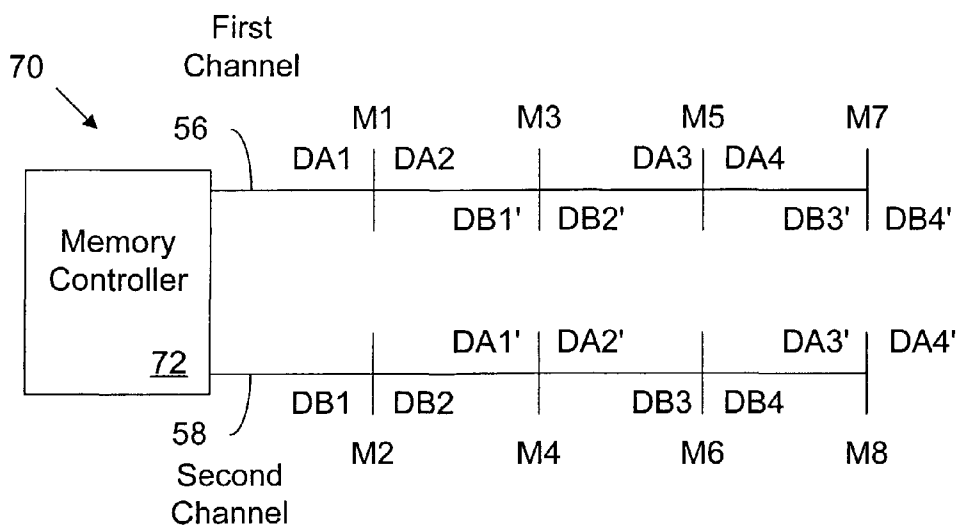
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(54) Title: MEMORY CONTROLLERS WITH INTERLEAVED MIRRORED MEMORY MODES



(57) Abstract: In some embodiments, a memory controller includes first and second memory channel interfaces and memory access control circuitry. The memory access control circuitry is to send first and second primary data sections to the first and second memory channel interfaces, respectively, and send first and second redundant data sections to the second and first memory channel interfaces, respectively. The first and second redundant data sections are redundant with respect to the first and second primary data sections, respectively. Other embodiments are described and claimed.

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