

METHOD OF LAYERING CACHE AND ARCHITECTURAL
SPECIFIC FUNCTIONS

ABSTRACT

Cache and architectural specific functions (212, 214, 218) are layered within a controller (202), simplifying design requirements. Faster performance may be achieved and individual segments of the overall design may be individually tested and formally verified. Transition between memory consistency models is also facilitated. Different segments of the overall design may be implemented in distinct integrated circuits, allowing less expensive processes to be employed where suitable.

Fig. 1

This Sheet Has Been Replaced

